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AN APPROACH TO DESIGN OF DIGITAL SLIDING MODE CONTROL FOR DC-DC CONVERTERS

Ph.D. dissertation

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JEDAN PRISTUP PROJEKTOVANJU DIGITALNOG UPRAVLJANJA S KLIZNIM REŽIMOM ZA DC-DC KONVERTORE

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SUMMARY

An Approach to Design of Digital Sliding Mode Control for DC-DC Converters

The primary goal of research in this Ph.D. dissertation is to investigate the possibilities of application of modern control methods in controlling the output voltage of the DC-DC converters (buck, boost) in order to ensure the system robustness to the input voltage and load variations. This dissertation deals with the analysis and application of sliding mode control algorithms in the synthesis of these converters in order to improve the properties of existing converters and to modify them, as well as to adjust and tune the digital sliding mode controls based on the input-output plant model to be applicable in these converters.

The design procedure is based on the converter models given in the form of discrete transfer functions. The proposed control for converters is a combination of the digital sliding mode control and (generalized) minimum variance control techniques. The problem caused by an unstable zero of the boost converter, which prevents the direct control of the output voltage of this converter, has been overcome by introducing the generalized minimum variance control. Also, only the output voltage of converter must be measured for the realization of the proposed control, so there is no need for an additional current sensor. This dissertation includes the modification of the developed algorithms with the aim of applying them to low-cost, standard 8-bit microcontrollers.

Finally, the efficiency of the proposed solutions is verified by digital simulation and a series of experiments on the laboratory developed prototypes of both converters, as well as by their comparative analysis. The satisfactory experimental results are obtained regarding the typical characteristics of the converters.

Keywords: buck converter, boost converter, quasi-sliding mode, digital sliding mode control, (generalized) minimum variance control, pulse width modulation, continuous conduction mode.

REZIME

Jedan pristup projektovanju digitalnog upravljanja s kliznim režimom za DC-DC konvertore

Glavni cilj istraživanja u ovoj doktorskoj disertaciji je istraživanje mogućnosti primene savremenih upravljačkih metoda u regulaciji izlaznog napona DC-DC konvertora (buck, boost), kako bi se obezbedio sistem robustan na promenu ulaznog napona i opterećenja. Ova disertacija bavi se analizom i primenom algoritama upravljanja s kliznim režimom u sintezi ovih konvertora sa ciljem poboljšanja osobina i modifikacije postojećih konvertora, kao i prilagođavanja digitalnog upravljanja s kliznim režimom zasnovanim na ulazno-izlaznom modelu objekta za njihovu primenu na ove konvertore.

Procedura projektovanja zasniva se na modelima konvertora datim u obliku diskretne funkcije prenosa. Predložena upravljanja za konvertore zasnovana su na kombinaciji digitalnog upravljanja s kliznim režimom i upravljanja (uopštene) minimalne varijanse. Problem izazvan nestabilnom nulom boost konvertora, koja sprečava direktno upravljanje izlaznog napona ovog pretvarača, je prevaziđen na ovaj način uvođenjem upravljanja uopštene minimalne varijanse. Takođe, za realizaciju predloženog upravljanja potrebno je da se meri samo izlazni napon konvertora. Struju kroz kalem pretvarača nije potrebno meriti, pa samim tim ne postoji potreba za dodatnim senzorom struje. Ova disertacija obuhvata modifikaciju razvijenih algoritama s ciljem njihove primene na jeftinim, standardnim 8-bitnim mikrokontrolerima.

Na kraju, efikasnost predloženih rešenja verifikovana je digitalnim simulacijama i nizom eksperimenata na razvijenim laboratorijskim prototipovima oba konvertora i njihovom uporednom analizom. Pri tome su dobijeni zadovoljavajući eksperimentalni rezultati u pogledu tipičnih karakteristika konvertora.

Ključne reči: buck konvertor, boost konvertor, kvazi-klizni režim, digitalno upravljanje s kliznim režimom, upravljanje (uopštene) minimalne varijanse, širinsko impulsna modulacija, režim kontinuiranog provođenja.

LIST OF ABBREVIATIONS

C

C	Capacitance
CCM	Continuous Conduction Mode

D

d	Duty Cycle
DCM	Discontinuous Conduction Mode
DSM	Digital Sliding Mode
DSMC	Digital Sliding Mode Control
DSMCGMVC	Digital Sliding Mode Control Based on Generalized Minimum Variance Control
DSMCMVC	Digital Sliding Mode Control Based on Minimum Variance Control
DSP	Digital Signal Processor
DPWM	Digital Pulse Width Modulator

E

EMC	Electro-magnetic Compatibility
EMI	Electro-magnetic Interference

F

f_s	Switching Frequency

G

GMV	Generalized Minimum Variance
GMVC	Generalized Minimum Variance Control

I

i_L	Inductance current
i_C	Capacitance current
i_R	Load current

K

KCL	Kirchhoff Current Law

KVL	Kirchhoff Voltage Law

L

L	Inductance
LFR	Loss-Free Resistor

M

MV	Minimum Variance
MVC	Minimum Variance Control
MPPT	Maximum Power Point Tracking

P

PD	Proportional Derivative controller
PI	Proportional Integral controller
PID	Proportional Integral Derivative controller
PV	Photovoltaic
PVT	Process, Voltage and Temperature
PWM	Pulse Width Modulation

Q

QSM	Quasi-Sliding Mode

R

R_L	Load Resistance

S

SISO	Single-Input-Single Output
SM	Sliding Mode
SMC	Sliding Mode Control
SMPS	Switch Mode Power Supply

T

T	The total period of the signal
T_{on}	Time where the signal is active

U

$\hat{u}$	Small-signal input vector
u	Input vector

V

V_i	Input Voltage
V_o	Output Voltage
V_{ref}	Reference voltage
VSC	Variable Structure Control
VSCS	Variable Structure Control System
VSS	Variable Structure System

X

$\hat{x}$	Small-Signal State Vector
x	State Vector

Y

$\hat{y}$	Small-Signal Output Vector

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CONTENT

1 INTRODUCTION

1.1 MOTIVATION

For many years, DC power supplies based on transformers and rectifiers have been the most used devices as DC voltage supplies for electric circuits but nowadays DC-DC converters based on switched mode are widely used as devices that convert DC voltage from one level to another with different methods of conversion. The switching process is achieved by using the pulse/pause ratio of the switching elements in the circuit, so that the DC component of the output voltage is equal to a given reference value. In this Ph.D. dissertation, a design of two most commonly used converter topologies namely buck (step-down) and boost (step-up) converters will be considered by implementing a sliding mode control (SMC) strategy.

It is well known that the SMC belongs to the wider group of a nonlinear control named variable structure control systems (VSCS). The sliding mode occurs when control input forces the motion of system phase point towards a predetermined sliding surface, which is determined by a switching function, providing the system robustness with external disturbances and parameter variations. As a consequence, the system order is reduced. Because of these features, the SMC is recommended for the converters with a variable load. On the other hand, the switching control signal frequency of SMC varies and this variation can lead to the significant losses in coils, as well as in transformer cores, producing electro-magnetic interference (EMI). The pulse width modulation (PWM), known as a pulse/pause control, is used as a solution to this problem.

The development of digital technology based on the use of microprocessors, microcontrollers and digital signal processor (DSP) enables the easy and fast realization of SMC algorithms but at the same time creates new problems and causes new phenomena that do not occur in continuous-time systems, which is called quasi-sliding mode (QSM). In both cases, i.e., continuous-time and digital SMC, the plant state coordinates must be known, which means implementing a state observer in the control design. This observer in digital SMC (DSMC) does not cause a major problem but it complicates the control algorithm. Another DSMC algorithms are introduced, which use only the plant output measurements and are based on the (generalized) minimum variance control ((G)MVC). This method is also robust to external disturbances and parameter perturbations and it will be the backbone in the development of new control strategies for DC-DC converters presented in this work.

The relevance and attractiveness of this dissertation are established by a large number of scientific papers published previously. These articles mainly deal with the application of SMC in the synthesis of DC-DC converters.

The main idea of this dissertation is to provide a unified approach to control of DC-DC buck and boost converters based on DSMC theory. The control algorithms should be simple enough to be implemented on standard 8-bit microcontrollers without using additional current sensors, as well as to deal with the unstable zero dynamics of the boost converter.

The systematization and development of mathematical models, which will be used in the process of designing control algorithms for DC-DC converters, are conducted, as mathematical models of the converter define the paths to the development of various control strategies used for the practical realization of these devices. Therefore, particular attention will be paid to the analysis of different models of buck and boost converters. The aim is to perform the selection of that model that will be most appropriate for the development of universal solutions for controlling these converters. Regardless of the primary form of converter design, all of them will be transformed into the form of the discrete-time transfer function. Stable output voltages and system robustness to parameter and load influence are reached using the control law that combines digital sliding mode and (G)MVC variance control techniques. The control laws are realized by using only the converter output. This combination of GMVC or MVC with DSMC alleviates the drawbacks of (G)MVC, achieves a required accuracy of tracking or ensures a zero error signal. This strategy will be implemented on DC-DC buck and boost converters. Particular attention will be paid to the boost converter because its model in state-space contains the right zero (non-minimum phase plant), which significantly complicates the design of the controller. In this case, DSMC algorithm based on GMVC must be implemented [1], [2].

DSPs are traditionally used to control the voltage of the DC-DC converters based on the state-space model. In [3], the hysteresis SMC based on the state-space model is implemented using inexpensive memory components such as the values of the sliding surface and the proper control signals are stored in the memory chip as a lookup table. Then, the outputs are used to control the switching element of the converter. On the other hand, continuous-time SMC, depending on the model in the state-space, is digitally implemented by dsPIC30F4013 [4] characterized by weaker computing performance. Therefore, this Ph.D. dissertation includes the development of algorithms and their modifications for implementation on an

inexpensive, standard 8-bit microcontroller. The obtained experimental results validate the good performances of designed converters.

The manuscript contains the introduction, four chapters, the concluding remarks and the list of the literature that was used. The second chapter presents DC-DC converters models: the state-space average model, the small signal state-space model and the appropriate models in the form of transfer functions. In Chapter 3, the basic principles of SMC, both in continuous- and discrete-time domain, are considered. An overview of SMC design methods for buck and boost converters is given in Chapter 4. Finally, in Chapter 5, new approaches in the design of DC-DC buck and boost converters with DSMC are presented. The experimental prototypes are developed and several experiments are conducted to validate the functionalities of the proposed solutions. The experimental results are compared with the digital simulation ones showing large matching. The dissertation ends with the concluding remarks and the list of references.

1.2 DC-DC Converters (Classification, Types, Operational Modes)

In everyday use, electronic circuits are needed, which are assumed to operate by their own power supplies, usually considered to be constant. These power supplies have control circuits that maintain the output voltage as constant as possible irrespective of change in load current or line voltage. Thanks to the improvement of technology, a variety of control schemes are available, which can meet the strict requirement for accurate and fast regulation of the output voltage. These power supplies contain three critical parts: power stage, power converter and controller, as depicted in Figure 1.1.

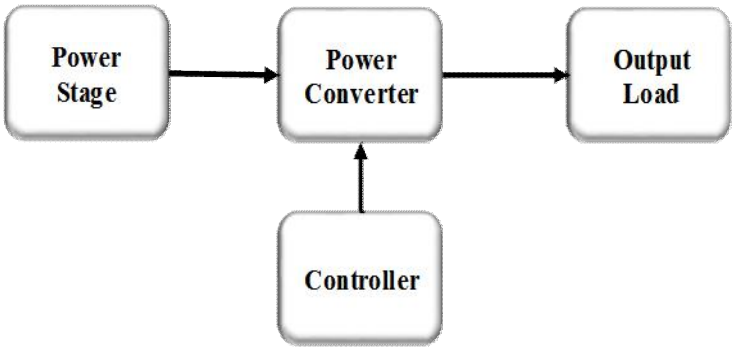


Figure 1.1 *Basic power electronic system*

1.2.1 CLASSIFICATION OF DC-DC CONVERTERS

The DC-DC converters can be divided either according to the power conversion systems or to the waveforms of input and output signals as shown in Figure 1.2 [5].

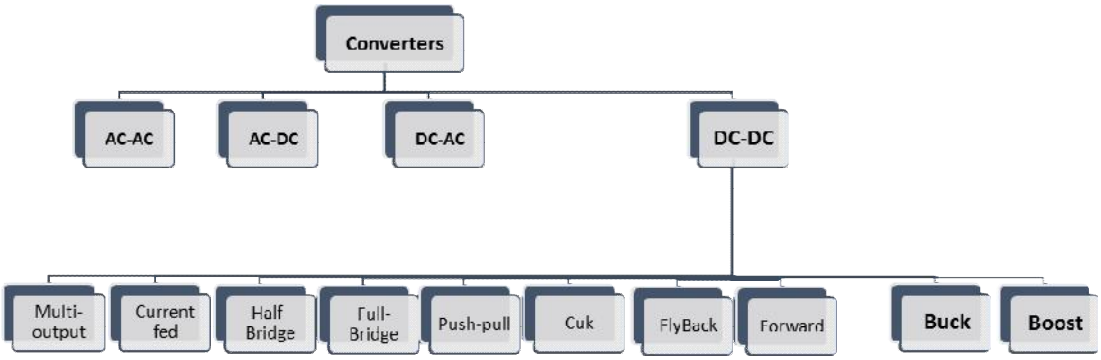


Figure 1.2 *Classification of DC-DC converters*

The functions of DC-DC converters are to:

1) change the DC input voltage V_i into the DC output voltage V_o,
2) regulate the DC output voltage against load and line variations,
3) reduce the voltage ripple on the DC output voltage to the required level,
4) provide isolation between the input source and the load (the isolation is not always necessary),
5) look after the supplied system and the source of electro-magnetic interference (EMI),
6) meet various international and national safety standards.

DC-DC converters present a method of generating several controlled voltages from a single variable battery voltage, thus saving space as a replacement for using multiple batteries to supply different parts of the device.

1.2.2 DC-DC CONVERTERS TYPES

Each DC-DC converter consists of electrical components. These electrical components can be combined and connected to each other in a variety of ways, resulting in what is called topologies. Each of them has different specifications. The buck and boost are primary converter topologies [6], [7]. These topologies can be illustrated by using Figure 1.3 in the following manner:

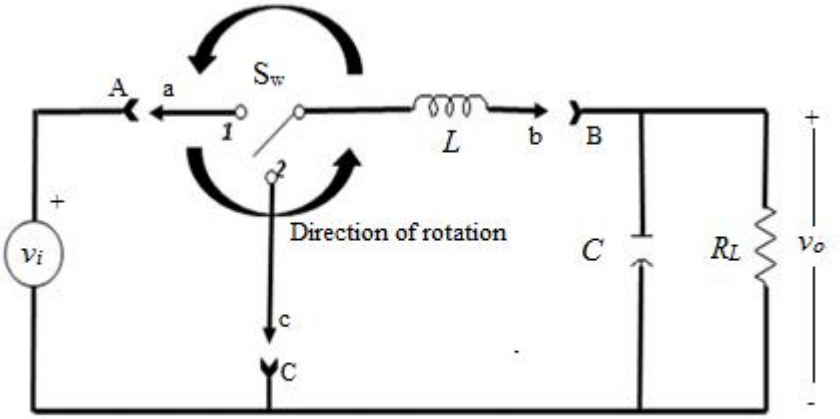


Figure 1.3 *DC-DC Converter topologies*

1) DC-DC buck converter (connect), as: $a \to A$, $b \to B$, $c \to C$,
2) DC-DC boost converter (rotate anti-clockwise), as: $a \to C$, $b \to A$, $c \to B$.

In the theory of DC-DC converters, there are different types of conversion methods such as linear, electronic, switched mode, magnetic and capacitive.

1.2.2.1 Linear Mode Power Supply

Linear power regulators are based on the voltage or current divider. They have a limitation that the output voltage must be lower than the input one. They also require low-frequency transformer and filters and can be implemented at the low-power levels as the low-dropout voltage regulators. Therefore, they are inefficient. On the other side, the linear regulators can provide a very high-quality output voltage, as the electronic devices used in these regulators operate in their linear modes.

For a long time, these linear regulators have been broadly used by many devices as power supply units until switch mode power supplies became widespread after the 1960s. Indeed, linear regulators are still widely utilized in an extensive range of applications. Because of their simplicity, these regulators have other performance advantages such as simple/low-cost solutions, low noise/low ripple applications, fast transient applications and low dropout applications. A notable drawback of utilizing linear regulators can be the excessive power dissipation. Linear regulators are straightforward and easy to use. Since their transistors operate in a linear mode, supply effectiveness is usually low when the output voltage is much lower than the input voltage.

1.2.2.2 SWITCH MODE POWER SUPPLY

One of the most widely used converters is the switch mode power supply (SMPS). It got its name because of a switching operation (ON-OFF) at high-frequency. ON and OFF periods are adequately controlled so that the average DC voltage applied to the output circuit equals to the preferred magnitude of the output voltage. The duty-ratio cycle (*d*) is the ratio of ON time to the cycle time (ON plus OFF time) of the converter circuit. The high switching frequency and the ripple voltage at the converter output during the duty ratio is the result of fast control, therefore the low-pass filter is applied to the circuit followed by the load. Low values of filter capacitors and inductors are utilized in order to effectively filter this high-frequency ripple in voltage [8], [9]. This conversion strategy is more power proficient than linear voltage conversion, which must dissipate undesirable power. This proficiency is helpful to expand the running time of battery operated devices. The drawback of switching converters is the electronic noises produced at high frequencies. The switching process of DC-DC converters can be achieved through:

1) power bipolar junction transistor (BJT),
2) metal oxide semiconductor field effect transistor (MOSFET),
3) gate turn-off thyristor (GTO) and
4) insulated gate bipolar transistor (IGBT).

The comparison between linear and switch mode power supplies provides the conclusion that in the linear regulator circuit the overabundance voltage from the unregulated DC input supply drops over an arrangement component (and therefore there are control drawbacks in the extent to this voltage drop), though in the switch mode circuit the unregulated segment of voltage is evacuated by modulating duty-ratio. The switching drawbacks in present-day switches (like MOSFETs) are substantially less contrasted with the drawbacks in the linear component.

The linear power supplies implement large and huge low-frequency transformer while DC-DC converters need a small high-frequency transformer. However, the linear power supply is bulkier and less efficient and has few points of interest as well as when contrasted with the switch mode control supply. In general, the control of linear power supply circuit is significantly less complicated than that of SMPS circuit. Since there is no high switching frequency, the switching related EMI is missing in linear power supplies. Additionally, as far as the output voltage regulation is concerned, the linear power supplies are better than SMPS. One would be rather able to effortlessly meet more tightly details on output voltage ripples by

utilizing linear power supplies. Because of the advantages of both types of power system mentioned above, a new regulator is formed - hybrid power supply.

Two categories of the DC-DC converters can be also identified according to isolation principle:

1) non-isolated converters with no galvanic isolation between the input and output of the system, such as synchronous buck, boost, Ćuk converters, etc., and
2) isolating converters with the inherent galvanic isolation between the input and output of the system, such as the full-bridge, half-bridge, push-pull, dual active bridge, forward or flyback converters.

1.2.2.3 NON-ISOLATING CONVERTERS

The non-isolating converters have no dielectric between the input and the output or, in other words, they share a common connection. The basic topologies for non-isolating converters are the buck and boost topologies.

Because of their lower cost and frequent use, these DC-DC converters are utilized as a part of negative ground submission in vehicles for different DC powered utilizations and equipment. The connection between the input and the output is the main disadvantage, which deals with little or no protection to the load for any high electrical voltage or current that appears at the part of the entry. These converters also have less noise filtering difficulty [10].

1.2.2.3.1 DC-DC BUCK CONVERTER

It is called the buck converter because the voltage across the inductor bucks or opposes supply voltage. This type of converters is also called step-down converter where the switch S_W is placed between the input voltage source v_i and the filter, as presented in Figure 1.3-1. The switch is used to replenish energy lost to the load during its OFF time. The inductor (L) and the shunt capacitor (C) present the energy storage reservoirs saving enough energy to maintain the load current.

1.2.2.3.2 DC-DC BOOST CONVERTER

This converter produces a higher average output voltage than the DC input voltage. The primary applications of the boost (step-up) converter (see Figure 1.3-2) are the regenerative braking of DC motors and regulated DC power supplies. The voltage across inductor L will

be added to the input supply voltage v_i to improve the output voltage v_o. This voltage is higher than the input voltage v_i and that is why it is called boost converter [11].

1.2.2.4 ISOLATING DC-DC CONVERTERS

Complete isolation between the input and the output is required for some applications, such as high voltage circuits, power metering systems, medical field and insulated-gate bipolar transistor (IGBT) controllers. The main classes of isolation are basic, operational or functional and reinforced.

The most used type in the industrial applications is the operational isolation, in which the primary and secondary windings of the transformer are wound overlaying each other. The inner magnetic fields are in this manner perfectly superimposed. Such design decreases, however, safety edges, as both windings are only separated by the respective wire covering thickness.

In any case, security and confirmation are the ultimate priority in electronic equipment for the use in the previously-mentioned applications. These viewpoints represent high-class requests for DC-DC power supply technology and producer as well.

The two main types of isolating converters are forward and flyback converters. The working principle of these converters depends upon the loading energy in the magnetic field of the inductor. Another definition of the isolated DC-DC converter is the ground isolated type or galvanic isolated type [12].

1.2.2.4.1 FLYBACK CONVERTER

This kind of converters works by storing energy in the transformer core during the ON state and releasing it to the output during the OFF state as shown in Figure 1.4. When the switch S_W is ON, the current starts to flow from the source through the primary winding L_1. This energy is stored in the transformer magnetic field. Later the switch S_W turns OFF and the transformer tries to keep current flow through L_1 by rapidly reversing the voltage across it. A higher flyback pulse is induced in the secondary winding L_2 due to the transformer action. In that way the current will supply the load and recharge the capacitor C through the diode d.

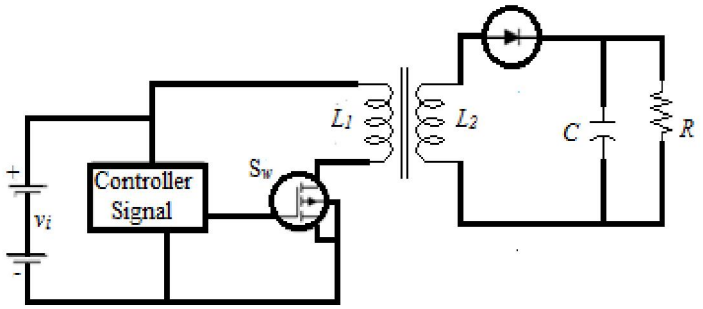


Figure 1.4 *Flyback Converter*

In this converter, two separate stages in its switching cycle are shown. During the first stage, the switch S_W conducts and the energy is kept in the transformer core through the primary winding L_1 while during the second stage (S_W turns OFF), the stored energy in the transformer is transported to the converter output through the secondary winding L_2. The input/output ratio depends on the turn ratio, the magnetic field, the winding inductance and the length of time during which S_W is turned on. The flyback converters have high turn ratio so as to enable a high voltage step-up ratio. The core in these converters must be also large to avoid saturation as the magnetic flux in this transformer core never opposes in polarity. A small winding is added to the flyback transformer for the automatic regulation of the output voltage in order to provide sensing of flyback pulse amplitude close to the output voltage and then feedback (supplying) the switch.

1.2.2.4.2 FORWARD CONVERTER

This converter comprises of a perfect transformer that converts the input AC voltage to an isolated secondary output voltage. This energy transfer requires one phase directly between the input and the output whereas the flyback converter requires two stages for storing energy and delivering it to the output. Figure 1.5 shows the circuit diagram of the forward converter.

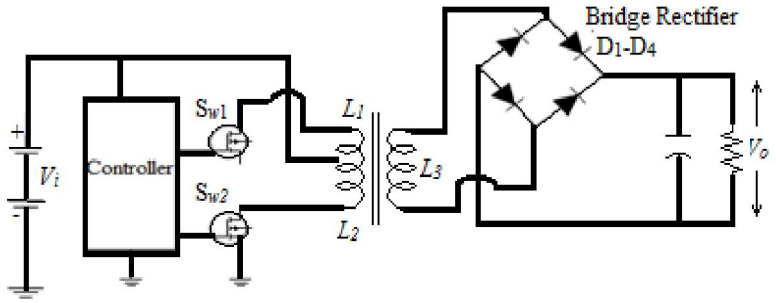


Figure 1.5 *Forward Converter*

The forward converter is of the push-pull type. It has two switches, S_{W1} and S_{W2}, connected to either end of the center-tapped primary winding of the transformer. The switching control circuit never turns on S_{W1} and S_{W2} at the same time. The positive terminal of the input voltage source is connected to the center tap and the negative terminal is attached to the sources of switches. Therefore the input voltage is first connected to one-half of primary winding and then across the other. Thus current flows through L_1 and then L_2. The S_{W1} and S_{W2} convert the DC input voltage into high-frequency AC square wave. The peak voltage during each half cycle is equal to:

$$V_{AC(peak)} = V_i \frac{N_3}{N_1} \tag{1.1}$$

where: N_1 and N_3 are the numbers of turns of each winding. The diodes that are connected directly to the secondary winding present a bridge rectifier. The AC signal that appears across L_3 is rectified back into high DC voltage supplying the load and ensuring the charge on the filter capacitor C. Ignoring the diode voltage drops, the DC output voltage V_o will be equal to the peak AC output from the transformer, i.e.: $V_o = V_{AC(peak)}$. The forward converter is used as a transformer for DC for the purpose of converting the DC energy into the AC energy. After the conversion, the AC voltage is rectified back into DC. The chances of saturation are less in the forwarding converter comparing to the flyback converter as the polarity of magnetic flux in the transformer core reverses for each alternate half cycle. The forward converters have also the tighter and predictable relationship between input and output making them suitable for high power applications.

1.2.3 Operating Modes of DC-DC Converters

The DC-DC converters can operate in two separate modes concerning the inductor current: a continuous conduction mode (CCM) in which the inductor current is always higher than zero and a discontinuous conduction mode (DCM) where the average value of the input current and the switching frequency f_s are low. In latter case, the inductor current is zero during a fraction of the switching period. The CCM is preferred for high efficiency and safe operation of semiconductor switches and passive parts. The DCM can be used in applications with special control requests since the effective order of the converter is decreased (the energy stored in the inductor is zero at the beginning and at the end of each switching period).

When it comes to the high efficiency and practical use of semiconductors, switches and passive components and because of their reliability, the converters with CCM can be selected while the converters with DCM can be used in applications with special control requirements such as fast response and lower cost because of the small inductor value. On the other hand, the DC-DC converter working in DCM has disadvantages such as load regulation problems (the converter ratio becomes load dependent) whereas the high current variation in the inductor may lead to magnetic saturation.

1.3 A Brief Survey of Different Control Approaches for DC-DC converters

Keeping the output voltage of DC-DC converter constant in the steady-state requires a control circuit that can implement different control methods. Some of these methods are shown in Figure 1.6.

The PWM voltage mode control, PWM current mode control with proportional (P), proportional integral (PI) and proportional integral derivative (PID) controllers are the most common approaches used for control of DC-DC converters. These control approaches are unable to perform acceptable results under serious parameter or load variation. The control circuit design can be based on Ziegler- Nichols's method [13], the root locus technique [14], the hysteresis control [15] and Bode plot, as well. Such approaches have good performance around the operating point but do not offer good large-signal operating conditions [16]. The hysteresis control methods are approaches that possess robustness with a simple design, they do not need feedback loop compensation, and they have a fast response to a load transient.

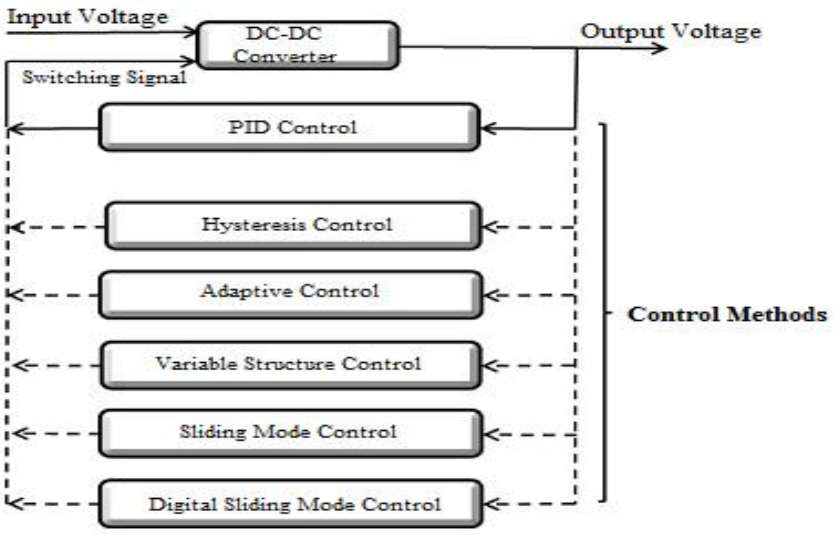


Figure 1.6 *The block diagram showing some methods used to control DC-DC converters*

As DC-DC converters represent nonlinear and time-variant systems, nonlinear controllers come into the focus for controlling them. In [17], the analysis and design of a hysteretic PWM controller with the improved transient response for a DC-DC buck converter is discussed. SMC is also nonlinear control technique, which makes DC-DC converters robust to parameter variations and external disturbances [18]. The use of PWM techniques in controlling converters that work in CCM may lead to the appearance of right zero in the transfer function of boost converter [19]. The non-minimum phase model of DC-DC boost converter complicates the design of the voltage regulator and significantly limits the bandwidth of the converter [20].

Another control approach for DC-DC converters is the DSMC. One such approach is used in the design of the digital control of DC-DC buck converter [21] wherein the control algorithm is implemented as a phase regulator that imitates the characteristics of a sliding mode. In [22], the design of DSMC for the DC-DC boost converter affected by disturbances is considered, such as the variations in the input voltage and the load resistance. In [23], Vivekanandan discusses the redefined discrete QSM control strategy, which improves the convergence rate of the system dynamics in the reaching mode for systems with both time-invariant disturbances and time-variant disturbances.

1.4 Implementation of DC-DC Converters

Due to their efficiency, high availability, high reliability, small size, lightweight and low-cost, DC-DC converters are widely used in many applications. They are power supplies, which operate under closed-loop feedback to produce preferred and regulated DC output voltage from an unregulated DC input voltage [24]. The buck converters find most of their applications in high-performance DC drive systems as in the electric vehicles. The DC motors with their winding inductances and mechanical inertia act as filters ensuing in high-quality armature currents. The boost converters are primarily used in radar and ignition systems, as well as in renewable energy sources.

The DC converters can be modified for two quadrant and four quadrant operation. Two quadrant converters may be part of the autonomous power supply systems that contain a battery, as in renewable DC devices (photovoltaic arrays), fuel cells or wind turbines. Four quadrant converters are used in drivers, where the breaking of DC motor is required, such as transportation systems with frequent stops. The isolated DC-DC converters can have multiple outputs, which are possible with additional secondary windings of transformers. Only one output is regulated by a feedback loop, but other outputs rely on the duty ratio of regulated

one and their loads. In the case of low-medium power applications (100-200W), the forward converter is mostly used, while in the case of low-power applications (<200W), the flyback converter is attractive. DC-DC converters have also primary applications related to the utility AC grid. For critical loads, in case that the utility grid fails, there must be a backup source of energy such as uninterrupted power supplies (UPSs). In UPSs, DC-DC converters are used to regulate the level of rectified grid voltage to that of backup source. Bidirectional DC-DC converters are converters that can be used in two modes: the first one wherein the power flows from the grid to the backup source and the second one wherein the power flows from the backup source to the load (at emergency conditions).

2 DC-DC CONVERTER MODELS

In the procedure of designing a control system for a converter, it is required to find a converter model in order to understand its dynamic behavior, which is unfortunately hampered by the nonlinearity nature of the switching and pulse width modulation process. Therefore, the mathematical models of converters provide the pathway to various control strategies discussed in the literature.

The state-space model averaging is one of many modern design methods used to model DC-DC converters. This methodology uses the state-space representations of the dynamical system to obtain the equations of PWM switching converters. The representations are averaged with respect to their duration in the switching period resulting in the nonlinear average model. The average model is then linearized at the operating point to form the linear time-invariant model. Finally, this linearized model is converted into a frequency domain, i.e., *s*-domain providing the transfer function. The second approach gives the small signal state-space model in the controllable canonical form by linearizing nonlinear model directly under the assumption that the converter has been already driven to the operating point.

2.1 PULSE WIDTH MODULATED DC-DC CONVERTER MODELS

PWM is a dominant technique used in power control, measurement and communication [25] due to their constant frequency, low component count, high efficiency, relatively simple control and its availability in integrated circuit controllers, as well as its ability to achieve high conversion ratios for both buck and boost converter application. This technique combines both voltage and frequency control. The output of the PWM circuit is a series of pulses of constant amplitude, in which the pulse duration is modulated to obtain the necessary signal.

In DC-DC converters, the control circuit regulates the output voltage by varying ON time of the switch and by fixing switching frequency using PWM circuit, i.e., the system dynamics is controlled by varying the duty cycle. Theoretically, the modulation frequency is the Nyquist frequency, so the carrier rate has to be more than twice the Nyquist frequency, but in practice, the carrier frequency must exceed the Nyquist frequency tenfold and more.

The most used techniques for controlling DC-DC converters are naturally sampled sine PWM (NSPWM), uniformly or regularly sampled sine PWM (USPWM) and space vector PWM (SVPWM). The NSPWM does not control the position of pulses, which are generated

in each cycle, and the minimum pulse width is not controlled. This technique is based on the comparison between the sine signal (modulation signal), and the triangle signal (high-frequency carrier signal) whereas the resulting signal is used to regulate the power switch of the converter. USPWM also uses the triangle carrier wave at the switching frequency and use the comparison result to determine the state duration of the switch (ON or OFF) but not the pulse position. SVPWM maps eight switching patterns of a three-phase full bridge converter into six 60^o apart space vectors on the same plane and two 0-axis vectors vertical to the plane whereas a reference vector on the plane is used as modulation signal and sets the time average of these switching patterns in each PWM cycle. If the reference vector rotates on the plane from sector to sector, a sine wave is modulated in the pulses.

The block diagram of the PWM DC-DC converter is given in Figure 2.1:

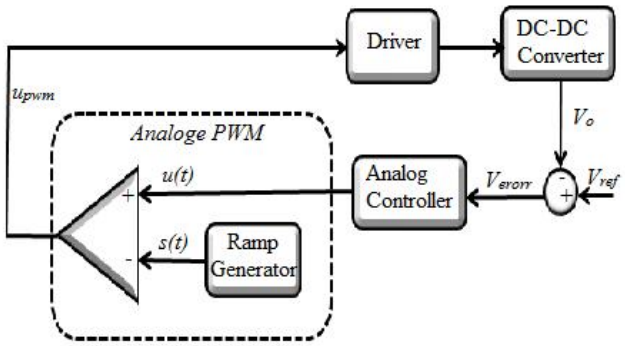


Figure 2.1 *Block diagram of the PWM DC-DC converter*

The controller monitors the output voltage and generates the signal u_{pwm} that controls the state of the converter switch (ON or OFF states). The durations of subintervals ON and OFF are related to the switching period T_s (the switching frequency is $f_s = 1/T_s$) and the duty ratio d by the equation (see Figure 2.2):

$$d = \frac{T_{ON}}{T_s},\ 1-d = \frac{T_{OFF}}{T_s}. \tag{2.1}$$

The traditional PWM compares a saw-tooth signal $s(t)$ with a signal $u(t)$ so the output signal is expressed as:

$$u_{pwm}(t) = \begin{cases} 1 & \text{if } s(t) < u(t) \\ 0 & \text{if } s(t) > u(t) \end{cases}. \tag{2.2}$$

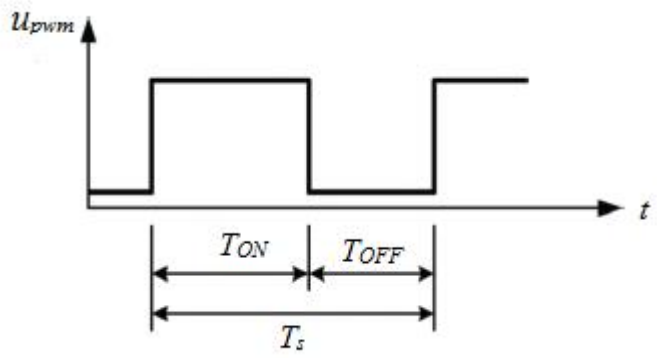


Figure 2.2 *The switching time T_s, ON and OFF periods*

Afterwards these PWM signals will be transferred to the switch device in the converter to control the output voltage. The analog PWM consists of a high gain operational amplifier, voltage controlled oscillator, ramp generator and a comparator. This technique has advantages such as simplicity, linearity and the ease of realization while this kind of PWM suffers from sensitivity to noise and process, voltage and temperature (PVT) variations.

The digital PWM (DPWM) uses the same principle described by (2.2) and possesses the quantization effect for a number comprised between 0 and 1 as the controller has a normalized output on the interval [-1, 1]. The accuracy of the output depends on the number of bits used for the DPWM. As a result, a source of error in the loop is decreased. The quantization block is represented in Figure 2.3. The number 2^{-n} relates to the number of the steps in the staircase signal, n is a number of total bits and is given by the equation:

$$n_{DPWM} = \left\lfloor n_{ADC} + \log_2\left(\frac{V_{out}H_v}{V_{fsADC}D_{\min}}\right)\right\rfloor + 1 = \left\lfloor \log_2\left(\frac{V_{out}H_v}{\Delta V_{qADC}D_{\min}}\right)\right\rfloor = \lfloor x \rfloor \tag{2.3}$$

where: V_{out} is the output voltage, $D_{\min}$ is the minimum duty cycle, $\lfloor x \rfloor$ is equivalent to the greatest integer greater or equal to x. The block diagram of DPWM controlled power converter is shown in Figure 2.4.

In the DPWM, a set of pulse widths (duty cycle) is produced depending on the input codes and the resolution of DPWM. The pulse width is equal to:

$$T_{ON} = \frac{D_{WORD}[n:0]}{2^n}T_{sw} \tag{2.4}$$

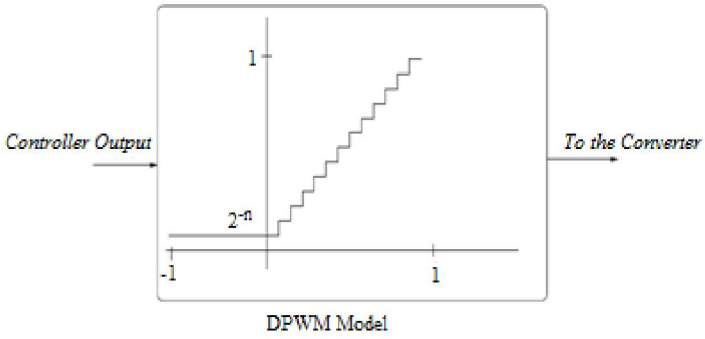


Figure 2.3 *The quantization block*

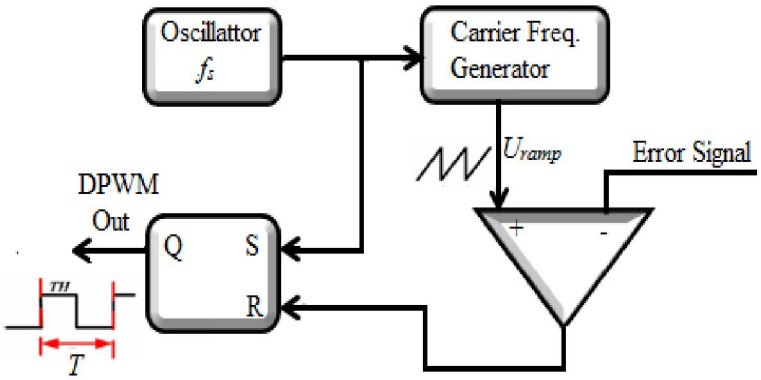


Figure 2.4 *The block diagram of the digital pulse width modulator*

where D_{WORD} is a decimal value of the input word for the DPWM, n is a number of bits in the word of entry for the DPWM, T_{sw} is a time period of switching clock of the converter.

The DPWM uses four techniques: DPWM Type I (Counter Method), DPWM Type II (Delay Line), DPWM Type III (Hybrid DPWM) and DPWM Type IV (Σ-Δ – DPWM).

The DPWM Type I depends on counting the time steps using a fast clock where frequency $f_{counter}$ is:

$$f_{counter}(n) = 2^n f_{sw} \tag{2.5}$$

where n is the number of bits introduced at the input of fast clock counter, f_{sw} is the switching frequency of the converter. This DPWM needs the *n*-bit counter and the *n*-bit digital comparator to implement the *n*-bit DPWM. The main drawback of this type is the need for the fast clock according to the increase of the resolution and switching frequency.

The DPWM Type II implements 2^n equally spaced transitions generated from matched delay cells to produce time steps wherein each delay element produces a delay equal to $\frac{T_{sw}}{2^n}$

so the need for the fast clock is ended. Matching of the delay elements, PVT variations and area are some of the biggest challenges in this type.

The DPWM Type III uses the merits of both types I and II. In this technique, the high DPWM resolution without increasing area and power requirements are achieved by dividing the design into two sets of delaying elements. It implements a counter for coarse delay generation and a delay locked loop to reach finer delay resolution between each coarse delay step. This type extensively improves area, power and clock requirement for higher resolution of the DPWM design.

The DPWM Type IV uses time domain averaging to reach high accuracy requirements. Averaging over time enables us to achieve sub low significant bit level accuracy without increasing the switching frequency of the switching clock. Using this type of DPWM, one can shape the switching noise and reduce the EMI/EMC challenges.

2.2 DC-DC BUCK CONVERTER MODELS

The DC-DC buck converter with real switching device that operates with the switching period T_s and the duty cycle d is considered in Figure 2.5.

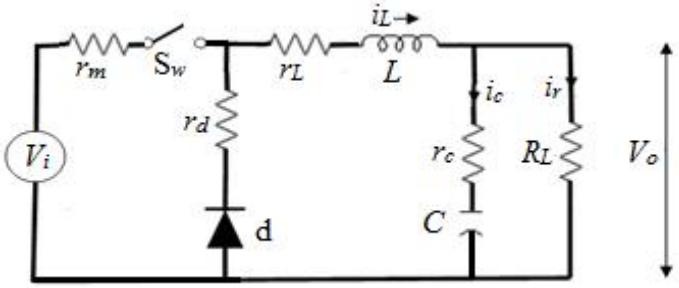


Figure 2.5 *The real DC-DC buck converter*

When the switch S_w is ON, as in Figure 2.6a, the current from the source V_i flows through the switch S_w, described by the parasitic resistance r_m, the coil (L, r_L), the capacitor (C, r_c) and finally to the load R_L (continuous line). The magnetic field is built up as the current flows through L, causing energy to be stored in the inductor. When S_W turns OFF, as in Figure 2.6b, the energy stored in the inductor supplies a current to the load through diode d (continuous line).

The voltage across the load is a fraction of the input voltage. This portion is called duty cycle (d). The duty cycle is once again the percentage of one period T_s in which a signal is active whereas the period T_s is the time it takes for a signal to complete the ON and OFF cycle.

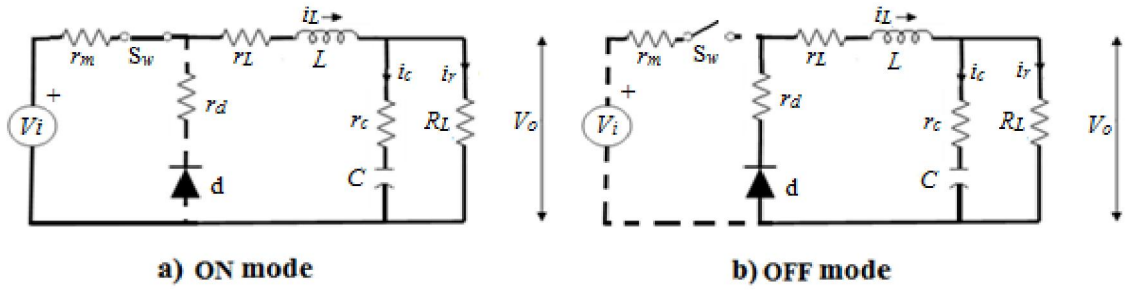


Figure 2.6 *The operational modes of DC-DC buck converter*

The duty cycle may be expressed as:

$$\frac{V_o}{V_i} = d = \frac{T_{on}}{T_s}. \tag{2.6}$$

The signal waveforms of DC-DC buck converter are shown in Figure 2.7.

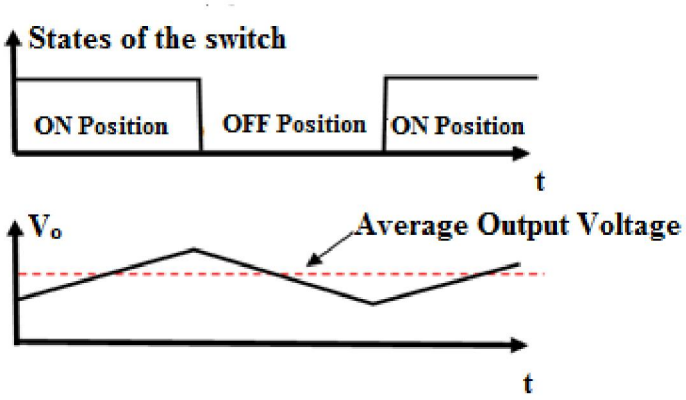


Figure 2.7 *The waveforms of DC-DC buck converter signals*

2.2.1 STATE-SPACE AVERAGE MODEL

A state-space average method is a way to extract various small-signals and averaged DC transfer functions. It is employed to get a set of equations that describe the system over one switching period. Theoretically, a dynamical system is described by a set of the first-order differential equations. These differential equations are adopted from the states of the switch S_W of the DC-DC buck converter. The resulting state-space description is called the switched state-space model [26]. It contains two modes: the ON mode and the OFF mode. The ON time is denoted by dT_s and the OFF time is denoted by $d'T_s = (1 - d)\ T_s$ where T_s is the PWM period. When the switch is ON, as shown in Figure 2.6a, the converter state-space model is given by:

$$\begin{aligned} \dot{x}(t) &= A_1 x(t) + B_1 v_i(t), \\ v_o(t) &= C_1 x(t) \end{aligned} \tag{2.7}$$

where:

$$A_1 = \begin{bmatrix} -\dfrac{R_L r_L + R_L r_c + R_L r_m + r_c r_L + r_c r_m}{(R_L + r_c)L} & -\dfrac{R_L}{(R_L + r_c)L} \\ \dfrac{R_L}{(R_L + r_c)C} & -\dfrac{1}{(R_L + r_c)C} \end{bmatrix},$$
$$B_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, \; C_1 = \begin{bmatrix} \dfrac{R_L r_c}{(R_L + r_c)} & \dfrac{R_L}{(R_L + r_c)} \end{bmatrix} \tag{2.8}$$

and $x(t) = \begin{bmatrix} i_L(t) & v_C(t) \end{bmatrix}^T$.

When the switch is in the OFF position (see Figure 2.6b), the converter state-space model is:

$$\begin{aligned} \dot{x}(t) &= A_2 x(t) + B_2 v_i(t), \\ v_o(t) &= C_2 x(t) \end{aligned} \tag{2.9}$$

where:

$$A_2 = \begin{bmatrix} -\dfrac{R_L r_c + R_L r_L + r_c r_L + R_L r_d + r_d r_c}{(R_L + r_c)L} & -\dfrac{R_L}{(R_L + r_c)L} \\ \dfrac{R_L}{(R_L + r_c)C} & -\dfrac{1}{(R_L + r_c)C} \end{bmatrix},$$
$$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \; C_2 = \begin{bmatrix} \dfrac{R_L r_c}{(R_L + r_c)} & \dfrac{R_L}{(R_L + r_c)} \end{bmatrix}. \tag{2.10}$$

Combining the equations (2.7), (2.8), (2.9) and (2.10), the average state-space model of DC-DC buck converter is obtained as:

$$\begin{aligned} \dot{x}(t) &= A_k x(t) + B_k v_i(t), \\ v_o(t) &= C_k x(t) \end{aligned} \tag{2.11}$$

where: $A_k = A_1 d + A_2(1\text{-}d)$, $B_k = B_1 d + B_2(1\text{-}d)$, $C_k = C_1 d + C_2(1\text{-}d)$. By denoting $P_1 = -(R_L r_L + R_L r_c + R_L r_m + r_c r_L + r_c r_m)$ and $P_2 = -(R_L r_c + R_L r_L + r_c r_L + R_L r_d + r_d r_c)$, A_k, B_k, and C_k are presented as:

$$A_k = \begin{bmatrix} \dfrac{P_1 d + P_2(1-d)}{(R_L + r_c)L} & -\dfrac{R_L}{(R_L + r_c)L} \\ \dfrac{R_L}{(R_L + r_c)C} & -\dfrac{1}{(R_L + r_c)C} \end{bmatrix}, \; B_k = \begin{bmatrix} \dfrac{d}{L} \\ 0 \end{bmatrix}, \; C_k = \begin{bmatrix} \dfrac{R_L r_c}{(R_L + r_c)} & \dfrac{R_L}{(R_L + r_c)} \end{bmatrix}. \tag{2.12}$$

If the time constant of the circuit is much larger than the period of switching, then the results will be acceptable. If the duty cycle is constant and $d = D$, the state equation (2.11)

will become linear. Regulating D is performed by using a controller, so in this way, one can regulate the voltage of the converter. In general, the equation (2.11) is nonlinear and it has to be linearized around the operating point (D).

At the equilibrium point, the system states are:

$$\dot{x}(t) = A_k x(t) + B_k v_i(t) = 0 \Rightarrow \quad \mathrm{X} = -A^{-1} B V_i = \begin{bmatrix} I_L \\ V_c \end{bmatrix} \tag{2.13}$$

with $A = A_k$ and $B = B_k$ for $d = D$. Using the classic linearization method, the variables consist of two parts: the first ones represent the fixed DC levels while the second ones are small variations around these DC levels, so the variables in the state equation (2.11) are now:

$$x(t) = X + \hat{x}(t),\ v_i(t) = V_i + \hat{v}_i(t),\ d(t) = D + \hat{d}(t),\ v_o(t) = V_o + \hat{v}_o(t) \tag{2.14}$$

where: V_o is a nominal value of DC output voltage, X is a nominal value of the state variable vector $x(t) = \begin{bmatrix} i_L(t) & v_c(t) \end{bmatrix}^T$, V_i is a nominal value of the input voltage, $\hat{x}(t), \hat{v}_i(t), \hat{d}(t), \hat{v}_o(t)$ are small variations of these values.

By substituting (2.14) in (2.11), taking into account (2.13) and neglecting the terms $\hat{d}(t)\hat{x}(t)$ and $\hat{d}(t)\hat{v}_i(t)$, one can get the following model:

$$\begin{aligned} \dot{\hat{x}}(t) &= A\hat{x}(t) + B\hat{v}_i(t) + [(A_1 - A_2)X + (B_1 - B_2)V_i]\hat{d}(t), \\ \dot{\hat{v}}_o(t) &= C\hat{x}(t) + (C_1 - C_2)X\hat{d}(t) \end{aligned} \tag{2.15}$$

where:

$$\begin{aligned} A &= A_1 D + A_2(1-D), \\ B &= B_1 D + B_2(1-D), \\ C &= C_1 D + C_2(1-D). \end{aligned} \tag{2.16}$$

The voltage drops in the switch r_m, diode r_d, as well as the parasitic resistance of the capacitor r_c can be neglected in the analysis of the circuit if the input voltage $v_i(t)$ is high enough. Then $P_1 = P_2 = -R_L r_L$ and:

$$A_1 = \begin{bmatrix} -\dfrac{r_L}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_L C} \end{bmatrix},\ B_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix},\ C_1 = \begin{bmatrix} 0 & 1 \end{bmatrix}, \tag{2.17}$$

$$A_2 = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_L C} \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \quad C_2 = \begin{bmatrix} 0 & 1 \end{bmatrix}, \tag{2.18}$$

$$A = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_L C} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix}, \quad C = \begin{bmatrix} 0 & 1 \end{bmatrix}. \tag{2.19}$$

In order to find the duty-cycle-to-output-voltage transfer function, the following equation is used [19]:

$$G_{\hat{v}_o \hat{d}}(s) = C(sI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_i] + (C_1 - C_2)X, \tag{2.20}$$

resulting in:

$$G_{\hat{v}_o \hat{d}}(s) = \frac{R_L D V_i}{R_L L C s^2 + (R_L C r_L + L)s + R_L + r_L}. \tag{2.21}$$

2.2.2 SMALL-SIGNAL STATE-SPACE MODEL

The continuous-time small-signal state-space model of an ideal DC-DC buck converter in the controllable canonical form can be easily obtained from Figure 2.8 if the sensed output voltage [27], [18]:

$$x_1(t) = \beta v_o(t) \Rightarrow \; v_o(t) = \frac{1}{\beta} x_1(t) \tag{2.22}$$

and its time derivate:

$$x_2(t) = \frac{dx_1(t)}{dt} = \beta \frac{dv_o(t)}{dt} = \frac{\beta}{C} i_c(t), \; i_c(t) = C \frac{dv_o(t)}{dt} \tag{2.23}$$

are chosen for the state coordinates. It is assumed that in the steady-state $u(t) = 0$ as the converter is driven to the desired operating point (D) by PWM. The derived model is simpler than one from the previous section but it can be efficiently used in the design of control u, which will be implemented to the converter via PWM.

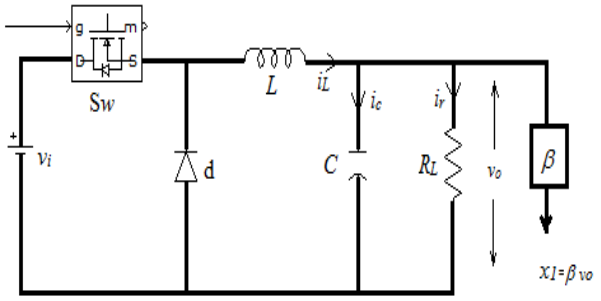


Figure 2.8 *The ideal DC-DC buck converter*

Using KCL gives:

$$i_c(t) = i_L(t) - i_R(t) \text{ , where : } i_R(t) = \frac{v_o(t)}{R_L} = \frac{x_1(t)}{\beta R_L} \tag{2.24}$$

whereas KVL yields:

$$v_i(t)u(t) - v_o(t) = L\frac{di_L(t)}{dt} = L\frac{d}{dt}(i_c(t) + i_R(t)) = L\left(\frac{di_c(t)}{dt} + \frac{di_R(t)}{dt}\right). \tag{2.25}$$

By substituting the equations (2.22) and (2.23) in (2.25) one can get:

$$v_i(t)u(t) - \frac{1}{\beta}x_1(t) = L\left(\frac{C}{\beta}\frac{dx_2(t)}{dt} + \frac{1}{\beta R_L}\frac{dx_1(t)}{dt}\right), \tag{2.26}$$

i.e.,:

$$\beta v_i(t)u(t) - x_1(t) = LC\frac{dx_2(t)}{dt} + \frac{L}{R_L}x_2(t). \tag{2.27}$$

Rearranging the equation (2.27), the state-space model is finally obtained:

$$\begin{aligned} \dot{x}_1(t) &= x_2(t), \\ \dot{x}_2(t) &= -\frac{1}{LC}x_1(t) - \frac{1}{R_L C}x_2(t) + \frac{\beta v_i}{LC}u(t) \end{aligned} \tag{2.28}$$

or in the matrix form:

$$\begin{aligned} \dot{x}(t) &= Ax(t) + Bu(t), \\ y(t) &= Cx(t) \end{aligned} \tag{2.29}$$

where: $A = \begin{bmatrix} 0 & 1 \\ -\frac{1}{LC} & -\frac{1}{R_L C} \end{bmatrix}$, $B = \begin{bmatrix} 0 \\ \frac{\beta v_i}{LC} \end{bmatrix}$ and $C = \begin{bmatrix} 1 & 0 \end{bmatrix}$. The transfer function of the DC-DC buck converter in the continuous-time domain is extracted from equation (2.29) by using:

$$W_{buck}(s) = C[sI - A]^{-1}B \tag{2.30}$$

in the form of:

$$W_{buck}(s)=\frac{Y(s)}{U(s)}=\frac{\frac{\beta V_i}{LC}}{s^2+\frac{1}{R_L C}s+\frac{1}{LC}}=\frac{\beta V_i}{R_L LCs^2+Ls+R_L}, \tag{2.31}$$

considering that at the operating point $v_i = V_i$.

Now, the input-output model of the buck converter in *z*-domain is got from (2.31) under the assumption that the control signal is constant during the sampling period T [27] in the next form:

$$\begin{aligned}
&y_k=\frac{z^{-1}B(z^{-1})}{A(z^{-1})}u_k,\\
&y_k=y(kT),\ u_k=u(kT),\\
&\mathrm{A}(z^{-1})=a_0+a_1z^{-1}+a_2z^{-2},\\
&a_0=1,\ a_1=-2e^{-aT}\cos(\omega_0 T)\ ,\ a_2=e^{-2aT},\\
&B(z^{-1})=b_0+b_1z^{-1},\\
&b_0=\frac{k}{a^2+\omega_0^2}(1-e^{-aT}\cos(\omega_0 T))\ ,\\
&b_1=\frac{k}{a^2+\omega_0^2}(e^{-2aT}-e^{-aT}\cos(\omega_0 T)),\\
&k=\frac{\beta v_i}{LC}\ ,\ a=\frac{1}{2R_L C}\ ,\ \omega_0=\sqrt{\frac{1}{LC}-\frac{1}{4R_L^2C^2}}.
\end{aligned} \tag{2.32}$$

2.3 DC-DC BOOST CONVERTER MODELS

This converter produces a higher average output voltage than the DC input voltage and it is depicted in Figure 2.9. Major applications of these converters are the regenerative braking of DC motors and the regulated DC power supply. The voltage across inductor L is added to the input supply voltage V_i to increase the voltage V_o above the input one and that is why it is called boost converter. Because of the nonlinearity nature of the DC-DC boost converters, which refers to the nonlinear components in its circuits (diode, an active switch), the operation of these converters varies by time. Therefore, it is very important to determine the appropriate mathematical model that will be used in the design of control for these converters. As in the case of the buck converter, the state-space average model will be derived first and then linearized around the operating point, finally resulting in the duty-cycle-to-output-voltage transfer function with the right-half-plane-zero [28], [29], [30]. The second small-signal state-space model in the controllable canonical form is introduced as well

assuming that the boost converter has been already driven to the desired operating point and that the control should ensure only the fine regulation around it.

2.3.1 STATE-SPACE AVERAGE MODEL

Let us consider the DC-DC boost converter with the switching period T_s and the duty cycle d as in Figure 2.9.

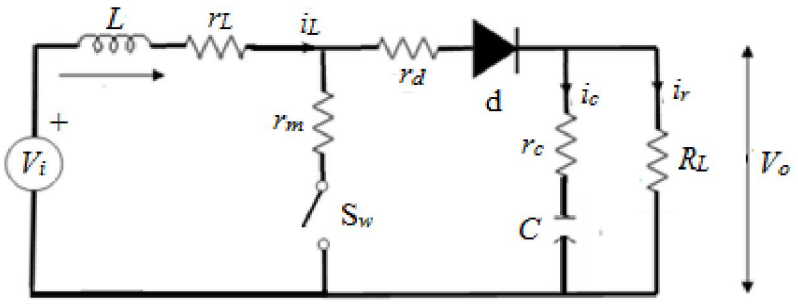


Figure 2.9 *The real DC-DC boost converter*

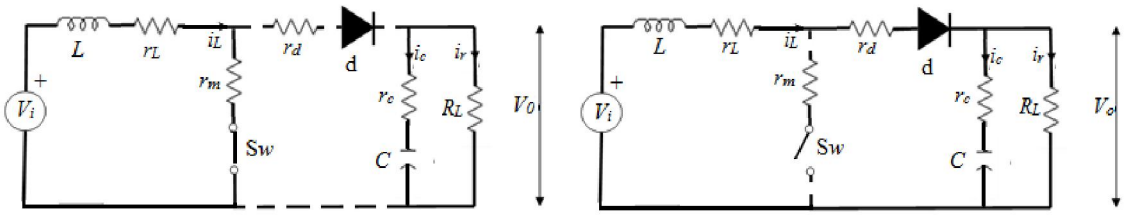


Figure 2.10 *The operational modes of DC-DC boost converter*

When the switch S_W is turned on, the current flows through L, r_L, r_m, S_W, storing energy in the inductor magnetic field as shown in Figure 2.10a. Thus, no current flows through diode d and the load current is supplied by the charge in the capacitor C. When S_W is turned off, as depicted in Figure 2.10b, the inductor L opposes any drop in the current by instantly reversing its electro-magnetic field. The inductor voltage is added to the source voltage boosting the output voltage in that way. Now the current flows from the source through L, r_L, r_d, d and the load R_L, and the capacitor is charged again. The voltage gain ratio is equal to:

$$\frac{V_o}{V_i} = \frac{1}{1-d}. \tag{2.33}$$

The signal waveforms of the DC-DC boost converter are shown in Figure 2.11.

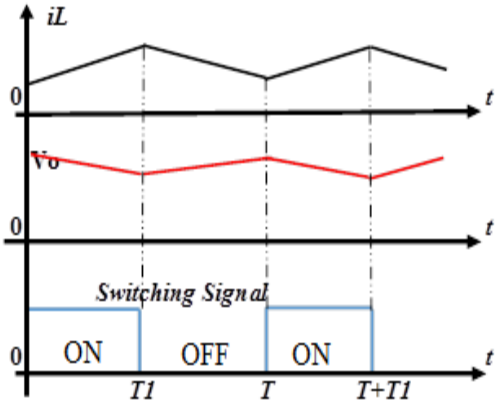


Figure 2.11 *The signal waveforms of DC-DC boost converter*

The state variable vector is also chosen as $x(t)=\begin{bmatrix} i_L(t) & v_c(t) \end{bmatrix}^T$. Based on the Figure 2.10a, the converter state-space model is given as:

$$\begin{aligned} \dot{x}(t) &= A_1 x(t) + B_1 v_i(t), \\ v_o(t) &= C_1 x(t) \end{aligned} \tag{2.34}$$

where:

$$A_1 = \begin{bmatrix} -\dfrac{r_L + r_m}{L} & 0 \\ 0 & -\dfrac{1}{(R_L + r_c)C} \end{bmatrix}, \; B_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, \; C_1 = \begin{bmatrix} 0 & \dfrac{R_L}{(R_L + r_c)} \end{bmatrix}. \tag{2.35}$$

When the switch is in the OFF position (see Figure 2.10b), the converter state-space model is:

$$\begin{aligned} \dot{x}(t) &= A_2 x(t) + B_2 v_i(t), \\ v_o(t) &= C_2 x(t) \end{aligned} \tag{2.36}$$

where:

$$A_2 = \begin{bmatrix} -\dfrac{R_L r_c + R_L r_L + r_L r_c + R_L r_d + r_d r_c}{L(R_L + r_c)} & -\dfrac{R_L}{(R_L + r_c)L} \\ \dfrac{R_L}{(R_L + r_c)C} & -\dfrac{1}{(R_L + r_c)C} \end{bmatrix}, \tag{2.37}$$

$$B_2 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, \; C_2 = \begin{bmatrix} \dfrac{R_L r_c}{(R_L + r_c)} & \dfrac{R_L}{(R_L + r_c)} \end{bmatrix}.$$

By combining the equations (2.34), (2.35), (2.36) and (2.37), the average state-space model of DC-DC boost converter is obtained as:

$$\begin{aligned} \dot{x}(t) &= A_k x(t) + B_k v_i(t), \\ v_o(t) &= C_k x(t) \end{aligned} \tag{2.38}$$

where: $A_k = A_1 d + A_2(1\text{-}d)$, $B_k = B_1 d + B_2(1\text{-}d)$, $C_k = C_1 d + C_2(1\text{-}d)$. By denoting $P_1 = -(R_L r_L + R_L r_m + r_c r_L + r_c r_m)$ and $P_2 = -(R_L r_c + R_L r_L + r_L r_c + R_L r_d + r_d r_c)$, A_k, B_k, and C_k are presented as:

$$A_k = \begin{bmatrix} \dfrac{P_1 d + P_2(1-d)}{(R_L + r_c)L} & -\dfrac{R_L(1-d)}{(R_L + r_c)L} \\ \dfrac{R_L(1-d)}{(R_L + r_c)L} & -\dfrac{1}{(R_L + r_c)C} \end{bmatrix},$$
$$B_k = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, \; C_k = \begin{bmatrix} \dfrac{R_L r_c(1-d)}{(R_L + r_c)} & \dfrac{R_L}{(R_L + r_c)} \end{bmatrix}. \tag{2.39}$$

Once more, the equation (2.38) with (2.39) is nonlinear as $A = A_k$ and $B = B_k$ depend on the duty cycle *d*. It has to be linearized around the operating point (*D*). At the equilibrium point, the system states are defined by (2.13). By substituting (2.14) in (2.38), taking into account (2.13) and neglecting the terms $\hat{d}(t)\hat{x}(t)$ and $\hat{d}(t)\hat{v}_i(t)$, one can get (2.15). Since the voltage drops on the parasitic resistances r_m, r_d and r_c are very small, (2.35), (2.37) and (2.39) can be rewritten in the following form:

$$A_1 = \begin{bmatrix} -\dfrac{r_L}{L} & 0 \\ 0 & -\dfrac{1}{R_L C} \end{bmatrix}, \; B_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, \; C_1 = \begin{bmatrix} 0 & 1 \end{bmatrix}, \tag{2.40}$$

$$A_2 = \begin{bmatrix} -\dfrac{r_L}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_L C} \end{bmatrix}, \; B_2 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, \; C_2 = \begin{bmatrix} 0 & 1 \end{bmatrix}, \tag{2.41}$$

$$A = \begin{bmatrix} -\dfrac{r_L}{L} & -\dfrac{1-D}{L} \\ \dfrac{1-D}{C} & -\dfrac{1}{R_L C} \end{bmatrix}, \; B = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, \; C = \begin{bmatrix} 0 & 1 \end{bmatrix}. \tag{2.42}$$

By using (2.20), the duty-cycle-to-output-voltage transfer function of DC-DC boost converter is calculated as:

$$G_{\hat{v}_o\hat{d}}(s)=\frac{-R_L L V_i}{\left(r_L+(1-D)^2R_L\right)}\frac{\left(s-\left((1-D)^2R_L-r_L\right)/L\right)}{\left(s^2R_LLC+(L+r_LCR_L)s+(1-D)^2R_L+r_L\right)} \tag{2.43}$$

and, obviously, it has a right-half-plane-zero causing the difficulties in controller design process.

2.3.2 SMALL-SIGNAL STATE-SPACE MODEL

The continuous-time small-signal state-space model of the ideal DC-DC boost converter in the controllable canonical form is obtained from Figure 2.11. The sensed output voltage (2.22) and its time derivate (2.23) are selected for the state coordinates here as well. Suppose that in the steady-state $u(t)=0$ as the converter is driven to the desired operating point (D) by PWM. The derived model is simpler than one from the previous section but it can be efficiently used in the design of control $u(t)$, which will be implemented to the converter via PWM [31], [18].

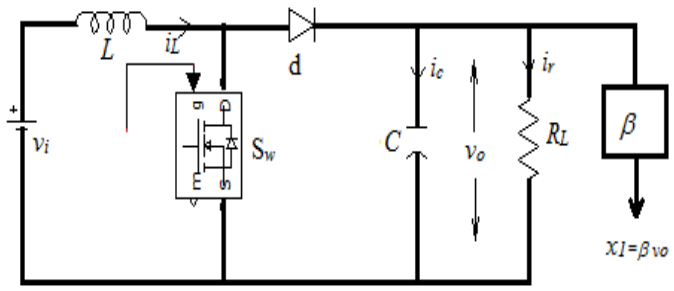


Figure 2.12 *The ideal DC-DC boost converter*

By using KCL and KVL, one can get:

$$i_c(t)=i_L(t)-i_R(t),\ \ i_R(t)=\frac{v_o(t)}{R_L},\ \ i_c(t)=C\frac{dv_o(t)}{dt}, \tag{2.44}$$

$$(v_i(t)-v_o(t))u(t)=L\frac{di_L(t)}{dt}=L\frac{d(i_c(t)+i_R(t))}{dt}=L\frac{d}{dt}\left(C\frac{dv_o(t)}{dt}+\frac{v_o(t)}{R_L}\right), \tag{2.45}$$

i.e., taking into account (2.22) and (2.23):

$$(v_i(t)-x_2(t))u(t)=L\left(\frac{C}{\beta}\frac{dx_2(t)}{dt}+\frac{1}{\beta R_L}\frac{dx_1(t)}{dt}\right). \tag{2.46}$$

By rearranging the equation (2.46), the state-space model is finally obtained:

$$\begin{aligned}\dot{x}_1(t) &= x_2(t),\\ \dot{x}_2(t) &= -\frac{1}{R_L C}x_2(t) + \frac{\beta(v_i(t) - x_1(t))}{LC}u.\end{aligned} \tag{2.47}$$

The linearized state-space continuous-time model of the DC-DC boost converter in the controllable canonical form around the operating point is given by (2.29) with:

$$A = \begin{bmatrix} 0 & 1 \\ 0 & -\frac{1}{R_L C} \end{bmatrix}, B = \begin{bmatrix} 0 \\ \frac{(V_i - V_o)}{LC} \end{bmatrix}, C = \begin{bmatrix} 1 & 0 \end{bmatrix} \tag{2.48}$$

and its transfer function is:

$$W_{Boost}(s) = \frac{Y(s)}{U(s)} = \frac{\frac{\beta(V_i - V_o)}{LC}}{s^2 + \frac{1}{R_L C}s}. \tag{2.49}$$

The input-output model of the buck converter in z-domain is:

$$\begin{aligned}
&y_k = \frac{z^{-1}B(z^{-1})}{A(z^{-1})}u_k,\\
&y_k = y(kT),\ u_k = u(kT),\\
&\mathrm{A}(z^{-1}) = a_0 + a_1 z^{-1} + a_2 z^{-2},\\
&a_0 = 1,\ a_1 = -(1 + e^{-aT}),\ a_2 = e^{-aT},\\
&B(z^{-1}) = b_0 + b_1 z^{-1},\\
&b_0 = \frac{b}{a}T + \frac{b}{a^2}(\mathrm{e}^{-aT}\text{-}1),\\
&b_1 = -\frac{b}{a}Te^{-aT} - 2\frac{b}{a^2}e^{-2aT} + 3\frac{b}{a^2}e^{-aT} - \frac{b}{a^2},\\
&a = -\frac{1}{R_L C},\ b = \frac{\beta(V_i - V_o)}{LC}.
\end{aligned} \tag{2.50}$$

3 BASIC PRINCIPLES OF SLIDING MODE CONTROL

The development of VSCS theory began with the analysis and synthesis of control in the continuous-time domain, therefore this chapter will contain a brief overview of continuous-time VSCS and SMC as a particular class of VSCS. The second part of this chapter will be dedicated to a DSMC, which can be easily implemented on DSPs and microcontrollers. The design of DSMC is usually based on the state-space system model. Unfortunately, the main limiting factor for the wider use of VSCS is reflected in the need to measure all the state coordinates of the plant under control. If this condition is not met, it is necessary to use an observer to estimate the state coordinates assuming that the plant under control is observable. This observer does not pose a particular problem in the digital realization of control processes although it contributes to its complexity. However, a series of logical questions arises, including the issue whether if it is possible that DSMC is designed if only the plant output is measurable, whether such an approach is complex for realization and whether, possibly, it is acceptable in the engineering practice. The positive answers to these questions are contained in numerous works and the basic principles of this approach to the synthesis of SMC, as well as a brief overview of the greatest contributions, will be revised in this chapter. The latter DSMC algorithms will be the basis for the design of a controller for DC-DC converters in this dissertation.

In the analysis of SMC, the terms such as "robust" and "invariant" are often used, so in order to indicate their good features and their full explanation, the simple definitions will be considered in the first place.

Definition 3.1: The system is said to be sensitive to the changes of its parameters if the sensitivity measure S' is different from zero. In a particular case if $S' = 0$, such system is said to be zero-sensitive. If the sensitivity measure S' is small, the system is called insensitive.

Definition 3.2 [32], [33]: The system is said to be robust if the system feature of interest remains within the limited range of significant but limited perturbations. The invariance conditions of SMC are given in [34].

3.1 CONTINUOUS-TIME SLIDING MODE CONTROL

In this chapter, only linear, continuous-time SMC will be considered while the interested reader can find the basic information on the nonlinear SMC in [35]. The special approach in analyzing and designing VSCS using geometric approach is shown in [36].

3.1.1 BASIC DEFINITIONS OF CONTINUOUS-TIME SMC

Let us consider a general model of a system first, given by:

$$\dot{\mathbf{x}}(t) = \mathbf{A}(\mathbf{x}(t)) + \mathbf{B}(\mathbf{x}(t))\mathbf{u}(t) \tag{3.1}$$

where $\mathbf{x}(t)$ is a vector of state coordinates with dimension n and $\mathbf{u}(t)$ is a vector of control inputs with dimension m.

Definition 3.3: A structure in VSCS is determined by the sign of the vector $\mathbf{s}(\mathbf{x}(t))$. The switching function $\mathbf{s}(\mathbf{x}(t))$ is m-dimensional and linear, i.e.:

$$\mathbf{s}(\mathbf{x}(t)) = \sum \mathbf{x}(t) \tag{3.2}$$

where:

$$\mathbf{s}(\mathbf{x}(t)) = \left[s_1(\mathbf{x}(t)) \;\; s_2(\mathbf{x}(t)) \;\cdots\; s_m(\mathbf{x}(t)) \right]^T, \tag{3.3}$$

$$\sum = \left[\boldsymbol{\sigma}_1 \quad \boldsymbol{\sigma}_2 \quad \cdots \quad \boldsymbol{\sigma}_\mathbf{m} \right]^\mathbf{T}, \tag{3.4}$$

$$s_i(\mathbf{x}(t)) = \boldsymbol{\sigma}_\mathbf{i}\mathbf{x}(t). \tag{3.5}$$

Each scalar value $s_i(\mathbf{x}(t))$ defines a surface:

$$s_i(\mathbf{x}(t)) = 0, \tag{3.6}$$

which is called a switching surface. As the switching function is linear, the surface (3.6) may be called a switching hyperplane or, in general, when the switching function is nonlinear, it is called a switching hypersurface.

Let $\mathbf{x_0} = \mathbf{x}(t_0)$ be the system initial state at the initial moment t_0 and let $s_i(\mathbf{x}(t)) = 0$ be the switching hypersurface containing $\mathbf{x}(t) = 0$.

Definition 3.4: If for any initial state $\mathbf{x_0}$, which is located at the switching hypersurface $s_i(\mathbf{x}(t_0)) = 0$, all the system states $\mathbf{x}(t)$ are always placed on the switching hypersurface $s_i(\mathbf{x}(t)) = 0$ for each $t > t_0$, then $\mathbf{x}(t)$ describes the sliding mode motion of the system.

Definition 3.5: If each point of switching hypersurface $s_i(\mathbf{x}(t)) = 0$ is a final point, i.e., if for each point of this switching hypersurface there are trajectories of the system that reach from its both sides, then this switching hypersurface is called a sliding hypersurface.

Definition 3.6: The condition under which the system state moves towards and fall onto the sliding hypersurface is known as a reaching condition.

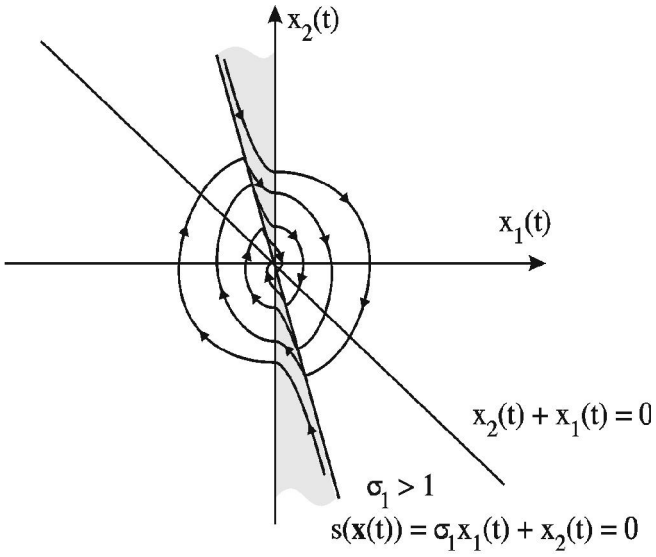


Figure 3.1 *Switching motion*

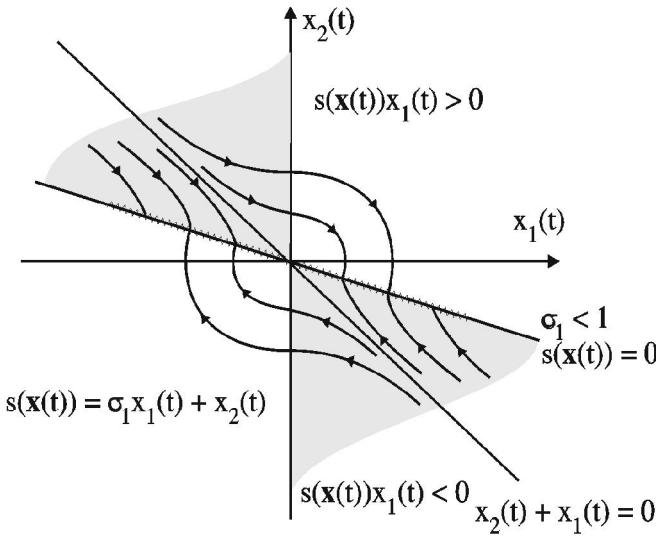


Figure 3.2 *Sliding mode motion*

Theorem 3.1: The n-order system with *m* control inputs (3.1) will have $2^m - 1$ switching hypersurfaces.

3.1.2 CONTINUOUS-TIME SMC DESIGN PROCEDURE

After defining the basic terms used in the analysis and synthesis of VSCS, SMC design procedure can be formulated as follows. For the system, represented by the state equation (3.1), one should find:

1) m switching functions given by $s_i(\mathbf{x}(t))$,
2) SMC

$$\mathbf{u}(\mathbf{x}(t))=\begin{cases}\mathbf{u}^{+}(\mathbf{x}(t)) & \text{for } \mathbf{s}(\mathbf{x}(t))>0\\ \mathbf{u}^{-}(\mathbf{x}(t)) & \text{for } \mathbf{s}(\mathbf{x}(t))\le 0\end{cases} \tag{3.7}$$

so that the reaching and existence condition of sliding mode is attained. This practically means:

1) to design the switching hypersurfaces $s_i(\mathbf{x}(t))=0$ so that they provide the desired system dynamics, which is of a lower order than the dynamics of the starting plant and
2) to design the SMC $\mathbf{u}(\mathbf{x}(t))$ so that the system state $\mathbf{x}(t)$ reaches the hypersurface in finite time and the system continues to move in sliding mode afterward.

Determining the equation of system motion in sliding mode is based on the fact that the differential equation, which describes the system dynamics, is not defined at the points where its right side has discontinuities or is not analytic since the existence and uniqueness of its solution are not guaranteed in those points. In order to analyze the system in sliding mode, it is necessary to determine the auxiliary equation of sliding mode using one of the continuity or regularization methods for linear systems with one input [37], [15], multivariable linear systems [15], systems linear to control (equivalent control method) [34], [38] and general case (Filipov`s method) [38], [39], [40]. Herein, the equivalent control method will be addressed in detail.

For all plants, which are linear in relation to the control and can be represented by (3.1), the equations of system motion in sliding mode can be obtained using the equivalent control method [34], [38]. The basic idea of this method is to calculate the equivalent control that will ensure that the system trajectory remains on $\mathbf{s}(\mathbf{x}(t))=0$. It is derived from $\dot{\mathbf{s}}(\mathbf{x}(t))=0$ as follows:

$$\dot{\mathbf{s}}(x(t))=\frac{\partial \mathbf{s}(\mathbf{x}(t))}{\partial \mathbf{x}(t)}\mathbf{A}(\mathbf{x}(t))+\frac{\partial \mathbf{s}(\mathbf{x}(t))}{\partial \mathbf{x}(t)}\mathbf{B}(\mathbf{x}(t))\mathbf{u}(t)=0, \tag{3.8}$$

so the equivalent control is:

$$\mathbf{u}_{eq}(t)) = -\left(\frac{\partial \mathbf{s}(\mathbf{x}(t))}{\partial \mathbf{x}(t)} \mathbf{B}(\mathbf{x}(t)) \right)^{-1} \frac{\partial \mathbf{s}(\mathbf{x}(t))}{\partial \mathbf{x}(t)} \mathbf{A}(\mathbf{x}(t)). \tag{3.9}$$

The necessary condition for calculating equivalent control is that the inversion matrix in (3.9) exists. By substituting $\mathbf{u}_{eq}(t)$ in (3.1), the equation that describes the system dynamics in sliding mode is obtained.

After selecting the appropriate sliding hypersurface and determining the equation of sliding mode motion, it is necessary to design the control that will provide sliding mode on the hypersurface (3.2). In the case of the single input system (a scalar control problem), the control is selected to satisfy the reaching and existence condition of sliding mode, which can be interpreted by Definition 3.5 in the following form:

$$s(\mathbf{x}(t))\dot{s}(\mathbf{x}(t)) < 0 \tag{3.10}$$

where: $s(\mathbf{x}(t)) = \sigma_1 x_1(t) + \cdots + \sigma_{n-1} x_{n-1}(t) + x_n(t)$.

This reaching and existence condition of sliding mode (3.10) is not directly applicable to the multi-input systems (a vector control problem). Its implementation requires an additional transformation of the system initial model (3.1) and (3.2). As the system has *m* control inputs, and therefore *m* switching functions, it has $2^m - 1$ switching hypersurfaces. The issue whether there will be a hypersurface that is also sliding one, in fact, depends on the design procedure of control. Different design approaches provide different switching schemes leading to the sliding mode motion in some regions. In the practical implementation of SMC, the following four switching schemes are used, which defines the way in which the sliding mode exists in the system.

Switching scheme of fixed order [34], [38], [15]. This switching scheme is carried out according to the predefined order in a correct predetermined hypersurface. Let *m* switching hypersurfaces be given by:

$$S_i = \left\{ \mathbf{x}(t) \middle| \mathbf{s}_i(\mathbf{x}(t)) = \boldsymbol{\sigma}_i \mathbf{x}(t) = 0 \right\}, \quad i = 1, \cdots, m \tag{3.11}$$

and let the phase point from the initial state $\mathbf{x}_0(t_0)$ reaches first the hypersurface S_1, whose dimension is $n-1$, after which it continues to move along it. Then the phase point can move towards hypersurface $S_{12} = (S_1 \cap S_2)$, whose dimension is $n-2$. In this way, the sliding moves towards hypersurfaces of lower dimensions until the so-called final hypersurface $S_k = (S_1 \cap S_2 \cap \cdots \cap S_m)$, which is the cross-section of all the hypersurfaces defined by (3.11)

and of *n-m* dimension. The switching scheme of fixed order can be shown in the following way:

$$\mathbf{x}_0(t_0) \to S_1 \to (S_1 \cap S_2) \to \left(S_1 \cap S_2 \cap S_3\right) \to \cdots \to S_k . \tag{3.12}$$

This switching scheme is obtained using the hierarchical control method. By implementing this method, it is possible to use the reaching and existence condition of sliding mode that applies to the scalar control problem. The switching scheme of fixed order is also called the hierarchical scheme. It contains a series of weaknesses and disadvantages, which are primarily reflected in a slow and bad transient process, difficulties in its application and high control values [15].

Decentralized switching scheme [41], [42], [43], [15]. This scheme occurs when a multivariable linear system with *m* control inputs is treated as a set of *m* independent scalar subsystems. Each of them has its own switching function and the associated sliding hypersurface. As a result, it is possible to use the reaching and existence condition of sliding mode for scalar control cases. Subsystems are interconnected, which can create difficulties in designing local control for each subsystem. This switching scheme provides good results in the control of large-scale systems.

Switching scheme of free order. Unlike the switching scheme of fixed order, in this scheme, the sliding hypersurface, in which the sliding mode motion is taking place, is not predefined, but follows the natural flow of the system trajectory. This scheme provides a quick response of the system with the excellent transient characteristics. SMC design is relatively easy and results in small control amplitudes, so there is no saturation in the system. The reaching law method [44], [15] gives the switching scheme just like this one.

Eventual switching scheme provides that the phase point reaches the eventual sliding hypersurface S_k from any initial position $\mathbf{x}_0(t_0)$. So, the sliding can but also cannot be performed on other sliding hypersurfaces. This switching scheme is achieved by a design approach based on the use of Lyapunov's function. Choosing the Lyapunov's function candidate in the next form:

$$V(\mathbf{x}(t)) = \mathbf{s}^T(\mathbf{x}(t))\mathbf{s}(\mathbf{x}(t)), \tag{3.13}$$

the reaching and existence condition of sliding mode on S_k is given by:

$$\dot{V}(\mathbf{x}(t)) < 0 \tag{3.14}$$

for $\mathbf{s}(\mathbf{x}(t)) \neq 0$. The final reaching time is determined by changing the condition (3.14) into:

$$\dot{V}(\mathbf{x}(t)) < -\gamma \tag{3.15}$$

where $\gamma > 0$ for $\mathbf{s}(\mathbf{x}(t)) \neq 0$.

3.1.3 PROPERTIES OF CONTINUOUS-TIME SLIDING MODE CONTROL

The motion in VSCS with SMC consists of three parts: the reaching mode, the sliding mode and the steady-state. Accordingly, the characteristics of SMC can be considered separately at each stage of the motion.

The reaching mode is often referred to as the fast-phase system motion since reaching of the sliding hypersurface by the phase point from any initial state takes place in a very short period of time. Before the reaching law control method [44], [15], the system dynamics in this mode was not defined in advance and the control is provided only by the establishment of the sliding mode.

As already mentioned, when the system is in the sliding mode, its dynamics is predefined and described by the lower-order model. Also, the system possesses robustness in relation to external disturbances and parameter variations. Due to the final switching time, which is the result of the presence of time delays, hysteresis, and unexpected low time constants in the system, the unwanted high-frequency oscillations occur in the sliding mode called chattering. The chattering can excite a high-frequency non-modeled system dynamics and thus leads to the undesirable system responses. One of the possible approaches to eliminate chattering consists of the application of saturated instead of relay control. This access is called the boundary layer approach [45], [46], [47], [48], [49].

The main disadvantage of this approach is the loss of invariance features and robustness in the boundary layer or the non-existence of sliding mode. On the other hand, the chattering elimination is complete. The second approach wherein the gain is weaken in the feedback regarding a digital implementation of SMC or so-called fading is considered in [50]. A new way to alleviate chattering is based on the implementation of the phase regulator [51]. By combining the linear PD regulator and the SMC with quasi-relay [52] or saturation control [53], it is possible to alleviate, i.e., eliminate chattering. From an adaptive point of view, the control procedure proposed in [54] is particularly interesting. The control procedure consists of two phases. The first phase of control ensures a quick reaching the hypersurface by the phase point using a large gain with a traditional SMC while the second stage of control provides a mitigation of chattering. The transition from one phase to the other is based on the prediction of switching function value. In practical implementations of SMC, the chattering

alleviation is made by commonly used low-pass filters, which are placed at the SMC output. A very effective method to eliminate chattering is achieved by using VSCS with the second order sliding mode. The basics of this approach were placed in [55], [56] and they were elaborated in [57]. Namely, the differential equation describing the switching function dynamics is of the second order, which results in the final integration of the relay control component $\text{sgn}(s(\mathbf{x}(t)))$, thus eliminating the chattering completely. The chattering in steady-state can be eliminated using a quasi-relay instead of the relay control, as well as by introducing an integral effect before [58], or after the SMC [59], [60], [61], [62], which also affects the accuracy of the system.

3.2 Digital Variable Structure Control Systems Based on State-Space Models

Nowadays, microprocessors, microcontrollers and DSP are necessary for the easy and fast realization of different control algorithms as well as to solve fundamental problems that occur in SMC arising from the need for the knowledge of all the state coordinates of the plant. In other words, the design of state observer is made simpler and efficient, as well as the design of control law. However, the digital realization of discrete-time SMC has gained some undesired effects, such as chattering and quantization noise as well as the loss of system invariance to the external disturbances. These problems are nowadays the main topics of many researches in the field of DSMC. In the following sections, a brief overview of the basic results of DSMC theory whose design is based on the use of plant models given in the state-space will be presented. The pioneered research in this field of SMC theory is [63], [64].

Until the eighties of the last century only two papers [65], [66] were published in the field of discrete-time VSCS. During these years the interest in this area has increased, which resulted in the publication of a large number of papers [67], [68], [69], [70], [71], [72]. The term zigzag motion has been introduced to describe the appearance of a real sliding mode in DSMC but the term QSM prevailed in further terminology [73]. Also, the term pseudo-sliding mode can be found today, which is introduced in [74], [75] [76]. The necessary and sufficient conditions of a QSM were analyzed in [72], [77], [78], [79] while the digital equivalent control, Lyapunov`s stability and discrete-time sliding mode were initially introduced in [80], [81] and later elaborated and exploited in many works [82], [83], [84] [85], [86]. The digital equivalent control was combined with three-way relay control ensuring that the system state moves towards a predefined sector [85]. Based on the so-called reaching

law method for continuous-time, a new approach has been developed to design DSMC in which the system dynamics is not defined only in the sliding mode but also in the reaching mode [86]. The application of adaptive mechanisms in the design of DSMC [87] shows that a motion that is approximately an ideal discrete sliding mode can be achieved under the conditions of parameters change. The control algorithm considered in [88], [89] is based on Gao`s reaching law method and the plant model obtained by using δ-transformation. With the increase of microcontroller speed, the design approaches based on this transformation has become more important. The proposed control algorithm is characterized by high system robustness in QSM resulting in the elimination of chattering as the unwanted phenomenon. A similar approach is used in [90] where the elimination of chattering is ensured by using time-variant sliding hypersurface with an additional integral action. There is no chattering in the case of a nominal plant controlled by the chattering-free continuous-time SMC with digital signal processing [91]. Using higher-order sliding modes, especially the second order sliding mode [92], [93], the system motion without chattering has been achieved. Since DSMC does not provide the system invariance to external disturbances, the system robustness is reached by the disturbance estimator. The most commonly used type of estimator is one-step-delayed estimator [94], [95], [96]. The works cited so far are only the most significant representatives of the beginnings in the development of DSMC theory. Let us consider a plant, whose continuous-time model is given in state-space by:

$$\dot{\mathbf{x}}(t) = (\mathbf{A}_n + \Delta\mathbf{A})\mathbf{x}(t) + (\mathbf{B}_n + \Delta\mathbf{B})\mathbf{u}(t) + \mathbf{D}_n\mathbf{f}(t) \tag{3.16}$$

where $\mathbf{x}(t) \in R^n$, $\mathbf{u}(t) \in R^m$ and $\mathbf{f}(t) \in R_l$ are a state coordinate vector, a control input vector and a vector external disturbance, respectively, $\mathbf{A}_n, \mathbf{B}_n$ and $\mathbf{D}_n$ are nominal matrices, whereas $\Delta\mathbf{A}$ and $\Delta\mathbf{B}$ denote parameter perturbations. The pair $(\mathbf{A}_n, \mathbf{B}_n)$ is controllable. The elements of the matrices $\mathbf{A}_n, \mathbf{B}_n$ and $\mathbf{D}_n$ are known as well as the upper and lower bounds of external disturbance $\mathbf{f}(t)$. In addition, $\Delta\mathbf{A}$, $\Delta\mathbf{B}$ as well as $\mathbf{f}(t)$ satisfy the matching conditions [34] that is $\operatorname{rank}\left[\mathbf{B}_n \middle| \Delta\mathbf{A} \middle| \Delta\mathbf{B} \middle| \mathbf{D}_n\right] = \operatorname{rank}\mathbf{B}$.

It is also assumed that the plant (3.16) is a minimum phase. The digital realization of SMC can be achieved by partial or complete discretization, which implies:

1) discretization of the switching function $\mathbf{s}_i(\mathbf{x}(kT))$, where $k \in N^+$, and T is a sampling period while the control signal remains continuous $\mathbf{u}_i = \mathbf{u}_i(t)$;

2) discretization of the control signal $\mathbf{u}_i = \mathbf{u}_i(kT)$, while the switching function remains continuous $\mathbf{s}_i = \mathbf{s}_i(t)$;

3) discretization of the control signal and the switching function:

i) with double sampling periods $\mathbf{u}_i = \mathbf{u}_i(kT)$ and $\mathbf{s}_i = \mathbf{s}_i(kT_1)$ or

ii) with one sampling period $\mathbf{u}_i = \mathbf{u}_i(kT)$ and $\mathbf{s}_i = \mathbf{s}_i(kT)$.

The realization of control is accomplished by using microprocessors with A/D and D/A converters as the zero order hold circuits. In this case, the discrete-time plant model of (3.16) is:

$$\mathbf{x}_{k+1} = \mathbf{\Phi}\mathbf{x}_k + \mathbf{\Gamma}\mathbf{u}_k + \mathbf{h}_k \tag{3.17}$$

where:

$$\begin{aligned}
&\mathbf{\Phi} = e^{AT}\ ,\ \mathbf{\Gamma} = \int_0^T e^{A\lambda}\mathbf{b}\,d\lambda\ ,\ \mathbf{h}_k = \mathbf{h}_k^A + \mathbf{h}_k^B + \mathbf{h}_k^f,\\
&\mathbf{h}_k^{\mathbf{A}} = \int_0^T e^{\mathbf{A}\lambda}\Delta\mathbf{A}((k+1)T-\lambda)\mathbf{x}((k+1)T-\lambda)d\lambda,\\
&\mathbf{h}_k^{\mathbf{B}} = \int_0^T e^{\mathbf{A}\lambda}\Delta\mathbf{B}((k+1)T-\lambda)\mathbf{x}((k+1)T-\lambda)d\lambda,\\
&\mathbf{h}_k^{\mathbf{f}} = \int_0^T e^{\mathbf{A}\lambda}\mathbf{D}\mathbf{f}((k+1)T-\lambda)d\lambda
\end{aligned} \tag{3.18}$$

and $\bullet_k = \bullet(kT)$. If the pair ($\mathbf{A}_n$, $\mathbf{B}_n$) is controllable then the pair ($\mathbf{\Phi}$, $\mathbf{\Gamma}$) is controllable for almost all sampling periods. As the outside disturbance cannot be sampled or since the zero-order hold circuit is not placed in the channel of disturbance, the matching conditions are no longer valid in the case of DSMC. One cannot talk about invariance to external disturbances but only of a certain robustness and accuracy of the system in $O(T), O(T^2)$ and $O(T^3)$ boundaries according to the applied control algorithm. For these reasons, the sampling period T should be chosen to be as low as possible in order to obtain a maximum accuracy during the action of disturbances. As a consequence of the discretization process, the unstable zeros can appear in the discrete-time model for a given sampling period T, although the initial plant model is the minimum phase.

3.2.1 Basic Definitions of the Digital Sliding Mode Control

As it has been already seen, SMC implementation using a microprocessor leads to the loss of the invariance properties since the matching conditions are not fulfilled and because of the appearance of quasi-sliding [73] or pseudo-sliding mode [76], which differs a lot from the ideal sliding mode that occurs in a continuous-time SMC. Thanks to the discretization

process in DSMC, a particular form of motion appears in sliding mode, which does not exist in continuous-time SMC systems. This type of sliding is known as an ideal digital sliding mode (DSM) and may be used to establish a system with formal parameters. Now, a QSM will be defined and the definitions of the phases of QSM motion will be described and introduced.

Definition 3.7 [86]: QSM is the motion under the following conditions:

1) once the system trajectories for the first time finally hit the switching hypersurface S_k (3.12), it will again cut off this hypersurface at subsequent time instants resulting in the so-called zigzag motion around S_k;
2) the size of each consecutive zigzag steps will not increase and therefore the trajectory will remain in a predetermined region.

This is a too restrictive definition since the motion in a predefined region can be achieved without the successive switchover of the switching hypersurface in every subsequent step, which is of great importance in the practical realization of DSMC because such motion does not produce chattering. Therefore, the following definition seems to better describe the QSM.

Definition 3.8 [90]: QSM is a motion that defines Δ-vicinity of the switching hypersurface S_k in advance, such that when the system trajectory once enters this region, it never leaves and $|x_k| \le \Delta$ is always valid where 2Δ indicates the width of the region around S_k.

The motion in the DSMC can be divided into three phases:

1) the reaching mode,
2) QSM and
3) the steady-state mode [97].

The following definitions consider each of these phases separately.

Definition 3.9: DSMC is in the reaching mode if the following is valid:

$$\operatorname{sgn}(s_{k+1}) = \operatorname{sgn}(s_k) \tag{3.19}$$

for every $k \in (0, K)$ and:

$$|s_{k+1}| < |s_k|. \tag{3.20}$$

Definition 3.10: DSMC is in the chattering mode if the following is valid:

$$\operatorname{sgn}(s_{k+1}) = -\operatorname{sgn}(s_k) \tag{3.21}$$

for every k.

3.2.2 DIGITAL SLIDING MODE CONTROL DESIGN PROCEDURE

Similar to the design of continuous-time SMC, DSMC design procedure takes place in two steps. In the first step, the choice of m switching functions $s=[s_{1k} \quad s_{2k} \quad \cdots \quad s_{mk}]$ is made, so the vector $\mathbf{u}_k$ of the DSMC can be selected later, which guarantees the reaching and the existence of QSM. The choice of switching functions determines the system dynamics in QSM, and such one approach is described in [2].

The reaching and existence condition of sliding mode in continuous-time SMC is given by expression (3.10), which can be obtained by using the direct method of Lyapunov and the Lyapunov's functions in the form of $V(\mathbf{x}(t))=s(\mathbf{x}(t))^2/2$ and therefore, this is a sufficient condition. In the earlier period of theoretical research in the field of continuous-time SMC, the local conditions were used to provide the reaching and existence conditions of sliding mode instead of (3.10):

$$\lim_{\mathbf{s}\to 0^+}\dot{\mathbf{s}}(\mathbf{x}(t))<0,\ \lim_{\mathbf{s}\to 0^-}\dot{\mathbf{s}}(\mathbf{x}(t))>0. \tag{3.22}$$

The conditions (3.10) and (3.22) can be written in the discrete-time domain as:

$$s_k\Delta s_k<0,\ \Delta \mathrm{s}_\mathrm{k}=s_{k+1}-s_k, \tag{3.23}$$

$$\lim_{s_k\to 0^+}\Delta s_k<0,\ \lim_{s_k\to 0^-}\Delta s_k>0, \tag{3.24}$$

respectively, and they represent the necessary conditions for the establishment of QSM [73] but they do not guarantee a stable QSM and, therefore, they are not sufficient conditions, as it is shown in [79]. As the choice of discrete Lyapunov's function is free, under the condition that the selected function is a positive definite for all x(t) except in origin, the different reaching and existence conditions of QSM can be derived. In [81], Lyapunov's function is selected as:

$$V(\mathbf{x}_k)=|s_k| \tag{3.25}$$

and the reaching and existence conditions of QSM will become:

$$|s_{k+1}|<|s_k|. \tag{3.26}$$

The latter conditions represent the necessary and sufficient conditions. Namely, the inequality (3.26) can be expressed through two inequalities [77]:

$$(s_{k+1}-s_k)\,\mathrm{sgn}(s_k)<0\ , \tag{3.27}$$

$$(s_{k+1}+s_k)\,\mathrm{sgn}(s_k)\geq 0, \tag{3.28}$$

where (3.27) gives the necessary conditions whereas (3.28) gives the sufficient conditions for the convergence, that is, the stability of QSM. If the conditions (3.27) and (3.28) are met for a particular system, the system trajectory converges to a particular region around $s_k = 0$ (3.27) and remains in it (3.28) changing at any future time instant the side of $s_k = 0$ and never increasing the distance from $s_k = 0$, so that QSM is established.

By choosing the Lyapunov's function in the following form:

$$V(\mathbf{x}_k) = s_k^2 \tag{3.29}$$

considering that:

$$\Delta V(\mathbf{x}_k) = V(\mathbf{x}_{k+1}) - V(\mathbf{x}_k) < 0, \tag{3.30}$$

one can get:

$$(s_{k+1} - s_k)(s_{k+1} + s_k) < 0. \tag{3.31}$$

By multiplying the latter inequality with $\mathrm{sgn}^2(s_k)$, one can get the same necessary and sufficient conditions for the reaching and existence of QSM such as (3.27) and (3.28). Starting from (3.29) and (3.30), the conditions of QSM are derived in [85] like:

$$2s_k \Delta s_k + \Delta s_k^2 < 0, \tag{3.32}$$

A convergent QSM also exists if the following inequality [79]*:*

$$\left| s_{k+1} s_k \right| < s_k^2 \tag{3.33}$$

is met. In proving the system stability with QSM control, it is possible to use theories of sequences and series [2].

3.2.3 PROPERTIES OF DIGITAL QUASI-SLIDING MODE CONTROL

As in the case of continuous-time SMC, the choice of DSMC algorithm also needs an appropriate switching scheme and *vice versa*. There are the switching schemes of fixed and free order, the decentralized and the eventual switching schemes, which have the same description as in the continuous-time domain.

The motion in DSMC systems is also driven through three phases: the reaching mode, QSM and the steady-state. The first phase is defined by the term (3.19) and if a boundary layer control is selected, the control signal does not change the sign and it does not differ from the reaching mode in the case of the continuous-time SMC. The QSM takes place in a particular sector, no matter whether the system trajectory changes the side of switching hypersurface at each sampling time or whether the motion takes place in this area without

changing the sign of switching functions. The best representative of the first motion is described in [86] whereas the second motion is achieved by applying the control laws given in [89], [90] that do not produce the chattering. The width of this sector around the switching hypersurface also depends on the applied control algorithm as well as on the fact whether the estimator of the disturbance is used or not, so QSM takes place in $O(T)$, $O(T^2)$ or $O(T^3)$ boundaries. The steady-state accuracy of DSMC is not often analyzed except in [97], [98], [99], [100]. This accuracy depends on the system and the parameters of switching function and it can be maximal of $O(T^3)$ order since the higher accuracy does not make sense in the real control applications. Namely, the quantization effect due to A/D conversion of signals as well as the presence of other disturbance sources significantly reduces the system steady-state accuracy.

In the end, it should be notified that due to the presence of various non-idealities, such as dead zones, hysteresis, time delays, neglected small time constants, a real sliding mode in continuous-time SMC does not differ much from QSM in DSMC systems. However, the ease and flexibility in the realization of DSMC using microprocessor technology enable the increasingly frequent use of DSMC in control systems.

3.3 DIGITAL VARIABLE STRUCTURE CONTROL BASED ON INPUT/OUTPUT MODELS

When the design procedure of the DSMC is based on the plant model in state-space, the knowledge of system state coordinates is mandatory, so if the coordinates are not available for measurements, a state observer is needed. The design and implementation of such observer can be difficult when the plant parameters change in time because the observer does not take into account these parameters variations. Another approach in designing DSMC is based on the input-output model of plant. Here, it is necessary to measure only the plant output taking into account that the control signal is generated by the microcontroller and is immediately available for the calculations. Such existing approaches can be divided into two categories. The first one deals with the design techniques based on the (generalized) minimum variance control ((G)MVC) [101]. Those methods use two types of control and are also known as (G)MVC with QSM. (G)MVC enables the realization of DSMC using only output measurements and takes the role of the equivalent control in DSMC. On the other hand, DSMC provides the system robustness with external disturbances and parameter perturbations. The second category represents DSMC, which use multiple sampling in the

system (known as feedback with fast output sampling) where the system state coordinates are estimated by sampling the plant output with a frequency much greater than the sampling frequency used in the control signal channel.

3.3.1 MINIMUM VARIANCE CONTROL

Let us consider a single-input-single-output (SISO) plant represented by the state-space model:

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{b}u(t) + \mathbf{d}\,f(t), \\ y(t) &= \mathbf{c}\mathbf{x}(t) \end{aligned} \tag{3.34}$$

where $\mathbf{x}(t) = \begin{bmatrix} x_1(t) & x_2(t) & \cdots & x_n(t) \end{bmatrix}^T \in R^n$ is a state vector, $u(t)$ is a plant input, $y(t) \in R$ is a plant output, $f(t) \in R$ is an external disturbance, $\mathbf{A} = \left[a_{ij} \right]_{nxn}$, $\mathbf{b} = \left[b_i \right]_{nx1}$, $\mathbf{c} = \left[\mathrm{c_j} \right]_{1xn}$, $\mathbf{d} = \left[d_i \right]_{nx1}$ are matrix and vectors of appropriate dimensions. The discrete-time state-space model of plant can be represented in the following form:

$$\begin{aligned} \mathbf{x}_{k+1} &= \mathbf{\Phi}\,\mathbf{x}_k + \boldsymbol{\gamma}\,u_k + \mathbf{h}_k, \\ y_k &= \mathbf{c}\,\mathbf{x}_k \end{aligned} \tag{3.35}$$

where:

$$\mathbf{\Phi} = e^{AT}\ ,\ \boldsymbol{\gamma} = \int_0^T e^{\mathbf{A}\lambda}\mathbf{b}\mathbf{d}\lambda\ ,\ \mathbf{h}_k = \int_0^T e^{\mathbf{A}T}\mathbf{d}f((k+1)T-\lambda)\mathbf{d}\lambda, \tag{3.36}$$

$\mathbf{x}_k = [x_{1k} \quad x_{2k} \quad \cdots \quad x_{nk}]^T$. If the external disturbance $f(t)$ is a limited function of time, or if there is such a constant $F < \infty$, so that $|f(t)| < F$, it follows that the disturbance $\mathbf{h_k}$ has $O(T)$ accuracy, i.e. :

$$\mathbf{h}_k = \int_0^T e^{\mathbf{A}\lambda}\mathbf{d}f((k+1)T-\lambda)d\lambda = O(T). \tag{3.37}$$

On the basis of (3.35), the plant model in z-domain is obtained in the following form:

$$y_k = \frac{z^{-1}B(z^{-1})}{A(z^{-1})}u_k + \frac{z^{-1}\mathbf{D}(z^{-1})}{A(z^{-1})}\mathbf{h}_k \tag{3.38}$$

where:

$$A(z^{-1}) = z^{-n}\det(z\mathbf{I} - \mathbf{\Phi}), \tag{3.39}$$

$$B(z^{-1}) = z^{-n+1}\mathbf{c}\,[adj(z\mathbf{I} - \mathbf{\Phi})\,\boldsymbol{\gamma}], \tag{3.40}$$

$$\mathbf{D}(z^{-1}) = z^{-n+1}\mathbf{c}\,[adj(z\mathbf{I} - \mathbf{\Phi})\,]. \tag{3.41}$$

z^{-1} is a unit delay, $z = e^{pT}$ where p is a complex variable.

The control design goal is to find such control law that will provide the minimum variance of output variable:

$$s_{k+1} = C(z^{-1})(y_{k+1} - r_{k+1}), \tag{3.42}$$

or $s_{k+1} = 0$ in the deterministic case where $C(z^{-1})$ is a stable polynomial or in other words, its roots lie inside the unit disc in the z- plane. r_{k+1} is a reference input at $(k+1)$-th time instant. The plant output in steady-state (when $k \to \infty$ or $z \to 1$) is defined by:

$$y_\infty = r_\infty + \frac{s_\infty}{C(1)}. \tag{3.43}$$

The accuracy of system output will depend on the accuracy of s_k. Decreasing this variable will reduce the tracking error. As one can see later, s_k represents the switching function in DSMC whereas $s_k = 0$ represents the equation of sliding hypersurface. If it is assumed that the reference input signal (r_k) is known in advance, MVC can be written as:

$$u_k = -\frac{F(z^{-1})y_k - C(z^{-1})\, r_{k+1}}{E(z^{-1})B(z^{-1})}. \tag{3.44}$$

The polynomials $E(z^{-1})$ and $F(z^{-1})$ are the solutions of the Diophantine equation:

$$E(z^{-1})A(z^{-1}) + z^{-1}F(z^{-1}) = C(z^{-1}). \tag{3.45}$$

Substituting (3.44) in (3.38) gives the following:

$$(E(z^{-1})A(z^{-1}) + z^{-1}F(z^{-1}))y_{k+1} = C(z^{-1})\, r_{k+1} + E(z^{-1})\mathbf{D}(z^{-1})\mathbf{h}_k \tag{3.46}$$

and taking in the consideration (3.42) and (3.45), (3.46) finally becomes:

$$s_{k+1} = C(z^{-1})(y_{k+1} - r_{k+1}) = E(z^{-1})\mathbf{D}(z^{-1})\mathbf{h}_k = O(T). \tag{3.47}$$

s_k possesses the $O(T)$ accuracy inherited from the accuracy of disturbance $\mathbf{h}_k$ (3.43) the system accuracy in steady-state is determined by $\frac{O(T)}{C(1)}$.

3.3.2 Generalized Minimum Variance Control

The design of DSMC based on the MVC has disadvantages, which originate from the plant zero dynamics cancellation. Therefore, the proposed concept cannot be applied to the non-minimum and/or to the so-called weak non-minimum phase systems. In those cases, the problem of DSMC design is very difficult theoretically and practically. Even in the case

when the zero cancellation is allowed (the minimum phase plants), the control signal saturation may occur, as for low sampling period *T*, the control signal takes on high values.

The efficient overcoming of this problem has been performed by using GMVC in DSMC design. GMVC is similar to MVC since it also enables the use of control techniques based on the theory of VSCS where only the plant output (or the error signal) is available for measurement, takes the role of digital equivalent control and, in addition, efficiently resolves the problem of saturation and control of the non-minimum phase plant. DSMC, on the other hand, provides greater system robustness with external disturbances and parameter perturbations.

In order to design GMVC, the SISO plant model (3.38) will be considered again. The design goal is to find the control that will provide a minimum variation of the variable defined by:

$$s_{k+1} = C(z^{-1})(y_{k+1} - r_{k+1}) + Q(z^{-1})u_k \tag{3.48}$$

or its zero value in a deterministic case where the polynomial $C(z^{-1})$ has roots within the unit disc in the *z*-plane and the polynomial $Q(z^{-1})$ should meet the following equality:

$$Q(1) = 0 \tag{3.49}$$

in the steady-state, i.e., when $k \to \infty$ or $z \to 1$. Note that the variable s_k also represents the switching function of DSMC. The control law meeting these requirements is the GMVC defined by:

$$u_k = -\frac{F(z^{-1})y_k - C(z^{-1})r_{k+1}}{E(z^{-1})B(z^{-1}) + Q(z^{-1})} \tag{3.50}$$

where the polynomials $E(z^{-1})$ and $F(z^{-1})$ are obtained from (3.45). As $E(z^{-1})B(z^{-1}) + Q(z^{-1})$ is in the denominator of (3.50), it is therefore possible to avoid the cancellation of the unstable plant zero dynamics.

Implementing of (3.50) into the plant model (3.38) gives:

$$\begin{aligned} &B(z^{-1})(E(z^{-1})A(z^{-1}) + z^{-1}F(z^{-1}))y_k + A(z^{-1})Q(z^{-1})y_k = \\ &= z^{-1}C(z^{-1})r_{k+1} + z^{-1}(E(z^{-1})B(z^{-1}) + Q(z^{-1}))\mathbf{D}(z^{-1})\mathbf{h}_k. \end{aligned} \tag{3.51}$$

By substituting $A(z^{-1})y_{k+1}$ from (3.38) in (3.51), taking into account (3.45) and dividing by $B(z^{-1})$, one can finally get:

$$s_{k+1} = C(z^{-1})(y_{k+1} - r_{k+1}) + Q(z^{-1})u_k = E(z^{-1})\mathbf{D}(z^{-1})\mathbf{h}_k = O(T). \tag{3.52}$$

Therefore, by using GMVC (3.50) in the control of the plant (3.38), one can achieve the same accuracy of the variable s_k as well as in the case of the application of MVC with the difference that GMVC allows the control of the non-minimum phase plants thanks to the existence of polynomial $E(z^{-1})B(z^{-1})+Q(z^{-1})$ in the denominator of the control law (3.50). At the same time, it provides the ability to avoid the control signal saturation when the sampling period T is too low and when the control plant is not necessarily non-minim phase.

MVC can be treated as an analog to digital equivalent control in DSMC based on the state-space models. Unfortunately, there is no direct correlation between these control concepts and therefore, it is not possible to make an arbitrary choice of system dynamics in QSM. In the case of GMVC, this link exists. In other words, it is possible to define the system dynamics in QSM by using the digital equivalent control method and then to map the same dynamics to GMVC application by selecting $C(z^{-1})$, $Q(z^{-1})$, $E(z^{-1})$ and $F(z^{-1})$ polynomials. That will guarantee the similar, if not the same, system dynamics with QSM control techniques, which is based on the input-output model.

3.3.3 Digital Sliding Mode Control Based on Minimum Variance Control

Digital sliding mode control based on minimum variance control (DSMCMVC) represents a modification of MVC, which is enhanced by adding sliding mode component in the form of the relay control law, filtered through the digital integrator [1], [102]. As it has been mentioned earlier, MVC has the similar role as the digital equivalent control with DSMC based on the state-space model. The case with *a priori* known reference input signal is considered herein. Then, DSMCMVC has the following form:

$$u_k = -\frac{1}{E(z^{-1})B(z^{-1})}\left(F(z^{-1})y_k - C(z^{-1})r_{k+1} + \frac{\alpha T}{1-z^{-1}}\operatorname{sgn}(s_k)\right) \tag{3.53}$$

where s_k defined by (3.42) represents the so-called switching function of DSMCMVC, where the polynomials $E(z^{-1})$ and $F(z^{-1})$ are the solutions of Diophantine equation (3.45). The implementation of (3.53) in (3.38) considering (3.42) and (3.45) gives:

$$s_{k+1} = C(z^{-1})(y_{k+1} - r_{k+1}) = -\frac{\alpha T}{1-z^{-1}}\operatorname{sgn}(s_k) + E(z^{-1})\mathbf{D}(z^{-1})\mathbf{h}_k\,, \tag{3.54}$$

i.e.:

$$s_{k+1} = s_k - \alpha T \operatorname{sgn}(s_k) + E(z^{-1})\mathbf{D}(z^{-1})(\mathbf{h}_k - \mathbf{h}_{k-1}) \tag{3.55}$$

and $\mathbf{h}_k - \mathbf{h}_{k-1} = O(T^2)$ is valid. The equation (3.55) defines the switching function dynamics with the control law (3.53). The parameter α determining QSM in Δ-vicinity of the switching function $s_{k+1} = 0$ should be selected according to the following Theorem.

Theorem 3.2: Consider the discrete-time control system described by (3.38) and (3.53) with the switching function defined by (3.42) and its dynamics by (3.55). If the parameter α is chosen to meet the following inequality:

$$\alpha T > \max \left| E(z^{-1})\mathbf{D}(z^{-1})(\mathbf{h}_k - \mathbf{h}_{k-1}) \right| = O(T^2), \tag{3.56}$$

there is a natural number $K_0 = K_0(s_0)$, so that for every $k \geq K_0$ there exists QSM in $S_1(T^2)$ region defined by:

$$S_1(T^2) = \{ s_k : |s_k| < \alpha T + \max \left| E(z^{-1})\mathbf{D}(z^{-1})(\mathbf{h}_k - \mathbf{h}_{k-1}) \right| = O(T^2) \} \tag{3.57}$$

where $\alpha = O(T)$.

The proof of the Theorem 3.2 is elaborated in [2].

Theorem 3.3: The system described by (3.38) and (3.53) is stable if and only if:

1) there exists QSM, i.e. (3.56) is fulfilled for every k, and
2) the polynomial $C(z^{-1})$ has all roots inside the unit disc in *z*-plane.

Proof: If α is chosen in accordance with (3.56), then there is QSM in $S_1(T^2)$ region. Based on (3.38), it is concluded that:

$$y_k = r_k + \frac{s_k}{C(z^{-1})} \tag{3.58}$$

and therefore, y_k will tend to the reference input signal r_k if and only if the polynomial $C(z^{-1})$ is stable.

3.3.4 Digital Sliding Mode Control Based on Generalized Minimum Variance Control

Similar to the control discussed in the previous section, digital sliding mode control based on generalized minimum variance control (DSMCGMVC) is obtained when the SMC component is introduced into GMVC in the form of the relay control law, filtered through the digital integrator [1], [102], [103]. In other words, with this combination, DSMC with QSM, which can deal with non-minimum phase plants and avoid the saturation of control input signal, is realized. The presence of digital integrator alleviates the chattering phenomenon

providing relatively smooth control input signal. As it has been mentioned before, GMVC replaces digital equivalent control whereas s_k becomes the switching function of DSMC.

Under the assumption that the reference input signal is known in advance, DSMCGMVC law can be written as:

$$u_k = -\frac{F(z^{-1})y_k - C(z^{-1})r_{k+1} + \frac{\alpha T}{1-z^{-1}}\operatorname{sgn}(s_k)}{E(z^{-1})B(z^{-1}) + Q(z^{-1})} \tag{3.59}$$

where s_k defined by (3.48) is the so-called switching function whereas the polynomials $E(z^{-1})$ and $F(z^{-1})$ are the solutions of Diophantine equation (3.45) and the polynomial $Q(z^{-1})$ meets (3.49). By substituting (3.59) in (3.38), taking into account (3.45) and (3.48), one can get:

$$s_{k+1} = C(z^{-1})(y_{k+1} - r_{k+1}) + Q(z^{-1})u_k = -\frac{\alpha T}{1-z^{-1}}\operatorname{sgn}(s_k) + E(z^{-1})\mathbf{D}(z^{-1})\mathbf{h}_k, \tag{3.60}$$

i.e.:

$$s_{k+1} = s_k - \alpha T \operatorname{sgn}(s_k) + E(z^{-1})\mathbf{D}(z^{-1})(\mathbf{h}_k - \mathbf{h}_{k-1}). \tag{3.61}$$

The expression (3.61) determines the switching function dynamics with the control algorithm (3.59) and it is identical to (3.55). The system stability with the proposed control law is attained if the conditions of the following theorem are fulfilled.

Theorem 3.4: The system defined by (3.38) and (3.59) is stable if and only if

1) α is chosen in accordance with the Theorem 3.2 and
2) all roots of equation $B(z^{-1})C(z^{-1}) + A(z^{-1})Q(z^{-1}) = 0$ should be inside the unit disc in the z-plane, and the pairs ($B(z^{-1})$, $Q(z^{-1})$), ($C(z^{-1})$, $A(z^{-1})$) and ($C(z^{-1})$, $Q(z^{-1})$) should not have common zeroes outside this disk.

The system steady-state accuracy will be in $O(T^2)$ boundary.

The proof of this theorem can be found in [2].

4 DC-DC CONVERTERS WITH SLIDING MODE CONTROL

SMC belongs to the class of nonlinear control known as variable structure control (VSC) [38], [15], [104]. It forces system state to slide along predefined hypersurface providing system robustness with parameter variations and external disturbances, even invariance [105], for systems satisfying matching conditions. These SMC properties recommend it for DC-DC converting applications under the load and input voltage variations. However, SMC operates at varying switching frequency causing inductor and transformer core losses as well as producing some EMI noise issues. The first sliding mode controllers for power converters were hysteresis-modulation based. In order to make SMC more applicable to DC-DC converters, its switching frequency should be limited, so that it operates as an approximation of ideal sliding mode controller. This results in a reduction of system robustness. The limitation is done by changing the modulation method from hysteresis-modulation to PWM, known as duty cycle control as well [106]. It has been proven [107], that the system dynamics with sliding mode controller is equivalent to the system dynamics with PWM controller, i.e., that sliding equivalent control [34], [38], u_{eq} is equal to the duty cycle control signal d.

The implementation of PWM techniques in control of DC-DC boost converter operating in CCM may cause the appearance of right-half-plane-zero (RHPZ) in its duty-cycle-to-output-voltage transfer function, obtained on the basis of the state-space average model of converter [108], [19]. This makes the design of boost converter voltage controller more difficult and limits the system bandwidth [20]. In recent years, several DC-DC converters with PWM based SMC have been developed. The use of sliding mode strategy in DC-DC buck converters is introduced in [109]. The implementation of SMC to all the basic types of DC-DC converters and the introduction of the equivalent control method in order to get SMC with a constant frequency is proposed in [110]. Many papers have later discussed the improvement and the robustness of SMC for buck converters such as [111], [112], [113], [114], [115]. A unified approach to the design of PWM based sliding mode (SM) voltage controller for three basic converters (buck, boost and buck-boost) is demonstrated in [18]. A nonlinear sliding mode controller design of DC-DC converter based on the extended linearization technique is discussed in [116]. Fuzzy SMC is proposed and also implemented in the design of DC-DC buck converter [117]. The control of two DC-DC buck converters connected in parallel by using integral SMC algorithms is considered in [118]. The fixed frequency SM current controller for boost converter is presented in [119]. In order to increase

the steady-state accuracy of the boost converter, an additional double-integral term of the controlled variables is introduced in the sliding hypersurface equation of indirect SM controllers [120]. Based on the similar state-space model of boost converter as in the previous works [18], [119], [120], the proportional plus integral (PI) type of switching (sliding) function is introduced in [121], to cope with the load variations. Moreover, the switching function parameter is tuned as per a load, resulting in adaptive, unlike conventional SMC. The fast terminal SMC, having a nonlinear switching function to guarantee finite-time convergence to the sliding hypersurface, is implemented in the output voltage control of boost converter [122]. The proposed control scheme combines finite-time and exponent convergent properties in the design of switching function in order to improve the convergence performance if the system state is far from the equilibrium point.

Boost converters are widely used as power stages in the renewable energy resources such as photovoltaic (PV) systems. The connection of these systems to the main dc bus via power converters enables high maximum power point tracking (MPPT). Thanks to the fact that the input impedance of boost converter can be tuned by the duty cycle, i.e., it can be considered as an adjustable loss-free resistor (LFR), the operating point of PV system can be changed in order to maximize the output power. An overview of MPPT techniques for PV power systems is presented in [123]. Many MPPT methods do not take into account the system uncertainties and are not robust to them. To cope with parameter perturbation, MPPT algorithms with SMC are proposed for eliminating the perturbation effects [124], [125]. In [125] maximum power point curve is approximated, taking into account not only the voltage and current on the PV panel but also the temperature. This linear approximation is used then to form a switching function of SM controller. The impedance matching can be also obtained by the cascade connection of two boost converters driven by SM controllers based on LFR concept [126].

The fixed switching frequency of SM control can be attained by using discrete-time SM controllers [86], [90], [63]. However, the discretization process of SMC causes the quasi-sliding motion [73], in the vicinity of sliding hypersurface and produces an undesirable chattering. The latter phenomenon is also present in converters with PWM based continuous-time SMC techniques. It can be suppressed by using the boundary layer approach [125], the chattering-free [122], [124], control methods or, recently, the tensor product model [127], for sliding hypersurface design [105].

One of the first approaches in the design of discrete-time SM like controller is considered in [21], for the control of DC-DC buck converter. The control algorithm is implemented as a fuzzy logic controller with sliding mode like characteristics. DSMC, applicable for different DC-DC converters, is introduced in [128]. Discrete-time SM controllers for boost converter [22], [129] can be designed based on its state-space average model, which is the non-minimum phase system if the output voltage is directly controlled. Therefore, the indirect method is used that controls the inductor current, whose reference signal is selected such that the desired output voltage is obtained. The choice of the inductor current, as an output, results in the minimum phase system but the problem of the output voltage convergence to its reference signal arises. In [22], the design of discrete-time SMC with reference model is presented. The cascade regulation scheme consisting of the inner inductor current loop with discrete-time SMC and the outer one being composed of a discrete-time PI controller for output voltage regulation is considered in [129]. Another approach to modeling of boost converter [130], [131] using discrete Lagrange-Euler equations results also in the non-minimum phase system. The main difficulty to stabilize the unstable inductor current variable and to provide that output voltage tracks the desired reference signal is addressed in these papers. Due to the unstable zero dynamics of the state-space average model, the implementation of discrete-time SMC using stable system center [132] in direct control of the output voltage may be considered as a promising solution to this problem.

All the previous control design techniques are based on the state-space model representation of converters and therefore, the measuring of the inductor current is mandatory. Conventional current sensing methods, such as a resistor as a sensor element, suffer from significant power losses, especially when the current is high. That is why the loss-less current sensing methods are used [133] whereas input-output control laws are more than preferable. In this dissertation, a DSMC is presented that is designed by using the input-output model of buck and boost converters in the form of discrete-time transfer functions, which eliminates the need for the additional current sensor. The proposed control represents the combination of (generalized) minimum variance (G)MV and DSMC techniques [1], [2]. GMVC is suggested herein to cope with RHPZ of the duty-cycle-to-output-voltage transfer function and to enable the controller design based only on converter output voltage measuring. In order to alleviate chattering and achieve better converter accuracy, the discrete-time SMC component is filtered through discrete-time integrator [1].

In [134], an approach to the microcontroller-based realization of DC-DC boost converter with QSM control is presented. The theoretical background of the proposed control laws for the buck and boost converters are given in [31], [135], [136] based on contributions presented in [2] and partially in [1]. However, due to parameter variations, some additional stability issues are considered in the following chapter extending the theoretical results in that way. The advantage of using proposed DSMC over the continuous-time PID based SMC for DC-DC boost converter is elaborated in [136], [137]. This controller is also implemented in the control of DC-DC buck-boost converter and the results are shown in [138]. Similar DSM controller is implemented in the voltage control of buck converter [27]. As the buck converter represents a minimum phase system, DSMC is combined with MVC. As mentioned before, GMVC represents the equivalent control analog in DSMC techniques based on the input-output plant models. A novel DC-DC boost converter driven by GMVC with one-step delayed disturbance estimator is analyzed in [139].

Traditionally, DSPs are used to implement controllers for power converters. In recent years, some research efforts have been dedicated to designing of low-cost solutions for the voltage control of converter. In [3], the sliding-mode hysteretic control algorithm based on the state-space model is realized by low-cost memory hardware. The sliding hypersurface is derived in advance and stored in memory lookup table whose output drives a converter power switch. The continuous-time SMC designed by using state-space average model is digitally implemented using a low-cost dsPIC30F4013 microcontroller with small computing power [4]. The selection of sliding hypersurface provides the current mode controller making the inductor current a function of the output voltage.

In the chapter that follows, the realization of the suggested DSMC for buck and boost converters on the widely used ATmega8 microcontroller will be demonstrated. It is shown that these control algorithms are simple enough to be easily implemented on standard 8-bit microcontrollers but at the expense of little lower accuracy and slower dynamical response. Moreover, the suggested converter realizations give satisfactory experimental results indicating that better results can be expected if the DSP is used.

5 DESIGN OF DIGITAL SLIDING MODE CONTROL FOR DC-DC CONVERTERS

In this chapter, a design of DSMC for the both topologies of DC-DC converters (buck and boost) is considered.

5.1 DC-DC BUCK CONVERTER WITH DIGITAL SLIDING MODE CONTROL

As mentioned before, the major function of DC-DC buck converter is to transfer an unregulated input DC voltage to a lower regulated output DC voltage, which is invariant to external perturbation and parameter variations. To evaluate the performance of the control technique suggested in this dissertation, the complete model of DC-DC buck converter with DSMC will be digitally simulated and the obtained results will be compared with the experimental ones derived from the laboratory developed prototype.

5.1.1 DIGITAL SLIDING MODE CONTROL DESIGN PROCEDURE

Controlling the output voltage of DC-DC buck converter is built upon the algorithm that is the result of mixing DSMC with MVC technique using input-output measurements only. The starting point is the design conditions:

$$L > L_B, \text{ where : } L_B = \frac{(1-D)R_L}{2f_{pwm}} \tag{5.1}$$

and

$$C > C_{\min}, \text{ where: } C_{\min} = \frac{(1-D)V_o}{8V_r L f_{pwm}^2}. \tag{5.2}$$

The schematic diagram of DC-DC buck converter with DSMC is presented in Figure 5.1. The suggested structure only measures the sensed output voltage, and it is different from most existing solutions based on measurements of voltage error and either its time-derivative or capacitor current [106]. DSMC signal is compared with variable ramp signal providing a PWM signal *u,* which drives the power switch S_w. As it is well known, the average dynamics of system with SMC is equivalent to the average dynamics of PWM controlled system [107] implying that the equivalent control signal in sliding mode u_{eq} [34] corresponds to the duty cycle control signal *d* of PWM controller. For DSMC design purposes, the state-space continuous-time model of DC-DC buck converter in the controllable canonical form (2.29) with the state variables $x_1(t) = v_o(t)$ and $x_2(t) = \dot{x}_1(t) = \left(i_c(t)\right)/C$ is used:

$$\dot{\mathbf{x}}(t)=\begin{bmatrix}0 & 1\\ -\dfrac{1}{LC} & -\dfrac{1}{R_L C}\end{bmatrix}\mathbf{x}(t)+\begin{bmatrix}0\\ \dfrac{\beta V_i}{LC}\end{bmatrix}u(t),$$
$$y(t)=\begin{bmatrix}\beta & 0\end{bmatrix}\mathbf{x}(t) \tag{5.3}$$

where: L, C, R_L, V_i and β are the inductance, capacitance, load resistance, nominal input voltage and sensor gain, respectively. V_{ref}, $v_i(t)$ and $v_o(t)$ are the reference, output and output voltage, respectively, and $u(t)$ is 0 or 1, representing the switching state of the power switch. $u(t)$ is equal to PWM output obtained on the basis of the DSM controller output.

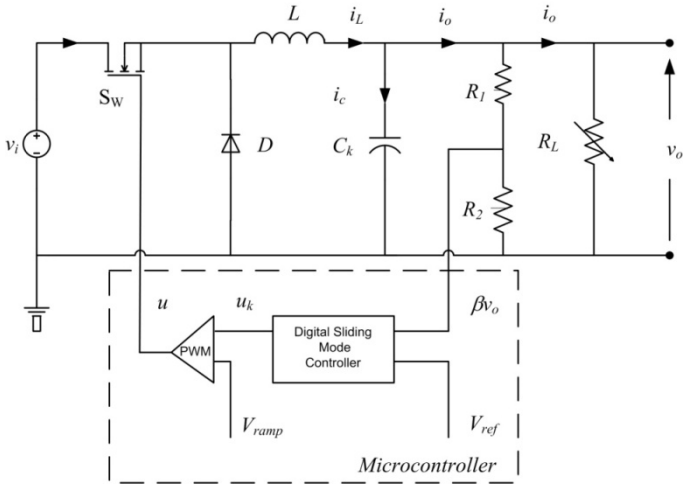


Figure 5.1 *Schematic diagram of DC-DC buck converter with DSMC*

The main disturbances are caused by load resistance and input voltage variations. The values of the state variables $x_1(t)$ and $x_2(t)$ may be determined by measuring sensed output and the capacitor current $i_C(t)$. To avoid the current acquisition, the implementation of discrete-time SMC algorithm based only on the input/output measurements is suggested. Once more, starting from (5.1), the transfer function of DC-DC buck converter (2.31) is:

$$W_{bc}(s)=\frac{Y(s)}{U(s)}=\frac{\dfrac{\beta V_i}{LC}}{s^2+\dfrac{1}{R_L C}s+\dfrac{1}{LC}} \tag{5.4}$$

where $Y(s)=\beta V_o(s)$, and under the assumption that control signal is constant during the sampling period *T*, the discrete-time input-output model is (2.32):

$$y_k=\frac{z^{-1}B(z^{-1})}{A(z^{-1})}u_k. \tag{5.5}$$

The control goal is to make the sensed output voltage $y_k = \beta v_{ok}$ stable, constant and equal to some constant reference voltage $V_{rk} = V_{ref}$ despite the variations of load resistance R_L and input voltage.

The algorithm implemented in voltage control of DC-DC buck converter is the combination of the DSMC and the well-known MVC technique [1], [2], which gives better system steady-state accuracy and chattering alleviation. The design goal is to find a control u_k that will force switching function:

$$s_k = C(z^{-1})(y_k - V_{rk}) \tag{5.6}$$

to its minimum value (zero value in the ideal case), i.e., that will keep system motion in the vicinity of the sliding hypersurface $s_k = 0$ determined by the quasi-sliding domain *S*. $C(z^{-1}) = c_0 + c_1 z^{-1} + c_2 z^{-2}$ is a polynomial with all zeros inside the unit disc. The system output in steady-state is defined by:

$$y_\infty = V_{ref} + \frac{s_\infty}{C(1)}. \tag{5.7}$$

Therefore, the system accuracy depends on the accuracy of switching function s_k, so that the smaller s_k is, the better precision is achieved. To achieve the design task, the control law is used in the form of:

$$u_k = -\frac{F(z^{-1})y_k - C(z^{-1})V_{rk} + \frac{\alpha T}{1 - z^{-1}}\operatorname{sgn}(s_k)}{E(z^{-1})B_n(z^{-1})} \tag{5.8}$$

where $E(z^{-1})$ and $F(z^{-1})$ are polynomials obtained as the solutions of Diophantine equation:

$$E(z^{-1})A_n(z^{-1}) + z^{-1}F(z^{-1}) = C(z^{-1}). \tag{5.9}$$

Note that herein $A_n(z^{-1})$ and $B_n(z^{-1})$ included in (5.8) and (5.9) denotes the polynomials with nominal converter parameters, i.e.:

$$A(z^{-1}) = A_n(z^{-1}) + \Delta A(z^{-1}), \tag{5.10}$$

$$B(z^{-1}) = B_n(z^{-1}) + \Delta B(z^{-1}) \tag{5.11}$$

where $\Delta A(z^{-1})$ and $\Delta B(z^{-1})$ are the polynomials with perturbed converter parameters. Notice that the relay component of the control $\operatorname{sgn}(s_k)$ is filtered through the discrete-time integrator. It is proved in [99] that the sum of all positive and negative values of $\operatorname{sgn}(s_k)$ is

equal to zero when the system is in the QSM. Consequently, the control signal should be smooth and equal to some average value proportional to the time-interval of reaching phase. This should result in chattering reduction. Theoretically, chattering free control law can be obtained if $T \to 0$.

The implementation of (5.8) in (5.5) gives:

$$\begin{aligned} &E(z^{-1})B_n(z^{-1})A_n(z^{-1})y_k = -E(z^{-1})B_n(z^{-1})\Delta A(z^{-1})y_k + \\ &+z^{-1}B(z^{-1})(-F(z^{-1})y_k + C(z^{-1})V_{r\,k+1} - \frac{\alpha T}{1-z^{-1}}\operatorname{sgn}(s_k)). \end{aligned} \tag{5.12}$$

By adding $E(z^{-1})A_n(z^{-1})\Delta B(z^{-1})y_k$ to both sides of (5.12), one can get:

$$\begin{aligned} &B(z^{-1})C(z^{-1})(y_{k+1} - V_{r\,k+1}) = -B(z^{-1})\frac{\alpha T}{1-z^{-1}}\operatorname{sgn}(s_k) + \\ &+E(z^{-1})(A_n(z^{-1})\Delta B(z^{-1}) - B_n(z^{-1})\Delta A(z^{-1}))y_{k+1}. \end{aligned} \tag{5.13}$$

The polynomial $B(z^{-1})$ has roots always inside the unit disc in z-domain as $b_1 < b_0$ (see (2.31)). Therefore, (5.13) can be rewritten as:

$$s_{k+1} = s_k - \alpha T \operatorname{sgn}(s_k) + \frac{R(z^{-1})}{B(z^{-1})}(y_{k+1} - y_k) \tag{5.14}$$

where:

$$R(z^{-1}) = E(z^{-1})(A_n(z^{-1})\Delta B(z^{-1}) - B_n(z^{-1})\Delta A(z^{-1})). \tag{5.15}$$

Equation (5.14) defines the switching function dynamics. According to (5.6), the system is stable if QSM exists in the vicinity of $s_k = 0$, i.e., if s_k converges to the sliding manifold and stays there afterward. The difference $y_{k+1} - y_k$ is always bounded by appropriate choice of the polynomial $C(z^{-1})$, which proves the next Theorem.

Theorem 5.1: If the polynomial:

$$P(z^{-1}) = B(z^{-1})C(z^{-1}) + E(z^{-1})(B_n(z^{-1})\Delta A(z^{-1}) - A_n(z^{-1})\Delta B(z^{-1})) \tag{5.16}$$

has all roots inside the unit disc for a priori known and bounded system parameter variations $\Delta A(z^{-1})$ and $\Delta B(z^{-1})$, then there is a positive real number $\mathrm{Y} \in R$ fulfilling:

$$|y_{k+1} - y_k| < \mathrm{Y} \tag{5.17}$$

for every *k*.

Proof: Having in mind that $V_{r\,k+1} = V_{r\,k} = V_{ref}$, the difference $y_{k+1} - y_k$ can be defined directly from (5.13) as:

$$y_{k+1} - y_k = -\frac{B(z^{-1})}{P(z^{-1})}\alpha T \operatorname{sgn}(s_k). \tag{5.18}$$

It is obvious from (5.18) that $y_{k+1} - y_k$ is upper bounded (5.17) if $P(z^{-1})$ is Jury's polynomial. In the case of the limited system parameter perturbations, the stability of $P(z^{-1})$ can be ensured by the adequate selection of stable polynomial $C(z^{-1})$.

If (5.17) is fulfilled then there is a positive real number $\Lambda \in R$ so that:

$$\max \left| \frac{R(z^{-1})}{B(z^{-1})}(y_{k+1} - y_k) \right| < \Lambda, \tag{5.19}$$

since $B(z^{-1})$ is stable polynomial. To provide stable switching function dynamics, i.e., to ensure the existence of QSM, the parameter α should be selected according to the following Theorem.

Theorem 5.2: If a parameter α meets the following inequality [2]:

$$\alpha T > \Lambda \tag{5.20}$$

where Λ is determined by (5.19), then there is an integer number $K_0 = K_0(s_0)$ so that the system trajectory enters quasi-sliding manifold S, determined by:

$$S = \left\{ s_k : |s_k| < \alpha T + \Lambda \right\}, \tag{5.21}$$

and stays in it for every $k > K_0$.

Proof: See Appendix A.

The overall system stability is ensured if and only if the conditions of the next Theorem 5.3 are fulfilled.

Theorem 5.3: System described by (5.5), (5.6) and (5.8) is stable if and only if:

1) the inequality (5.20) is fulfilled for every k, i.e., QSM exists in the system, and
2) the polynomial $C\left(z^{-1}\right)$ has its roots inside the unit disc in z-plane.

Proof: If the parameter α is chosen to fulfill the inequality (5.20), then according to Theorem 5.2, QSM exists in the domain S. Now, one can see from (5.6) that y_k will converge to the constant reference voltage V_{ref} if and only if the polynomial $C\left(z^{-1}\right)$ is stable.

5.1.2 Simulation Results

The digital simulation has been performed to verify the DSM voltage controller for DC-DC buck converter. The converter parameter values are given in Table 5.1.

Table 5.1 *Buck converter parameter values*

Description	Parameter	Value
Input voltage	V_i	24 V
Desired output voltage	V_o	12 V
Capacitance	C_k	1470 μF
Capacitance resistance	r_C	69 mΩ
Inductance	L	330 μH
Inductance resistance	r_L	0.12 Ω
PWM frequency	f_{pwm}	7.874 kHz
Sampling period	T	0.5 ms
Minimum load resistance	R_{L_min}	11 Ω
Maximum load resistance	R_{L_max}	33 Ω

The DSM controller parameters have been chosen as follows: the sampling period is $T = 0.5\,\text{ms}$, $C(z^{-1}) = 1 - 1.067z^{-1} + 0.2846z^{-2}$, $E(z^{-1}) = 1$, $F(z^{-1}) = 0.4279 - 0.7z^{-1}$, $V_{ref} = 1.2\,\text{V}$, the switching and sensor gains are $\alpha = 1.25$ and $\beta = 0.1$, respectively.

The simulation scenario is formed by varying the input voltage between 21 V, 24 V and 27 V whereas the load resistance is changed between 11 Ω, 16.5 Ω and 33 Ω. Namely, the step load changes from R_L = 33 Ω to R_L = 16.5 Ω, from R_L = 16.5 Ω to R_L = 11 Ω and from R_L = 33 Ω to R_L = 11 Ω are applied at three different input voltage values: minimum (V_i = 21 V), nominal (V_i = 24 V) and maximum (V_i = 27 V). The simulation results in the form of the output voltage v_o and current i_o waveforms are presented in Figures 5.2-5.4.

The results show that the suggested approach for control of DC-DC buck converter, using DSMC in combination with MVC, is very appropriate for the digitally controlled power converter and for the system requirement accomplishments. The high output voltage accuracy is ensured in the presence of load and input voltage variations. Furthermore, filtering the switching control component through the discrete-time integrator reduces chattering. The control algorithm is based only on measuring of output voltage signal rejecting the use of the expensive additional current sensors in that way. It is reasonable to expect certain performance degradation in the practical implementation of the suggested DSM voltage controlled buck converter due to PWM nonlinearities, finite measuring precision, noise and other. That is why the experimental verification is done, and the results are presented in the following section.

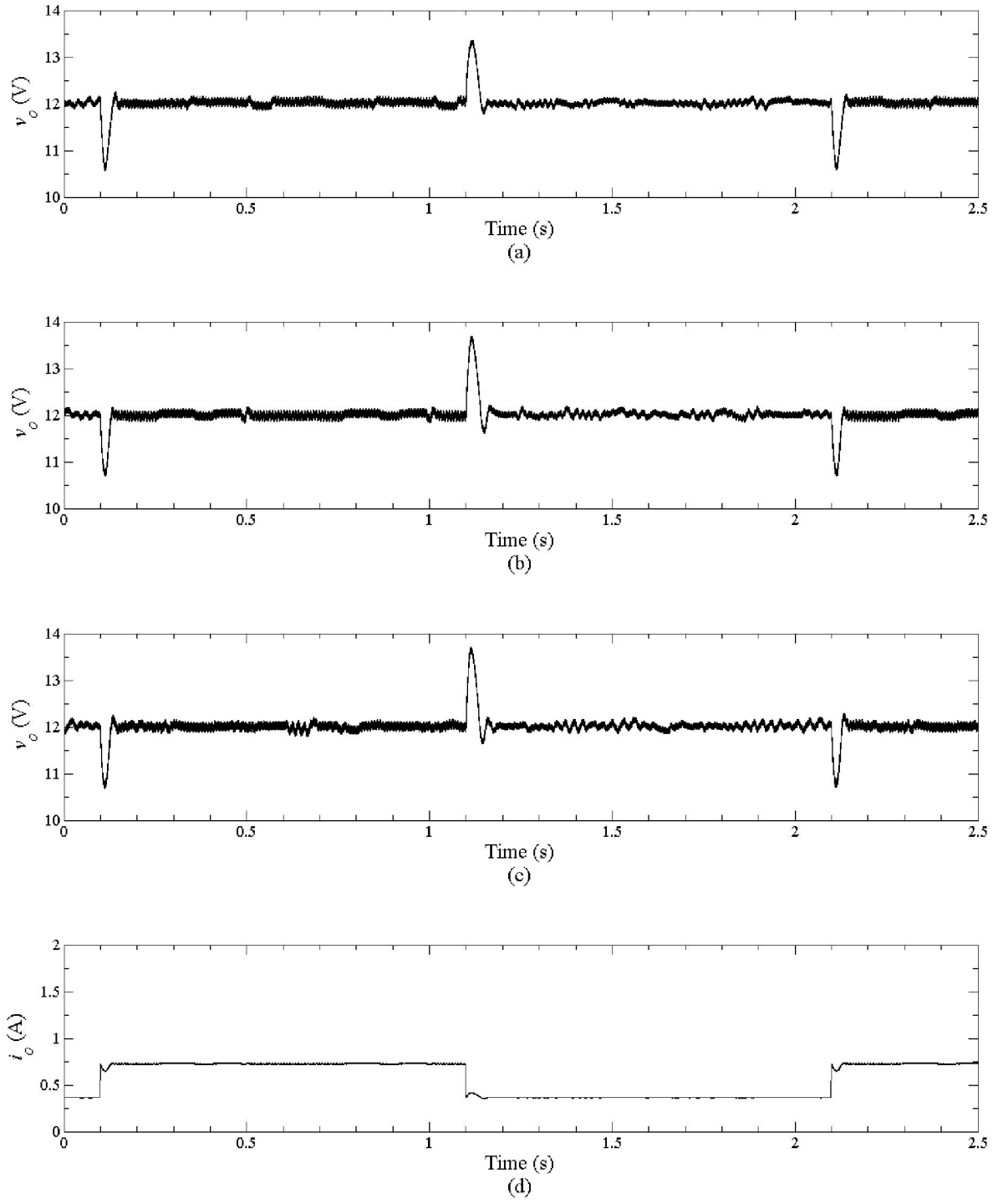


Figure 5.2 *Simulation waveforms of v_o (a-c) and i_o (d) of the buck converter with DSMC alternating between load resistance 33 Ω and 16.5 Ω and operating at V_i = 21 V (a), V_i = 24 V (b) and V_i = 27 V (c)*

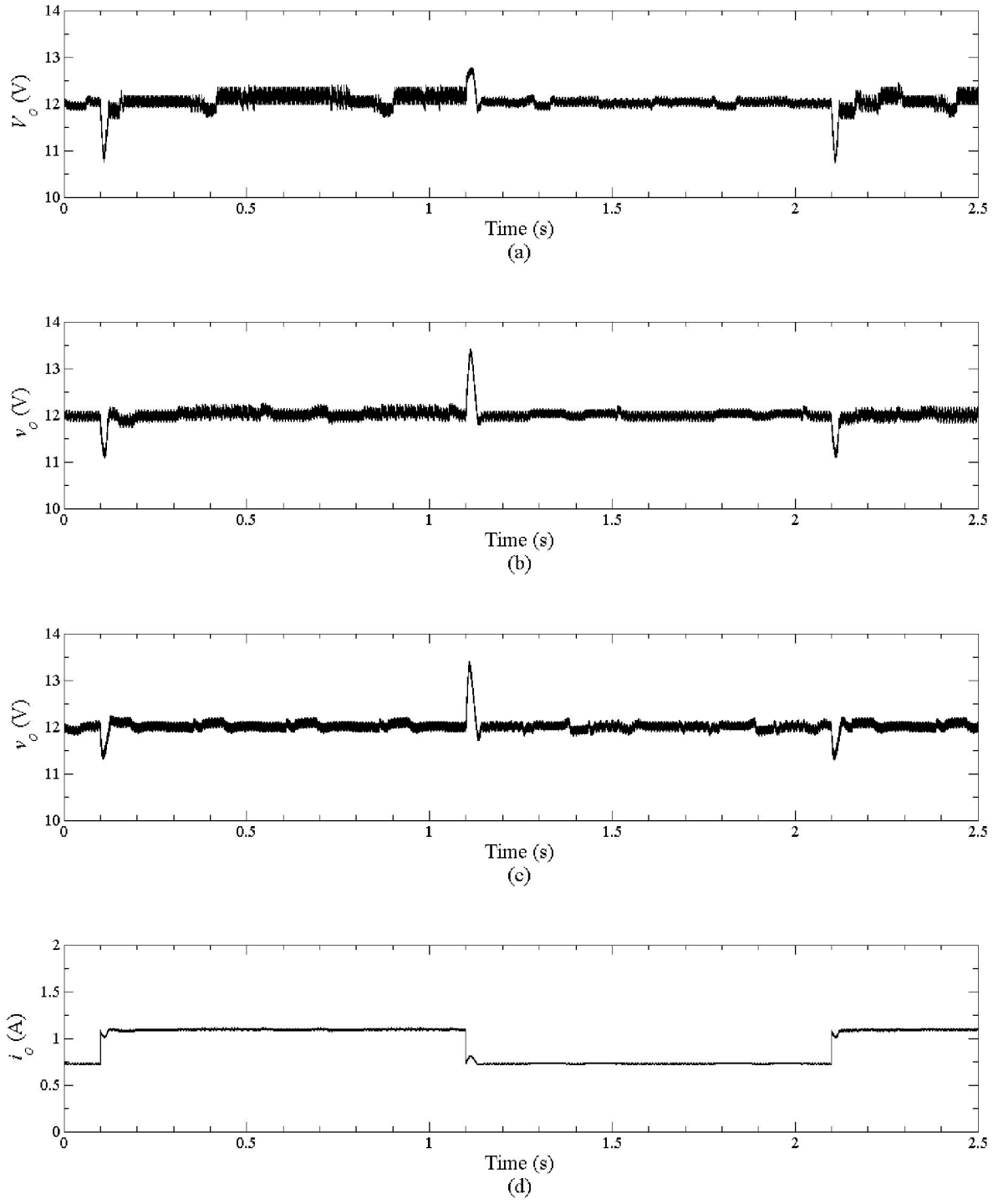


Figure 5.3 *Simulation waveforms of v_o (a-c) and i_o (d) of the buck converter with DSMC alternating between load resistance 16.5 Ω and 11 Ω and operating at V_i = 21 V (a), V_i = 24 V (b) and V_i = 27 V (c)*

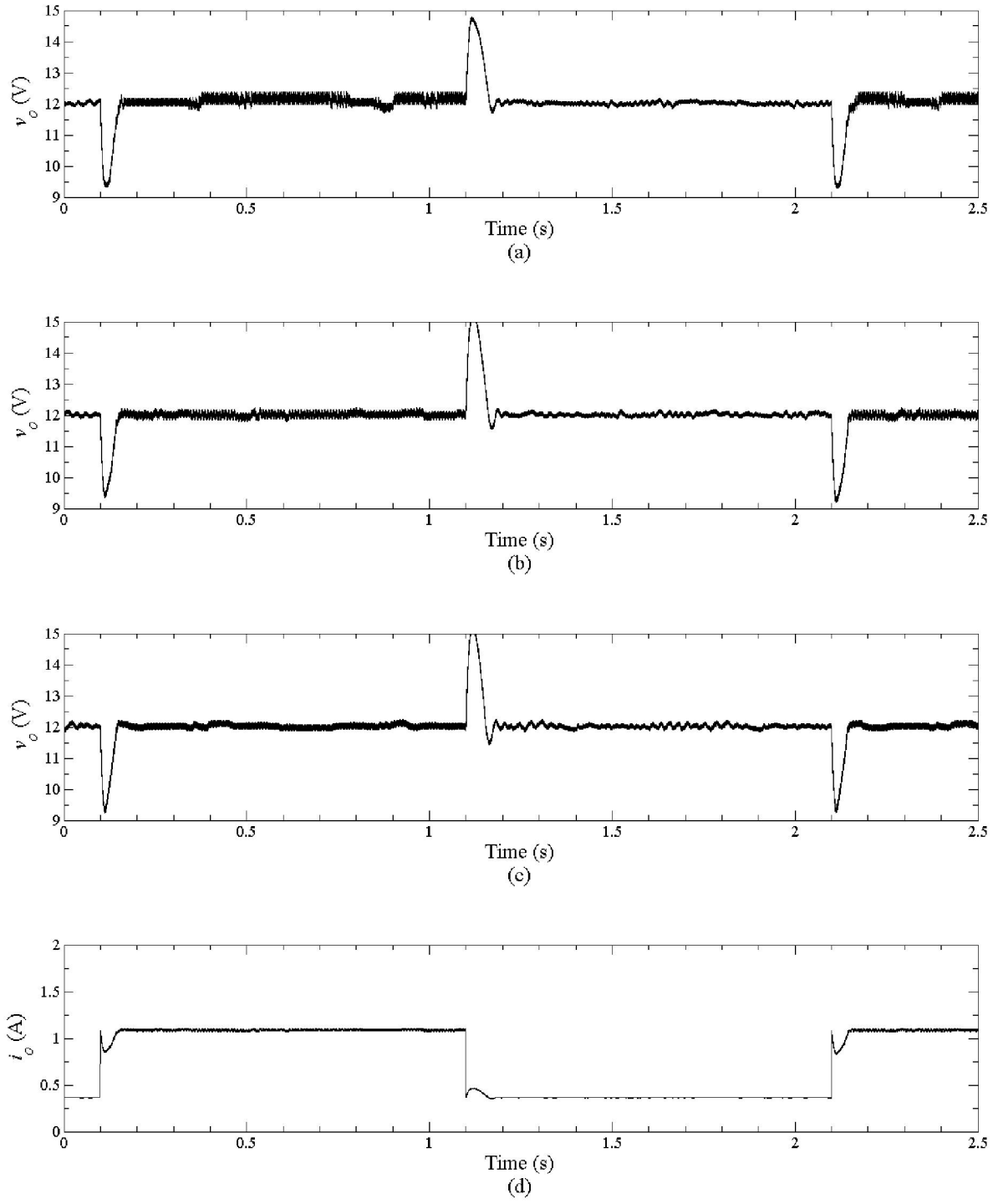


Figure 5.4 *Simulation waveforms of v_o (a-c) and i_o (d) of the buck converter with DSMC alternating between load resistance 33 Ω and 11 Ω and operating at V_i = 21 V (a), V_i = 24 V (b) and V_i = 27 V (c)*

5.1.3 EXPERIMENTAL RESULTS

In order to obtain experimental results, the experimental prototype has been developed and presented in Figure 5.5. The scheme of microcontroller based buck converter is given in Figure 5.6. The values of converter parameters are listed in Table 5.1. The controller parameters are selected to be the same as in the digital simulation.

DSMC algorithm is realized by using 8-bit microcontroller ATmega8 [140]. The sensed output voltage is fed into its 10-bit A/D converter. PWM is also incorporated in the microcontroller with the switching frequency f_{pwm} = 7.874 kHz.

The scenario is the same as in the case of digital simulation of the DC-DC buck converter with DSMC. In order to analyze load and line regulation properties of the realized microcontroller based buck converter with DSMC, the step load changes from R_L = 33 Ω to R_L = 16.5 Ω, from R_L = 16.5 Ω to R_L = 11 Ω and from R_L = 33 Ω to R_L = 11 Ω are made at three different input voltage values: minimum (V_i = 21 V), nominal (V_i = 24 V) and maximum (V_i = 27 V). The experimental results in the form of the output voltage v_o and current i_o waveforms are given in Figures 5.7-5.9. They are consistent with the simulation results largely.

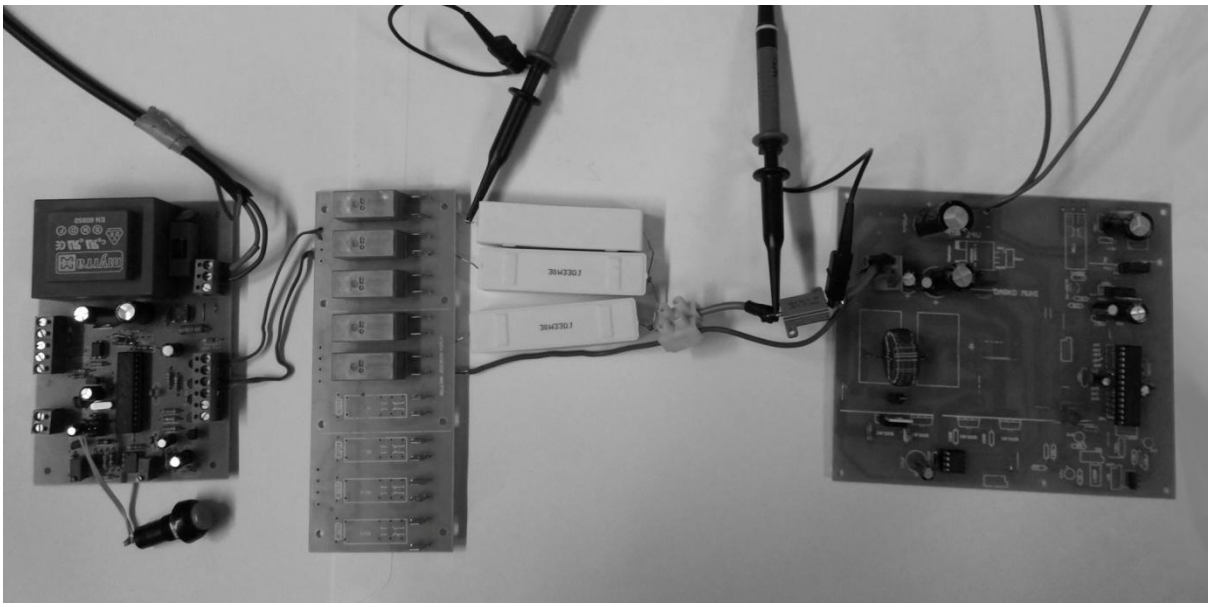


Figure 5.5 *Experimental prototype of the suggested buck converter*

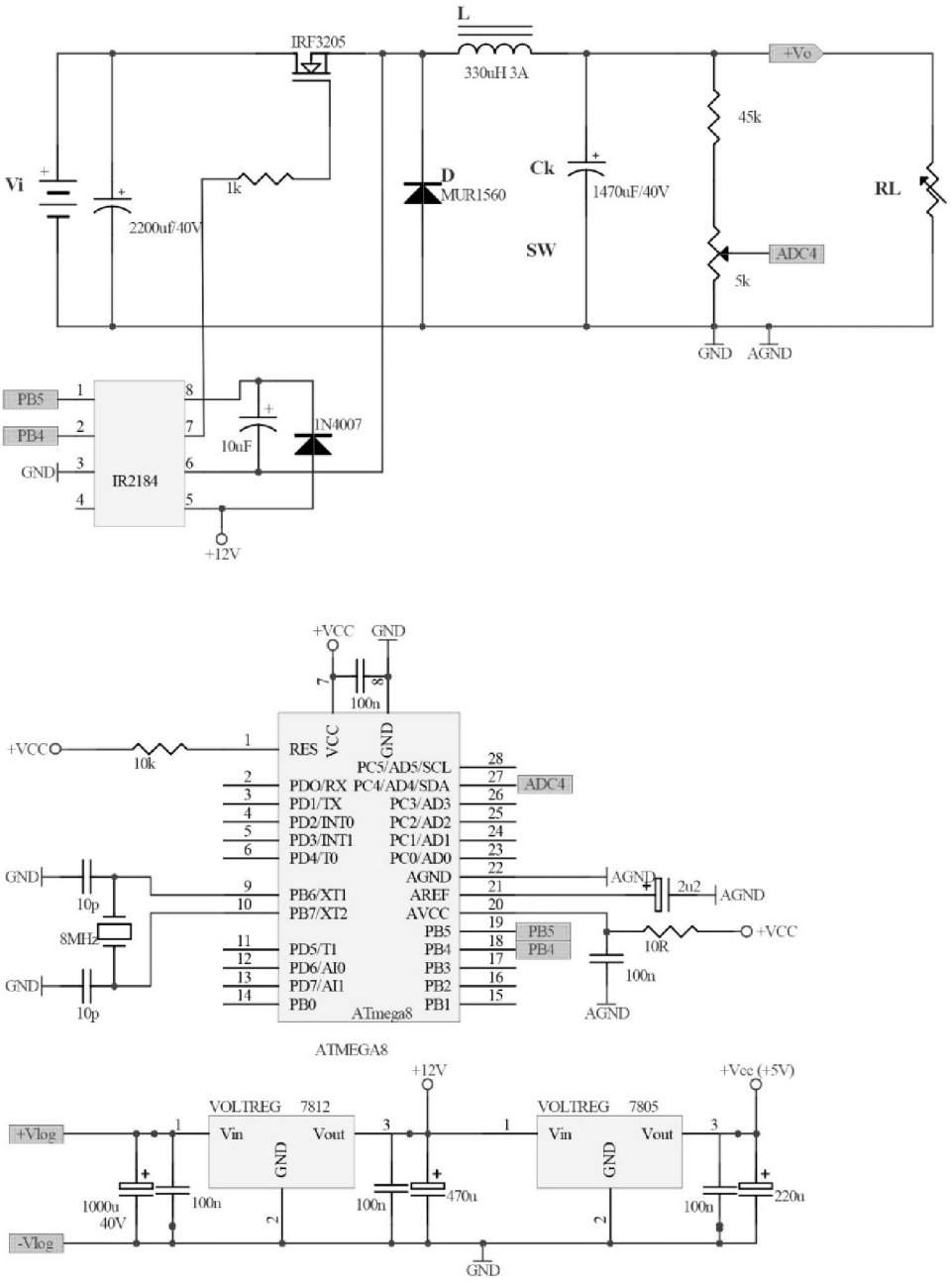


Figure 5.6 *Scheme of buck converter realization with ATmega8 microcontroller*

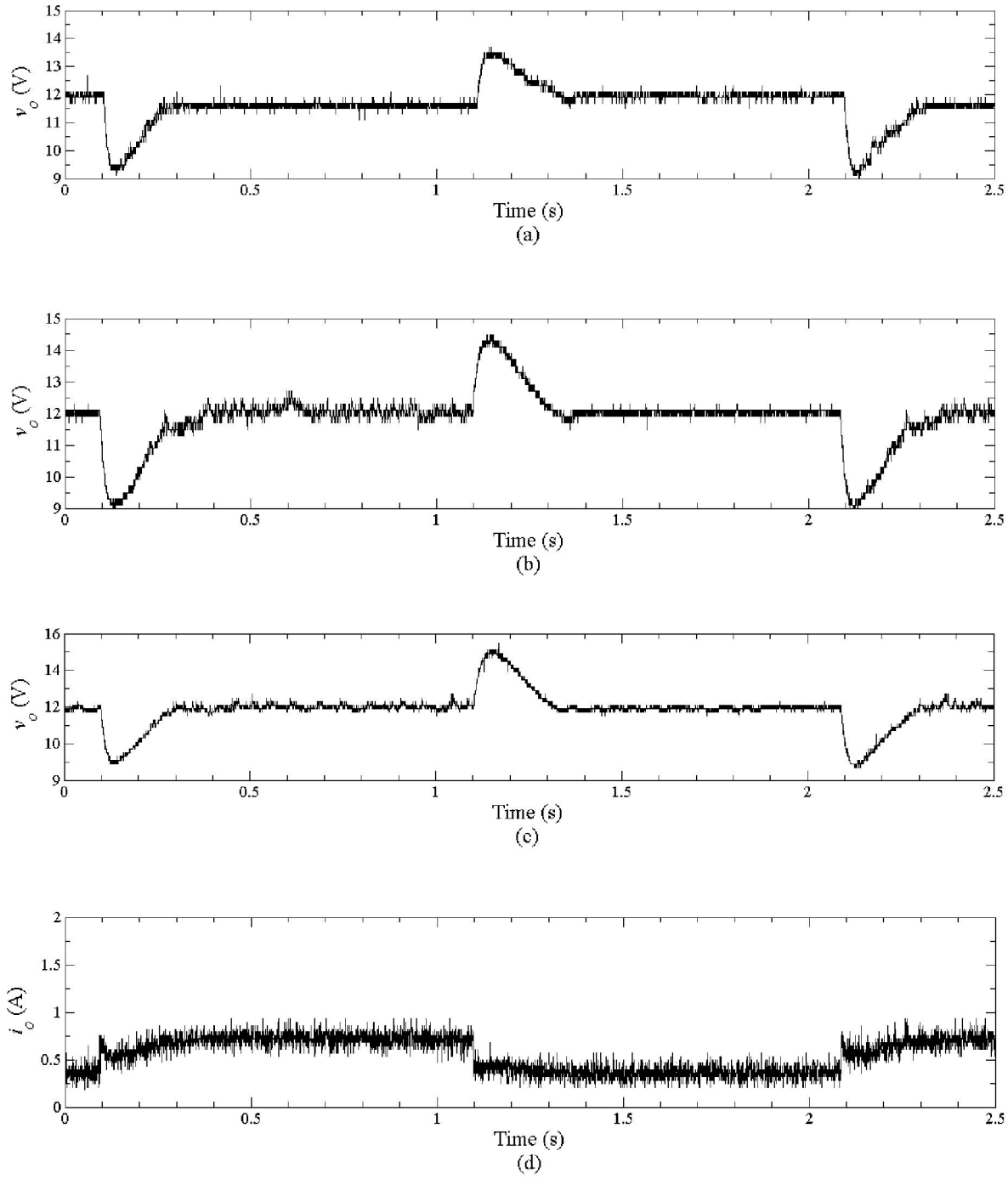


Figure 5.7 *Experimental waveforms of v_o (a-c) and i_o (d) of the buck converter with DSMC alternating between load resistance 33 Ω and 16.5 Ω and operating at V_i = 21 V (a), V_i = 24 V (b) and V_i = 27 V (c)*

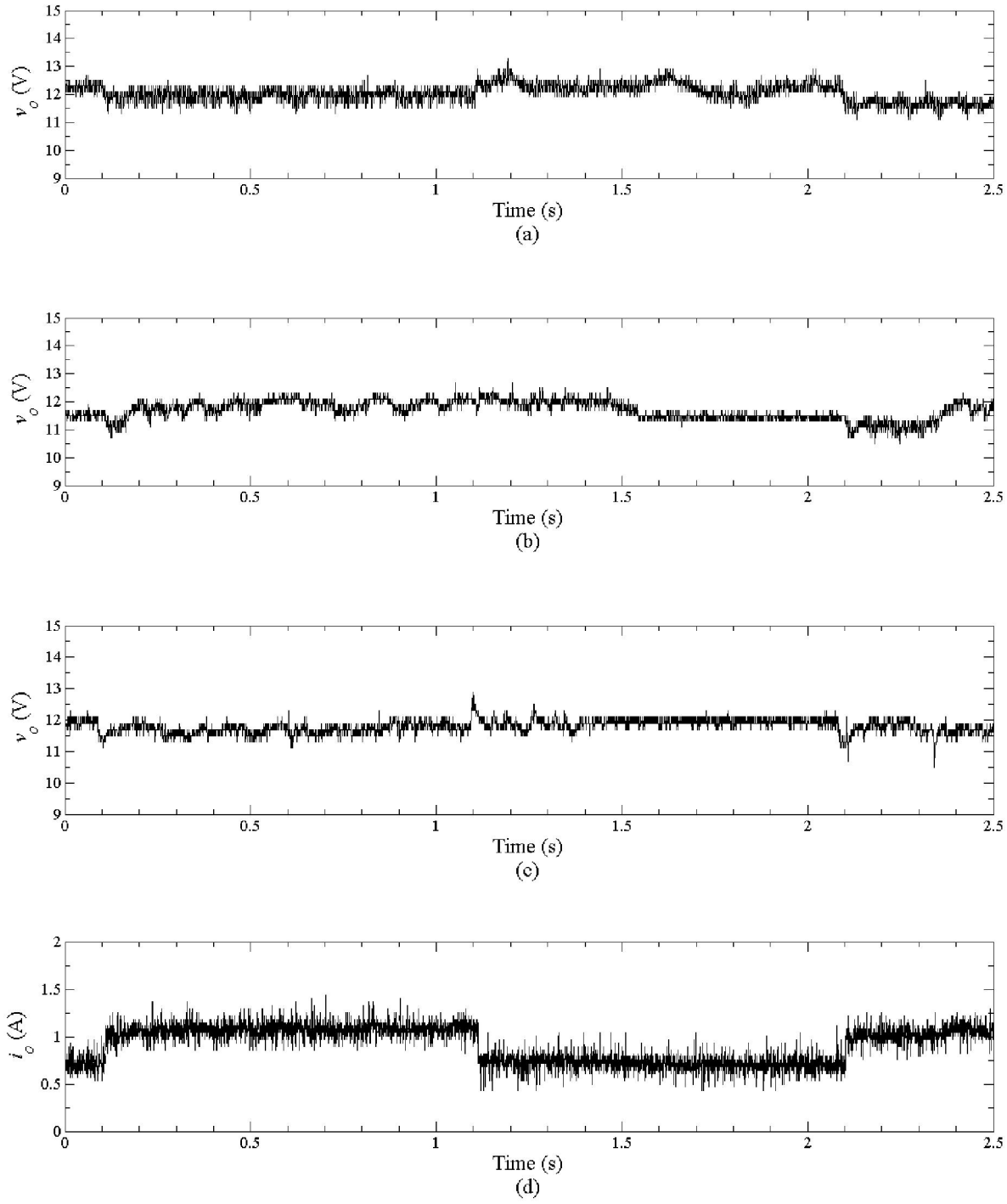


Figure 5.8 *Experimental waveforms of v_o (a-c) and i_o (d) of the buck converter with DSMC alternating between load resistance 16.5 Ω and 11 Ω and operating at V_i = 21 V (a), V_i = 24 V (b) and V_i = 27 V (c)*

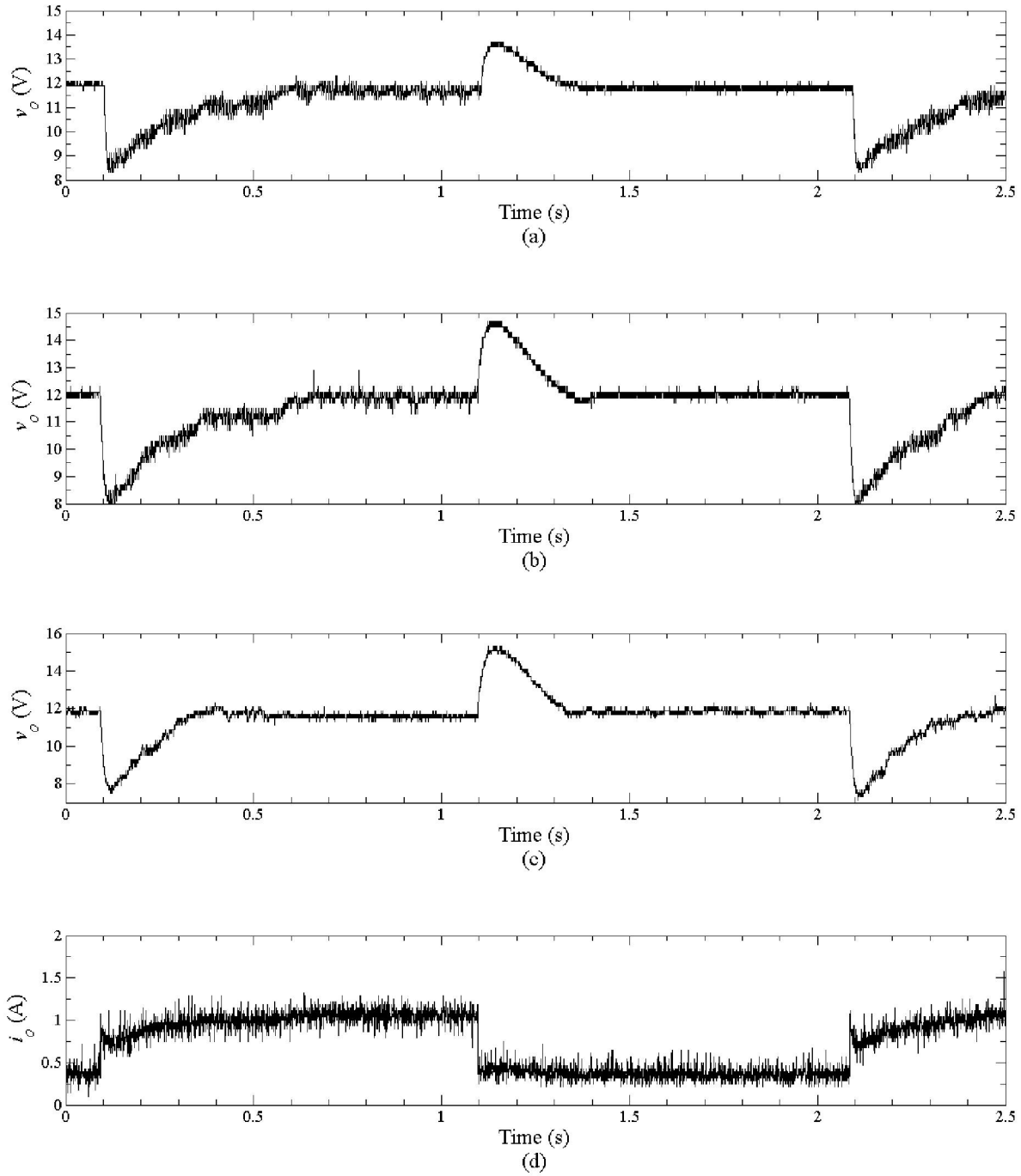
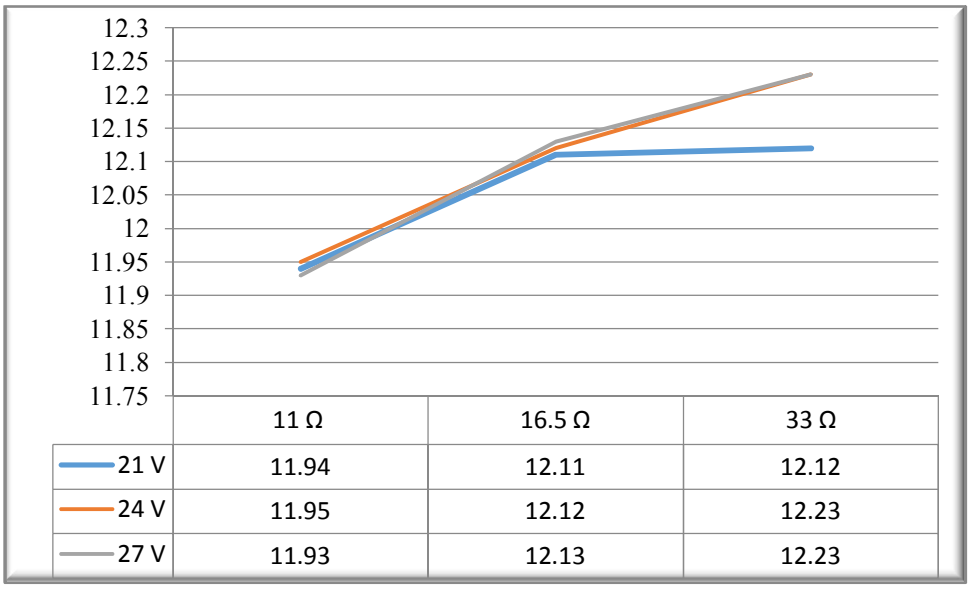


Figure 5.9 *Experimental waveforms of v_o (a-c) and i_o (d) of the buck converter with DSMC alternating between load resistance 33 Ω and 11 Ω and operating at V_i = 21 V (a), V_i = 24 V (b) and V_i = 27 V (c)*



	11 Ω	16.5 Ω	33 Ω
21 V	11.94	12.11	12.12
24 V	11.95	12.12	12.23
27 V	11.93	12.13	12.23

Figure 5.10 *Plots of V_o against R_L for the buck converter at minimum, nominal and maximum V_i (DC values)*

According to Table 5.2, the maximum load regulation error occurs at V_i = 21 V with a deviation of 1.50% from v_o at the nominal condition. On the other hand, the maximum line regulation error is at the minimum load (R_L = 33 Ω) with a deviation of 0.92% from v_o at the nominal condition (see Table 5.3). It is worth noting that the load and line regulation properties depend largely on microcontroller's A/D converter and PWM resolution as well as on the choice of DSMC parameters $C(z^{-1})$, α and T. Theoretically, according to (5.7), the converter steady-state error should be approximately 287 mV. Therefore, a better accuracy may be expected if a faster microcontroller with better A/D converter and PWM resolution is used.

Table 5.2 *Load regulation property*

$V_{o\ (nominal\ condition)}$ = 11.95 V at V_i = 24 V and R_{Lmin} = 11 Ω

V_i	$\Delta V_o = V_{o\ (33\ \Omega)} - V_{o(11\ \Omega)}$	$\frac{\Delta V_o}{V_{o(nominal\ condition)}} \times 100\%$
21 V	0.18 V	1.50 % of $V_{o\ (nominal\ condition)}$
24 V	0.28 V	2.34 % of $V_{o\ (nominal\ condition)}$
27 V	0.30 V	2.51 % of $V_{o\ (nominal\ condition)}$

Table 5.3 *Line regulation property*

($V_{o\ (nominal\ condition)}$ = 11.95 V at V_i = 242 V and R_{Lmin} = 11 Ω)

Loading condition	$\Delta V_o = V_{o\ (Vi=27\ V)} - V_{o\ (Vi=21\ V)}$	$\frac{\Delta V_o}{V_{o(nominal\ condition)}} \times 100\%$
R_{L_max} = 33 Ω	0.11 V	0.92 % of $V_{o\ (nominal\ condition)}$
R_{L_med} = 16.5 Ω	0.02 V	0.17 % of $V_{o\ (nominal\ condition)}$
R_{L_min} = 11 Ω	0.01 V	0.08 % of $V_{o\ (nominal\ condition)}$

5.2 DC-DC BOOST CONVERTER WITH DIGITAL SLIDING MODE CONTROL

In this section, DSMC will be discussed, which uses the input-output model of boost converter in the form of a discrete-time transfer function. The algorithm here is also the combination of GMV and DSMC techniques. The boost DC-DC converter working in CCM suffers from the appearance of right-half-plane-zero (RHPZ) in its duty-cycle-to-output-voltage transfer function because of the use of PWM techniques. In this case, the state-space average model is obtained and that is why the design of the voltage controller for this type is more difficult than the voltage controller at buck converter. Also, in this converter, the chattering phenomenon is alleviated by filtering the discrete-time SMC components using a discrete-time integrator.

5.2.1 DIGITAL SLIDING MODE CONTROL DESIGN PROCEDURE

The starting conditions in the design are now:

$$L > L_B \quad , L_B = \frac{(1-D)^2 D R_L}{2 f_{pwm}}, \tag{5.22}$$

$$C > C_{min} \quad , \quad C_{\min} = \frac{D V_o}{V_r R_L f_{pwm}} \tag{5.23}$$

and the mathematical model of DC-DC boost converter given in the form of the discrete-time transfer function is derived from the state-space model (2.48) [18]. The schematic diagram of DC-DC boost converter with the proposed DSMC is presented in Figure 5.11. Herein, C_k, L, R_L are capacitance, inductance and load resistance of the converter, respectively; $i_C(t)$,$i_L(t)$, $i_o(t)$ are capacitor, inductor and output (load) currents, respectively; V_{ref}, $v_i(t)$ and $v_o(t)$ denote the reference, input and output voltages, respectively; β denotes sensor gain whereas u represents the signal driving the power switch S_w. For the sake of brevity, the used model will

be explained herein once more. The boost converter operating in CCM is considered in the modeling process. By taking the output voltage and its time-derivative for the state coordinates ($x_1(t)=v_o(t), x_2(t)=\dot{x}_1(t)=\mathrm{d}v_o(t)/\mathrm{d}t$), the linearized small signal state-space continuous-time model of boost converter in the controllable canonical form can be written in the following form [18].

$$\begin{aligned}\dot{x}(t) &= \begin{bmatrix} 0 & 1 \\ 0 & -\dfrac{1}{R_L C_k} \end{bmatrix} x(t) + \begin{bmatrix} 0 \\ \dfrac{V_i - V_o}{L C_k} \end{bmatrix} u(t), \\ y(t) &= \begin{bmatrix} \beta & 0 \end{bmatrix} x(t) \end{aligned} \tag{5.24}$$

where V_i and V_o are nominal values of boost converter input and output voltages.

The transfer function of boost converter can be derived directly from Eq. (5.24) as:

$$W_{boost}(s) = \frac{Y(s)}{U(s)} = \frac{\dfrac{\beta(V_i - V_o)}{LC}}{s^2 + \dfrac{1}{R_L C} s} \tag{5.25}$$

and the input-output model of boost converter in z-domain is given by:

$$y_k = \frac{z^{-1} B(z^{-1})}{A(z^{-1})} u_k \tag{5.26}$$

where $A(z^{-1})$ and $B(z^{-1})$ are defined by (5.10) and (5.11), respectively.

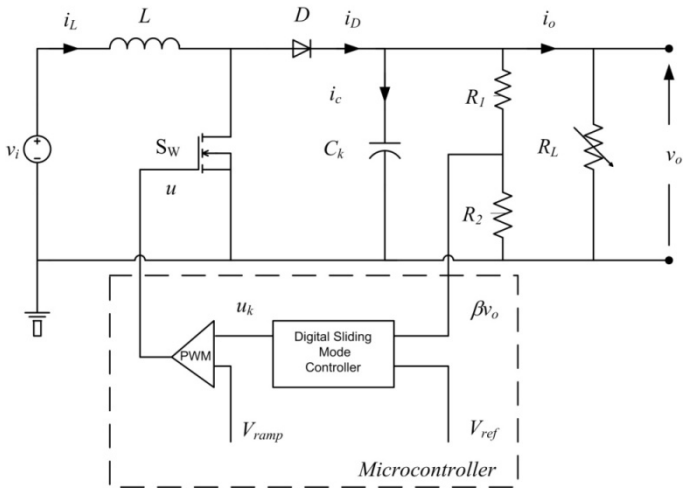


Figure 5.11 *Schematic diagram of DC-DC boost converter with DSMC*

The main aim of control design is to maintain the sensed output voltage $y_k=\beta v_{ok}$ stable, constant and equal to some reference voltage $V_{rk}=V_{ref}$ despite the variations of load resistance R_L and input voltage. In order to achieve the design task, DSMC algorithm [1], [2] is used to control DC-DC boost converter. It is determined by:

$$u_k = -\frac{F(z^{-1})y_k - C(z^{-1})V_{r\,k+1} + \dfrac{\alpha T}{1-z^{-1}}\operatorname{sgn}(s_k)}{E(z^{-1})B_n(z^{-1}) + Q(z^{-1})} \tag{5.27}$$

where s_k represents the switching function given by:

$$s_{k+1} = C(z^{-1})\left(y_{k+1} - V_{r\,k+1}\right) + Q(z^{-1})u_k\,. \tag{5.28}$$

$C(z^{-1})$ is a polynomial with all zeros inside the unit disc of z-plane and $Q(1)=0$. $E(z^{-1})$ and $F(z^{-1})$ are solutions of Diophantine equation (5.9). $s_k=0$ is the equation of sliding hypersurface in general case.

The closed-loop dynamics is directly derived from (5.26) and (5.28) in the form of [1]:

$$y_k = \frac{B(z^{-1})\left(C(z^{-1})V_{r\,k} + s_k\right)}{B(z^{-1})C(z^{-1}) + A(z^{-1})Q(z^{-1})}. \tag{5.29}$$

It is obvious from (5.29) that in order to guarantee the system stability, all the roots of equation $B(z^{-1})C(z^{-1}) + A(z^{-1})Q(z^{-1}) = 0$ should be inside the unit disc in the z-plane and the pairs ($B(z^{-1})$, $Q(z^{-1})$),($C(z^{-1})$, $A(z^{-1})$) and ($C(z^{-1})$, $Q(z^{-1})$) should not have common zeroes outside this disc, under the assumption that s_k is bounded. The system steady-state accuracy can be obtained from (5.29) for $z=1$ and $Q(1)=0$ as (5.7).

Substituting (5.27) in (5.26), taking into account (5.9), (5.10), (5.11) and (5.28), one can get:

$$B(z^{-1})s_{k+1} = -\frac{\alpha T B(z^{-1})\operatorname{sgn}(s_k)}{1-z^{-1}} + R(z^{-1})y_{k+1} \tag{5.30}$$

where $R(z^{-1}) = E(z^{-1})(A_n(z^{-1})\Delta B(z^{-1}) - B_n(z^{-1})\Delta A(z^{-1}))$. Replacing y_{k+1} in (5.30) by (5.29) and having in mind that $V_{r\,k+1} = V_{r\,k} = V_{ref} = const.$, one can get:

$$\Delta s_{k+1} = -\frac{B(z^{-1})C(z^{-1}) + A(z^{-1})Q(z^{-1})}{B(z^{-1})C(z^{-1}) + A(z^{-1})Q(z^{-1}) - R(z^{-1})}\alpha T \operatorname{sgn}\left(s_k\right) \tag{5.31}$$

where $\Delta s_{k+1} = s_{k+1} - s_k$ is bounded if all the roots of the equation $B(z^{-1})C(z^{-1}) + A(z^{-1})Q(z^{-1}) - R(z^{-1}) = 0$ are inside the unit disc in the z-plane. The latter is accomplished by the appropriate selection of the polynomials $C(z^{-1})$ and $Q(z^{-1})$. Finally, the switching function dynamics is defined as:

$$s_{k+1} = s_k - \alpha T \operatorname{sgn}(s_k) + l_{k+1} \tag{5.32}$$

with:

$$l_k = \frac{R(z^{-1})}{B(z^{-1})C(z^{-1}) + A(z^{-1})Q(z^{-1})}\Delta s_k \tag{5.33}$$

including all the parameter perturbations and, obviously, $|l_k| \le \Lambda$, where Λ is a positive real constant.

According to Theorem 5.2, if $\alpha > \Lambda / T$, a quasi-sliding motion is established in Δ-vicinity of s_k=0, i.e., $|s_k| \le \Delta$ is always fulfilled, where Δ is a function of αT. As a consequence, the whole system is stable if Theorem 3.4 is valid.

5.2.2 SIMULATION RESULTS

The digital simulation has been conducted to validate DSM voltage controller for DC-DC boost converter. The converter parameter values are given in Table 5.4. DSM controller parameters have been selected as follows: the sampling period is $T = 1\text{ms}$, $V_{ref} = 2.4\text{V}$, $C(z^{-1}) = 1 - 1.067z^{-1} + 0.2846z^{-2}$, $F(z^{-1}) = 0.9132 - 0.6956z^{-1}$, $Q(z^{-1}) = 0.05(1 - z^{-1})$, $E(z^{-1}) = 1$, the switching and sensor gains are $\alpha = 10$ and $\beta = 0.1$, respectively.

The simulation scenario is formed by varying the input voltage between 10.5 V, 12 V and 13.5 V whereas the load resistance is changed between 22.67 Ω, 34 Ω and 68 Ω. Namely, the step load changes from R_L = 68 Ω to R_L = 34 Ω, from R_L = 34 Ω to R_L = 22.67 Ω and from R_L = 68 Ω to R_L = 22.67 Ω are applied at three different input voltage values: minimum (V_i = 10.5 V), nominal (V_i = 12 V) and maximum (V_i = 13.5 V). The simulation results in the form of the output voltage v_o and current i_o waveforms are given in Figures 5.12-5.14.

Table 5.4 *Boost converter parameter value*s

Description	Parameter	Value
Input voltage	V_i	12 V
Desired output voltage	V_o	24 V
Capacitance	C_k	1470 μF
Capacitance resistance	r_C	69 mΩ
Inductance	L	330 μH
Inductance resistance	r_L	0.12 Ω
PWM frequency	f_{pwm}	7.874 kHz
Sampling period	T	1 ms
Minimum load resistance	R_{L_min}	22.67 Ω
Maximum load resistance	R_{L_max}	68 Ω

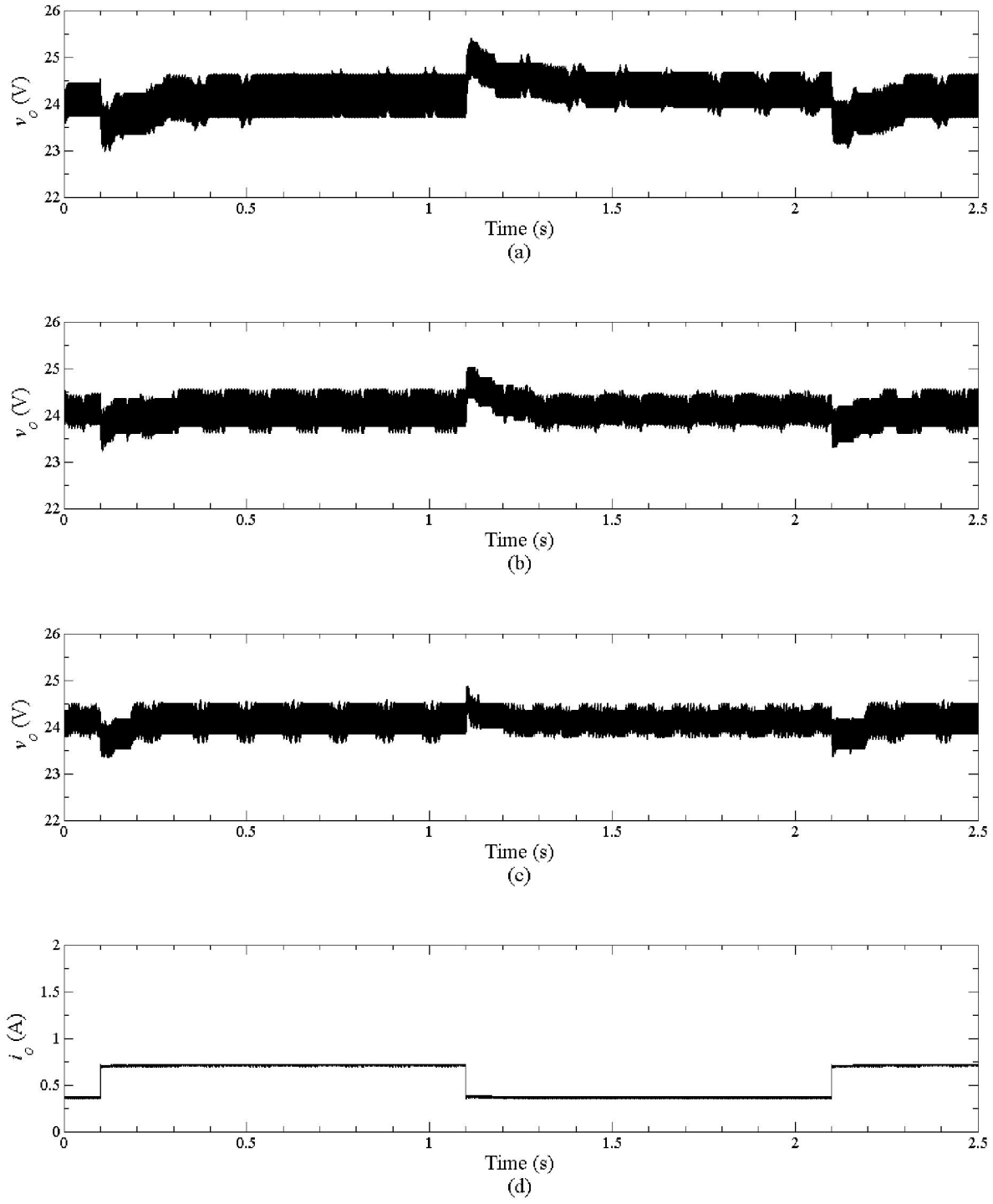


Figure 5.12 *Simulation waveforms of v_o (a-c) and i_o (d) of the boost converter with DSMC alternating between load resistance 68 Ω and 34 Ω and operating at V_i = 10.5 V (a), V_i = 12 V (b) and V_i = 13.5 V (c)*

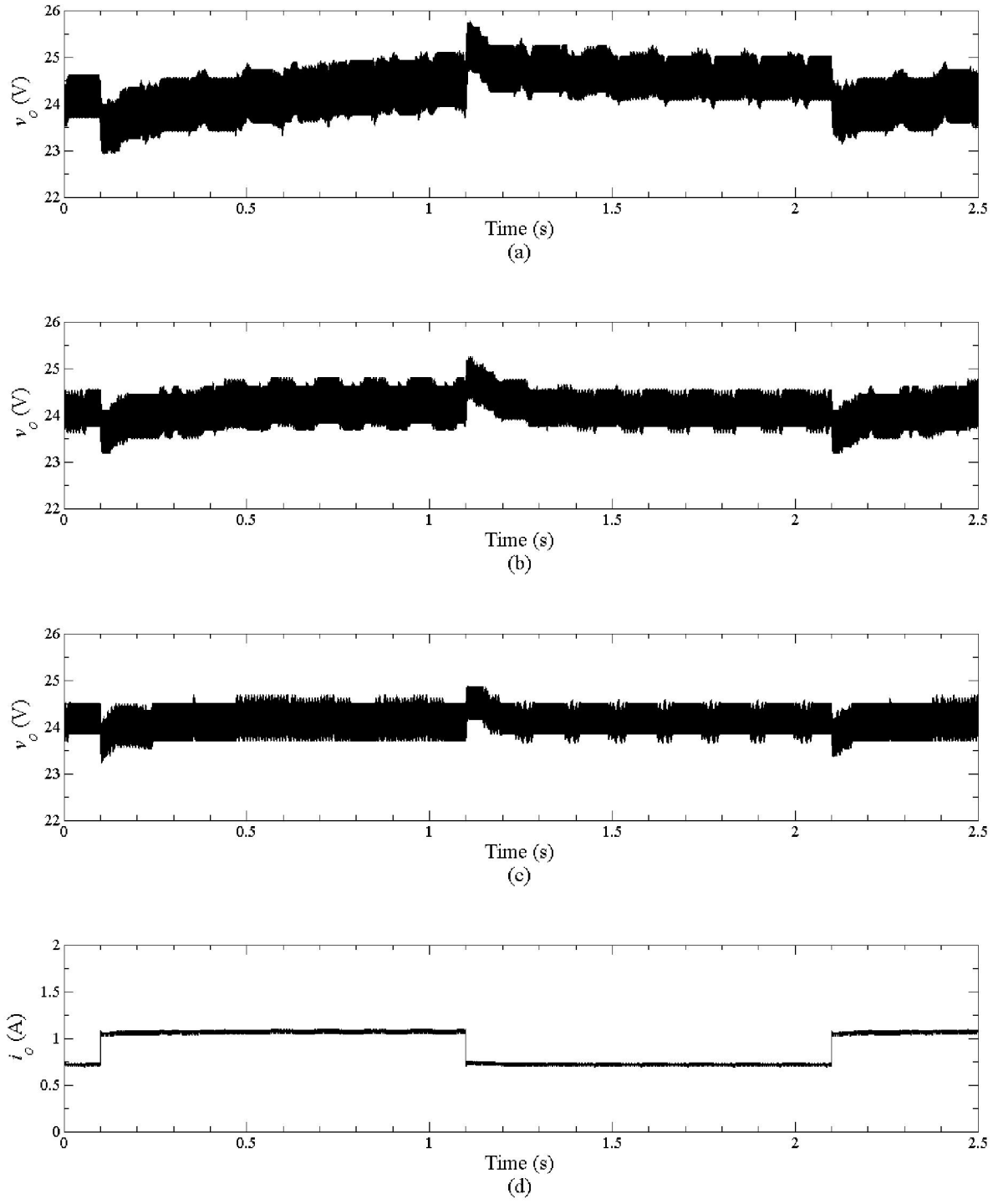


Figure 5.13 *Simulation waveforms of v_o (a-c) and i_o (d) of the boost converter with DSMC alternating between load resistance 34 Ω and 22.67 Ω and operating at V_i = 10.5 V (a), V_i = 12 V (b) and V_i = 13.5 V (c)*

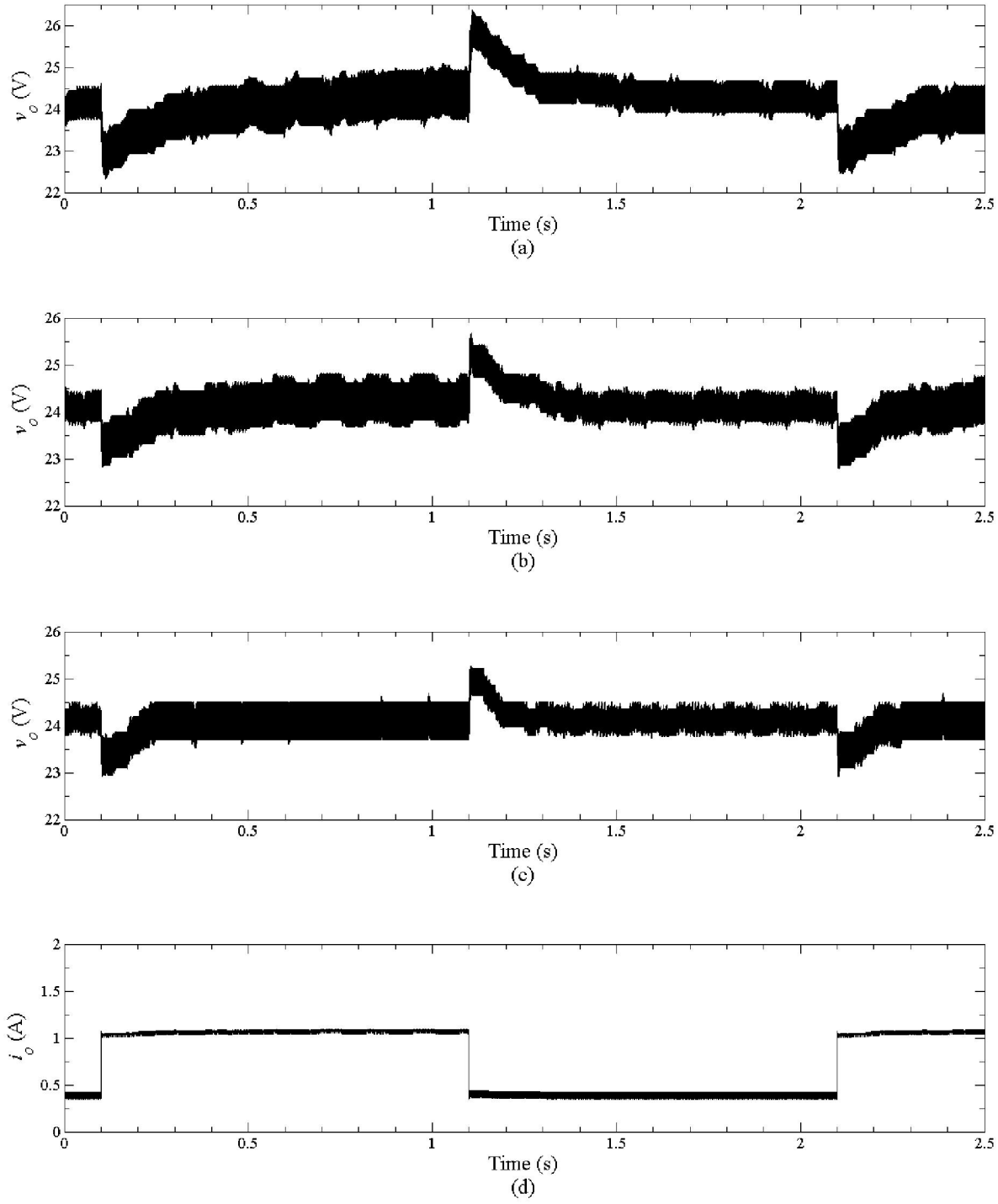


Figure 5.14 *Simulation waveforms of v_o (a-c) and i_o (d) of the boost converter with DSMC alternating between load resistance 68 Ω and 22.67 Ω and operating at V_i = 10.5 V (a), V_i = 12 V (b) and V_i = 13.5 V (c)*

The simulation results demonstrate good regulation performances under the load and input voltage variation. The certain performance degradation in the practical implementation of the proposed boost converter can be expected due to PWM nonlinearities, finite measuring precision, noise and other. Therefore, the experimental verification is carried out.

5.2.3 EXPERIMENTAL RESULTS

The experimental verification of the suggested boost converter is presented in this section. The developed experimental prototype is depicted in Figure 5.15 whereas the scheme of microcontroller based boost converter is shown in Figure 5.16. Table 5.4 contains the values of converter parameters. The parameters of DSMC are the same as in the digital simulation.

DSMC algorithm is realized by using 8-bit microcontroller ATmega8 [140]. The sensed output voltage is fed into its 10-bit A/D converter. PWM is also incorporated in the microcontroller with the switching frequency f_{pwm} = 7.874 kHz. Thanks to such choice of f_{pwm}, the influence of RHPZ in duty-cycle-to-output-voltage transfer functions is significantly suppressed but at the cost of lower bandwidth [108].

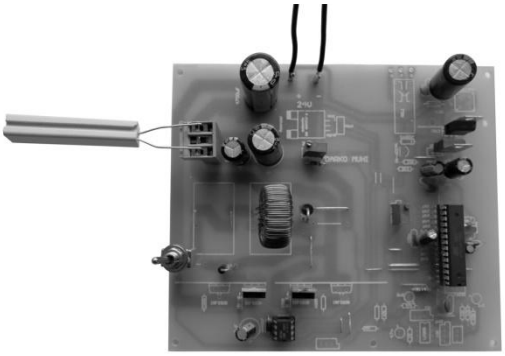


Figure 5.15 *Experimental prototype of the suggested boost converter*

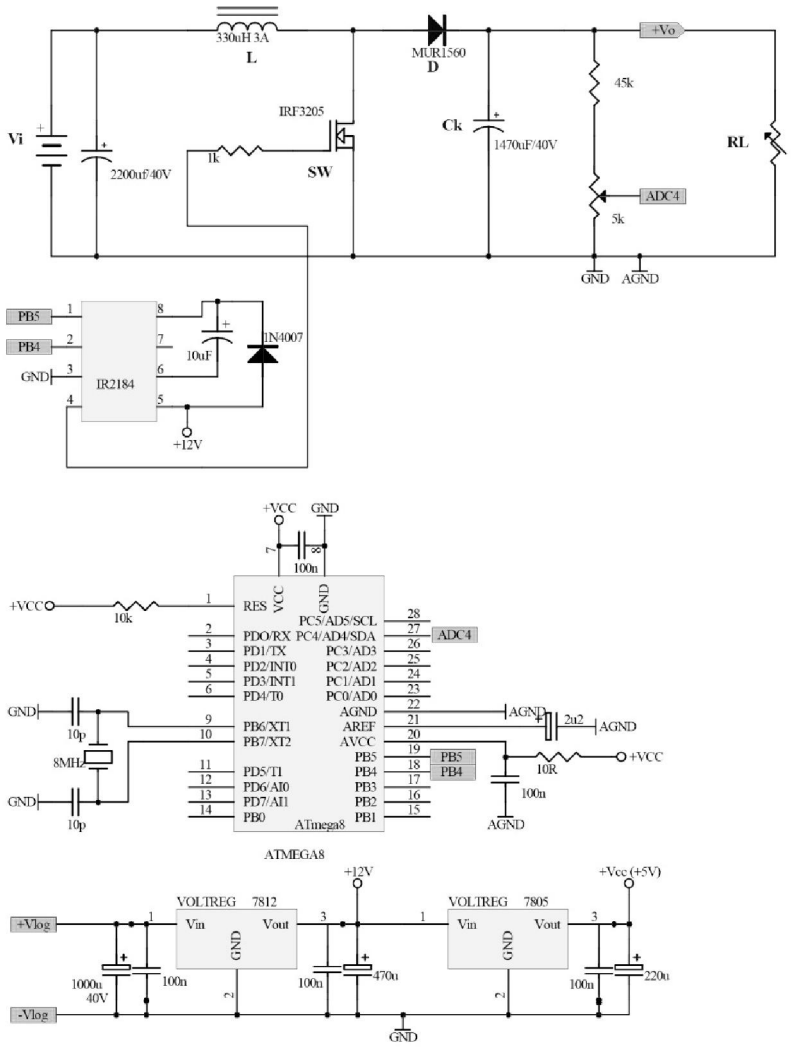


Figure 5.16 *Scheme of boost converter realization with ATmega8 microcontroller*

In order to analyze the load and line regulation properties of the realized microcontroller based boost converter with QSM control, the step load changes from R_L = 68 Ω to R_L = 34 Ω, from R_L = 34 Ω to R_L = 22.67 Ω and from R_L = 68 Ω to R_L = 22.67 Ω are applied at three different input voltage values: minimum (V_i = 10.5 V), nominal (V_i = 12 V) and maximum (V_i = 13.5 V). The experimental results in the form of the output voltage v_o and current i_o waveforms are presented in Figures 5.17-5.19. It is obvious that they coincide with the simulation results to a large extent.

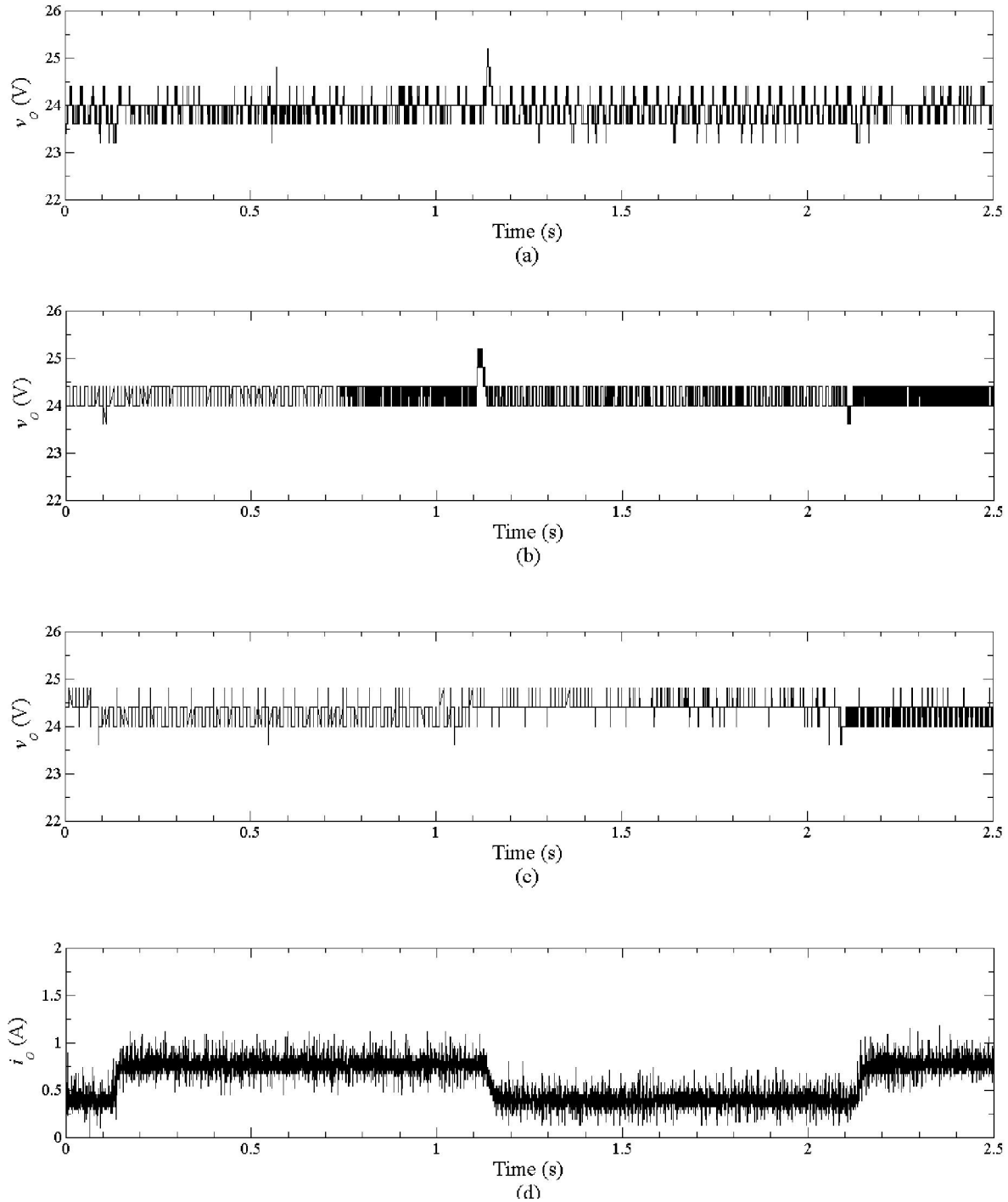


Figure 5.17 *Experimental waveforms of v_o (a-c) and i_o (d) of the boost converter with DSMC alternating between load resistance 68 Ω and 34 Ω and operating at V_i = 10.5 V (a), V_i = 12 V (b) and V_i = 13.5 V (c)*

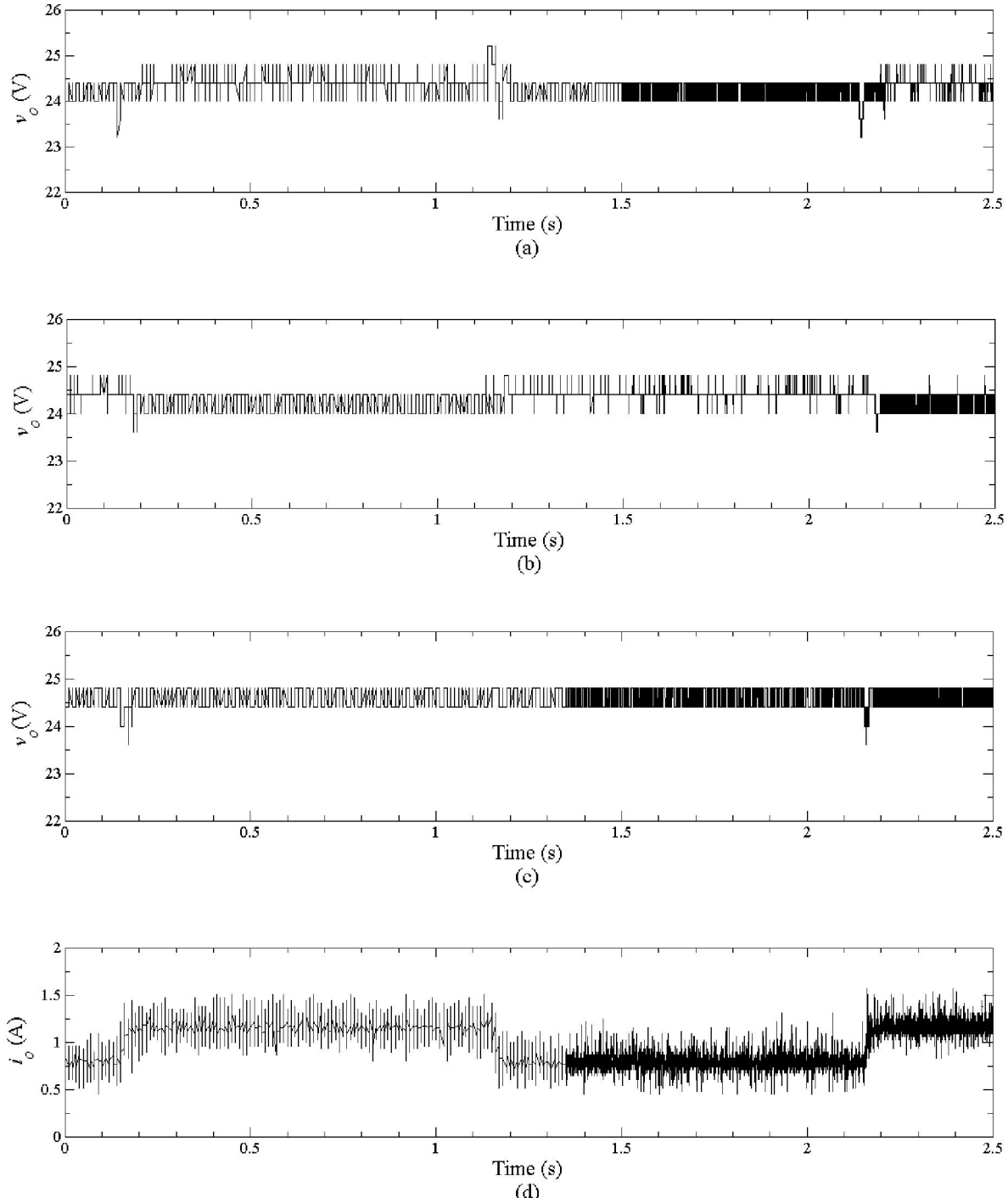


Figure 5.18 *Experimental waveforms of v_o (a-c) and i_o (d) of the boost converter with DSMC alternating between load resistance 34 Ω and 22.67 Ω and operating at V_i = 10.5 V (a), V_i = 12 V (b) and V_i = 13.5 V (c)*

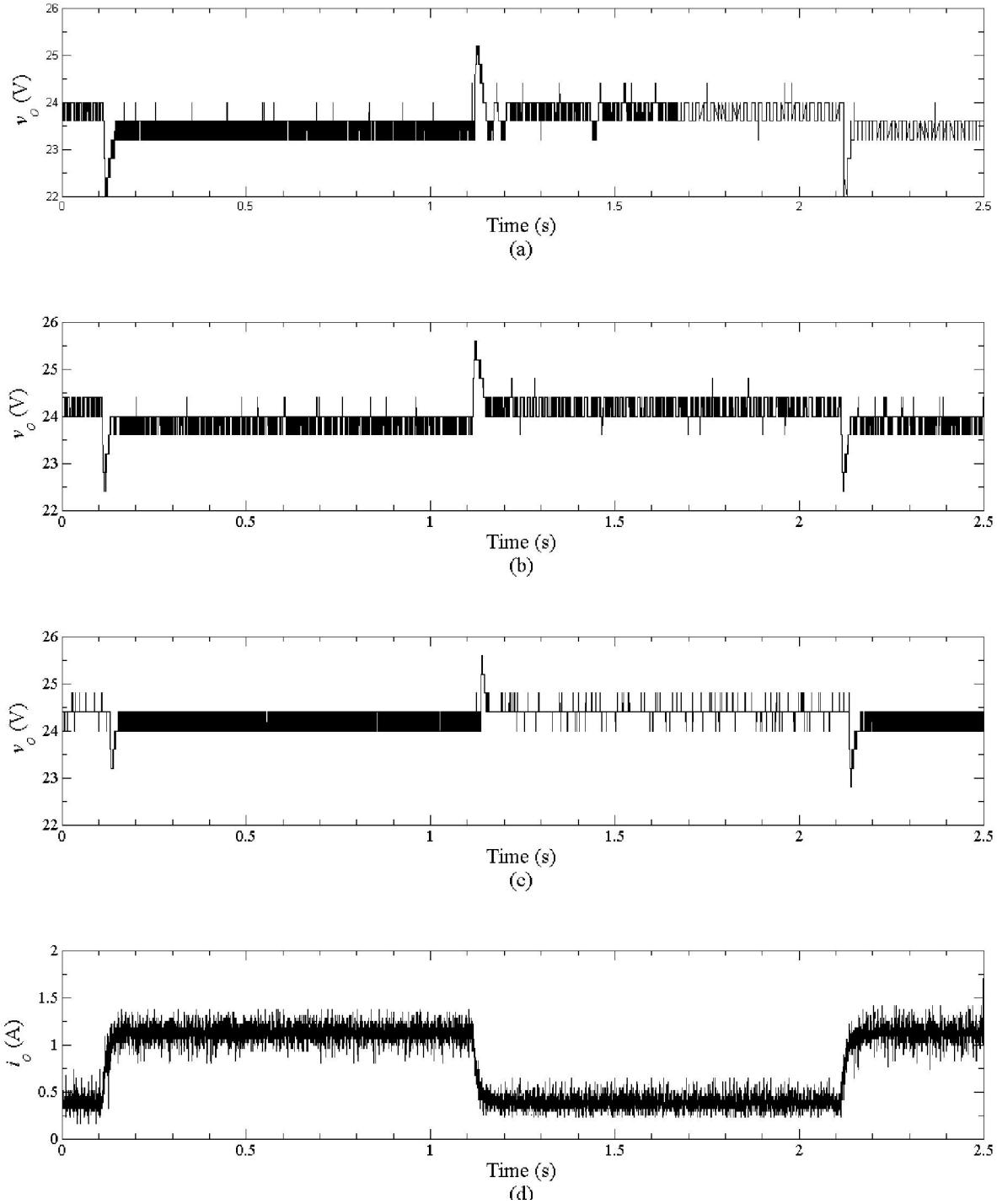
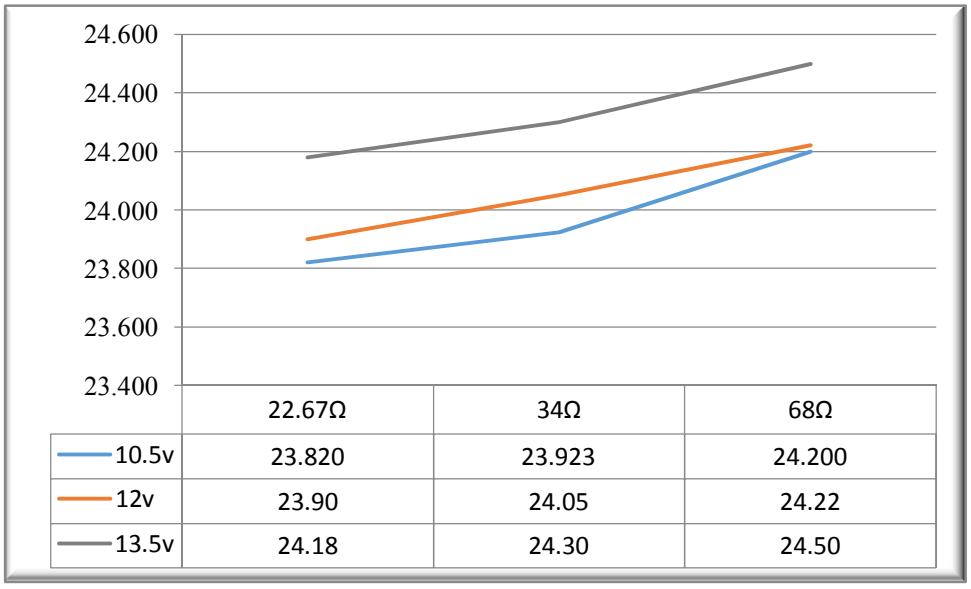


Figure 5.19 *Experimental waveforms of v_o (a-c) and i_o (d) of the boost converter with DSMC alternating between load resistance 68 Ω and 22.67 Ω and operating at V_i = 10.5 V (a), V_i = 12 V (b) and V_i = 13.5 V (c)*

According to Table 5.5, the maximum load regulation error occurs at V_i = 10.5 V with a deviation of 1.55% from v_o at the nominal condition. On the other hand, the maximum line regulation error is at the maximum load (R_L = 22.67 Ω) with a deviation of 2.9% from v_o at the nominal condition (see Table 5.6). It is worth noting that the load and line regulation properties depend largely on microcontroller's A/D converter and PWM resolution as well as on the choice of DSMC parameters $C(z^{-1})$, α and T. Theoretically, according to (5.7), the converter steady-state error should be approximately 400 mV. Therefore, a better accuracy may be expected if a faster microcontroller with better A/D converter and PWM resolution is used.



	22.67Ω	34Ω	68Ω
10.5v	23.820	23.923	24.200
12v	23.90	24.05	24.22
13.5v	24.18	24.30	24.50

Figure 5.20 *Plots of V_o against R_L for boost converter at a minimum, nominal and maximum V_i (DC values)*

Table 5.5 *Load regulation property ($V_{o\ (nominal\ condition}$ =23.9 V at V_i=12 V and R_{Lmin}= 22.67 Ω)*

V_i	$\Delta V_o = V_{o\ (68\ \Omega)} - V_{o(22.67\ \Omega)}$	$\frac{\Delta V_o}{V_{o(nominal\ condition)}} \times 100\%$
10.5 V	0.37 V	1.55 % of $V_{o\ (nominal\ condition)}$
12 V	0.32 V	1.32 % of $V_{o\ (nominal\ condition)}$
13.5 V	0.21 V	0.89 % of $V_{o\ (nominal\ condition)}$

Table 5.6 *Line regulation property ($V_{o\ (nominal\ condition)}$=23.9 V at V_i=12 V and R_{Lmin} = 22.67 Ω)*

Loading condition	$\Delta V_o = V_{o\ (Vi=13.5\ V)} - V_{o\ (Vi=10.5\ V)}$	$\frac{\Delta V_o}{V_{o(nominal\ condition)}} \times 100\%$
R_{L_max} = 68 Ω	0.4 V	1.67 % of $V_{o\ (nominal\ condition)}$
R_{L_med} = 34 Ω	0.3 V	1.25 % of $V_{o\ (nominal\ condition)}$
R_{L_min} = 22.67 Ω	0.7 V	2.90 % of $V_{o\ (nominal\ condition)}$

6 Concluding Remarks

DC-DC converters represent widespread electronic devices, which are used to convert one DC voltage level to another using various conversion methods where the most dominant ones nowadays are based on switching modes. The switching is achieved by using the appropriate controllers that provide a duty cycle of the switching element in the circuit, so that the DC component of the output voltage is equal to the desired reference value. The two most widely used topology of converters, buck (step-down) and boost (step-up) converters are considered in this Ph.D. dissertation.

Sliding mode control belongs to the class of nonlinear control known as variable structure control. The sliding mode occurs when control input forces the motion of system phase point towards a predetermined sliding surface, which is determined by a switching function and is of lower order reducing the system dynamics in that way. The system becomes robust to external disturbances and parameter variations. Because of these features, the sliding mode control techniques are chosen for the control of the converters herein. On the other hand, the switching control signal frequency of sliding mode control varies and this variation can lead to the significant losses in coils, as well as in transformer cores, producing electro-magnetic interference. That is why sliding mode control is combined with pulse-width-modulation control techniques, which are also known as duty cycle or pulse/pause control methods operating at fixed frequencies. The equivalence of the system dynamics with sliding mode control and pulse-width-modulation control is established, i.e., it is shown that sliding equivalent control u_{eq} is equal to the duty cycle control signal d.

The systematization and development of mathematical models, used in the process of designing control algorithms for DC-DC converters, have been conducted in the first place, as mathematical models of the converter define the paths to the development of various control strategies used for the practical realization of these devices. Therefore, particular attention has been paid to the analysis of different models of buck and boost converters. The aim was to perform the selection of that model that would be most appropriate for the development of unified solution for controlling these converters. Regardless of the primary form of converter design, all of them has been transformed into the form of the discrete-time transfer function.

However, the implementation of pulse-width-modulation techniques in control of DC-DC boost converter operating in continuous conduction mode causes the appearance of right-half-plane-zero in its duty-cycle-to-output-voltage transfer function, obtained on the basis of the

state-space average model of converter. This makes the design of boost converter voltage controller more difficult and limits the system bandwidth. Therefore, the digital sliding mode control based on generalized minimum variance control techniques is proposed in this dissertation to cope with this problem. Thanks to the presence of the generalized minimum variance control term, it is possible to handle the unstable zero dynamics of the boost converter. The combination of minimum variance control and digital sliding mode control is used to control a buck convertor since it is a minimum phase plant. The design of the suggested digital sliding mode control laws is based on the converter models given in the form of discrete-time transfer functions, so there is no need for additional current sensors since the control signal is calculated on the basis of measuring of converter output voltage.

Digital signal processors are traditionally used in the implementation of control for DC-DC converters. Lately, several researches have focused on designing cheaper solutions for voltage control of the converters. From this reason, the proposed digital sliding mode control algorithms have been realized on the standard and cheap 8-bit microcontroller ATmega8. Two laboratory prototypes have been developed, one for buck and another for boost converter, in order to validate the control solutions. The obtained experimental results are largely consistent with the simulation ones. One can conclude that the proposed digital sliding mode control algorithms for buck and boost converters give satisfactory results regarding the typical characteristics of these converters.

The further researches can be devoted to the implementation of the suggested digital sliding mode control laws in design of other types of DC-DC converters. The unified control approach to design of DC-DC converters with digital sliding mode control based on the average models should be also considered in the future investigations.

Contributions

This Ph.D. dissertation contains the following contributions.

- For the first time, the digital sliding mode control laws based on input-output models are implemented in design of DC-DC converters.
- Systematization of DC-DC converter models has been performed.
- The suggested control algorithms are universal and can be used for controlling different types of DC-DC converters.
- The direct output voltage control of DC-DC boost converter has been made possible despite of the unstable zero dynamics.
- It is not necessary to measure current so there is no need for additional current sensors.
- The proposed digital sliding mode control laws can be realized on the standard and cheap 8-bit microcontrollers.
- Laboratory prototypes of buck and boost converters have been practically developed.

Appendix A (The Proof of Theorem 5.2)

Let us prove that s_k enters the domain S in finite time and then show that s_k remains thereafter. Suppose that (s_k) defined by (5.14) is a positive sequence. The proof is similar when (s_k) is a negative sequence. Then:

$$s_{k+1} - s_k = -\alpha T + \frac{Q(z^{-1})}{B(z^{-1})}(y_{k+1} - y_k) < -\alpha T + \Lambda < 0 \tag{A.1}$$

is valid if (5.20) is fulfilled, i.e., $s_{k+1} < s_k$ and:

$$0 < \frac{s_{k+1}}{s_k} = q_k < 1. \tag{A.2}$$

There is a positive number δ fulfilling the following inequality:

$$|s_{k+1} - s_k| = \left| s_0 \left(\prod_{i=0}^{k-1} q_i \right)(q_k - 1) \right| < \delta, \tag{A.3}$$

as $\prod_{i=0}^{k-1} q_i < 1$ and $q_k < 1$. Therefore, based on Cauchy's theorem of sequence convergence, one can conclude that sequence (s_k) is convergent. The convergence domain of sequence (s_k) is:

$$\overline{S} = \{ s_k : |s_k| > \alpha T + \Lambda \}. \tag{A.4}$$

Namely, (A.2) implies:

$$0 < \left(\alpha T \operatorname{sgn}(s_k) - \frac{Q(z^{-1})}{B(z^{-1})}(y_{k+1} - y_k) \right) \Big/ s_k < 1 \tag{A.5}$$

directly giving (A.4) for both positive and negative sequence (s_k).

Let us show that system trajectory enters the domain S in finite time. The sequence (s_k) converges in the domain $\overline{S}$, so it is limited, i.e., $\lim_{k\to\infty} s_k = s_\infty$. Assume that $s_0 > \alpha T + \Lambda$ is fulfilled. According to (5.14):

$$s_k = s_0 - \sum_{i=0}^{k-1} \left(\alpha T - \frac{Q(z^{-1})}{B(z^{-1})}(y_{i+1} - y_i) \right). \tag{A.6}$$

Suppose that s_k never enters the domain S. When $k \to \infty$, the following inequality can be got straightforward from (A.6):

$$\sum_{i=0}^{\infty}\left(\alpha T-\frac{Q(z^{-1})}{B(z^{-1})}(y_{i+1}-y_i)\right)<s(0)-\alpha T-\Lambda \tag{A.7}$$

implying that the series $\sum_{i=0}^{\infty}\left(\alpha T-\left(Q(z^{-1})(y_{i+1}-y_i)\right)/B(z^{-1})\right)$ is convergent and its general element $\alpha T-\left(Q(z^{-1})(y_{i+1}-y_i)\right)/B(z^{-1})$ converges to zero as $i\to\infty$, i.e.:

$$\alpha T=\lim_{i\to\infty}\left(\frac{Q(z^{-1})}{B(z^{-1})}(y_{i+1}-y_i)\right), \tag{A.8}$$

which is opposite to the condition (5.20) of Theorem 5.2. Therefore, the assumption that s_k never enters the domain S is false. The proof is similar for $s_0<-\alpha T-\Lambda$. Moreover, s_k enters the domain S at $k=K_0$ determined by:

$$K_0=\operatorname{int}\left(\left(|s_0|-\alpha T-\Lambda\right)/\left(\alpha T-\Lambda\right)\right)+1. \tag{A.9}$$

It will be now shown that for every $k>K_0$, s_k remains in the domain S. Let $s_{K_0}\in S^{+}=\{s_k:0<s_k<\alpha T+\Lambda\}$. Then, according to (5.14), one can have:

$$-\alpha T-\Lambda \underset{(5.20)}{<} s_{K_0}-\alpha T+\frac{Q(z^{-1})}{B(z^{-1})}(y_{K_0+1}-y_{K_0})=s_{K_0+1}\underset{(5.20)}{<}2\Lambda\underset{(5.20)}{<}\alpha T+\Lambda \tag{A.10}$$

and s_k does not leave the domain S. This is also true when $s_{K_0}\in S^{-}=\{s_k:-\alpha T-\Lambda<s_k<0\}$ since:

$$-\alpha T-\Lambda \underset{(5.20)}{<} -2\Lambda \underset{(5.20)}{<} s_{K_0+1}=s_{K_0}+\alpha T+\frac{Q(z^{-1})}{B(z^{-1})}(y_{K_0+1}-y_{K_0})\underset{(5.20)}{<}\alpha T+\Lambda. \tag{A.11}$$

The case when $s_{K_0+1}<0$ and $s_{K_0+1}\notin S$ for $s_0,s_{K_0}>\alpha T+\Lambda$ is not possible as:

$$s_{K_0+1}=s_{K_0}-\alpha T+\frac{Q(z^{-1})}{B(z^{-1})}(y_{K_0+1}-y_{K_0})>\Lambda+\frac{Q(z^{-1})}{B(z^{-1})}(y_{K_0+1}-y_{K_0})>0. \tag{A.12}$$

The case when $s_{K_0+1}>0$ and $s_{K_0+1}\notin S$ for $s_0,s_{K_0}<-\alpha T-\Lambda$ cannot happen as well, since:

$$s_{K_0+1}=s_{K_0}+\alpha T+\frac{Q(z^{-1})}{B(z^{-1})}(y_{K_0+1}-y_{K_0})<-\Lambda+\frac{Q(z^{-1})}{B(z^{-1})}(y_{K_0+1}-y_{K_0})<0. \tag{A.13}$$

Therefore, $s_{K_0+1}\in S$ has been proven and using the mathematical induction method one can generalize it to:

$$s_{K_0+p}\in S \tag{A.14}$$

for every positive integer number p. Having demonstrated that (A.14) is fulfilled if (5.20) is valid, the proof ends.

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Curriculum Vitae

Muhanad Dheyaa Hashim Almawlawe was born on 13.12.1962. in Baghdad, Republic of Iraq. He is married and father of five children. He finished the elementary school ("Al Kholud", 1968-1974), the high school ("Al Etifija", 1974-1978) and the secondary school ("Al Etifija", 1978-1981) in Baghdad. In 1982/83 year, he enrolled the Air Force Technical Military Academy in Rajlovac (former Yugoslavia), major in Electronics. He graduated on July 19th, 1985 with the average grade of 9,545 during the study and obtained the professional title of a Military Aviation Electrical Engineer. The same year, 1985, he enrolled at the School of Electrical Engineering, University of Belgrade. On November 6th, 1987, he graduated both on the Department of Electronics, School of Electrical Engineering, University of Belgrade and on the Air Force Technical Military Academy, with the average grade of 7.22 and the grade 9 on the final exam. He became a graduated electrical and military aero engineer.

From 1988 until 2003, he was being employed as a professional officer in the previous army of Republic of Iraq as a radar engineer. In the period from 2007 to 2012, he was working as an assistant at the Engineering Faculty, University of Al-Qadisiyah in Iraq. He is the author or coauthor of 12 scientific papers published in the international journals and presented at the international conferences.

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a) Papers published in the international journals from SCI(e) list

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b) Papers published in the international journals verified by the special decision

b.1 **Muhanad D. Almawlawe**, Darko Mitić, "An Approach to Design of DC-DC Boost Converter With Digital Control," *Facta Universities, Series: Automatic Control and Robotics, Accepted for publication,* 2017. **(M24)**

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c.3 **Muhanad D. Almawlawe**, Darko Mitić, Marko Milojković, "The usage of the digital controller in regulating boost converter", *Circuits and Systems*, vol. 6, no. 12, (2015), pp. 268-279, Print ISSN**:** 2153-1285, (DOI: http://dx.doi.org/10.4236/cs.2015.612027), *Publisher: Scientific Research Publishing*. **(M52)**

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Faculty of Mechanical Engineering - Niš, SAUM – Association of Serbia for Systems, Automatic Control and Measurements, Serbia. **(M33)**

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