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The investigation of electro physical properties of sic and its application in Nanoelectronic devices

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Beograd, decembar 2013. g.

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Abstract:

The emergence of silicon carbide (SiC) based power semiconductor switches with their superior features compared with silicon (Si) based switches has resulted in substantial improvements in the performance of power electronics converter systems. These systems with SiC power devices are more compact, lighter, and more efficient, so they are ideal for high-voltage power electronics applications including hybrid electric vehicle (HEV) power converters.

In this dissertation, first In this section we studied physically based improvement of the analytical model for a vertical double implanted metal-oxide-semiconductor (DIMOS) transistor in 4H-Silicon Carbide (4H-SiC) is suggested. Special attention has been paid to its vertical section, i.e. to its geometrical profile. The answer to the question where this vertical region starts narrowing and how abruptly it happens has been found exploiting some fundamental principles of physics. This has made possible to considerably reduce the number of free parameters appearing in the construction of current-voltage characteristics.

In recent years, studies about Dual- Material Surrounding-Gate (DMSG) transistor have successively been proposed, and have attached a lot of attention. For future ULSI′S design, it is shown that Dual- Material Surrounding-Gate (DMSG) transistor have the following advantages, such as: reduced reduced short channel effects (SCEs), high packing density, high-speed cut-off frequency, low-power consumption, the application of Stacked circuit design, the excellent gate control ability over the channel and reduced fringe-induced barrier lowering (FIBL). To apply the device to the simulation, it is necessary to develop an analytical 2D model to predict precisely the performance of the Dual- Material Surrounding-Gate (DMSG) transistor MOSFETs.

On the basis of fully solution of two dimensional Poisson′s equation, a new two dimensional model including channel potential, threshold voltage, subthreshold swing and subthreshold current for Dual- Material Surrounding-Gate (DMSG) MOSFETs is successfully developed. The new model is verified by published numerical simulations with a close agreement. This model can be applied for SPISE simulation because of its efficient computation.

Sažetak :

Pojava silikon karbid (SiC) na bazi poluprovodničkih prekidača snage sa svojim superiornim karakteristikama u poređenju sa silicijuma (Si) na prekidačima rezultirao je značajnim poboljšanjima u obavljanju energetske elektronike konvertora sistema . Ovi sistemi sa SiC energije uređaja su kompaktniji , lakši i efikasniji , tako da su idealni za aplikacije visokog napona energetske elektronike , uključujući hibridnih električnih električnih vozila (HEV) energetskih pretvarača .

U ovoj disertaciji , prvi u ovom delu smo proučavali fizički zasnovan poboljšanje analitičkog modela za vertikalne dvostruke implanta metal - oksid - poluprovodnika (DIMOS) tranzistora u 4H - silikon karbid (SiC - 4H) je predložio . Posebna pažnja je posvećena vertikalnom delu , odnosno njegovog geometrijskog profila . Odgovor na pitanje gde se to vertikalna regionu počinje naglo sužava i kako se to desi je pronađen eksploatišu neke osnovne principe fizike . Ovo je omogućeno da znatno smanji broj slobodnih parametara koji se pojavljuju u izgradnji struje napona karakteristikama.

U poslednjih nekoliko godina , studija o dual - materijala Okolna - kapija (DMSG) tranzistora su sukcesivno su predložili , a imaju ugrađene dosta pažnje . Za projektovanje budućeg ULSI 'S , pokazuje se da dual - Materijal Okolna - kapija (DMSG) tranzistora imaju sledeće prednosti , kao što su : smanjenje snižene kratkih kanala efekti (SCEs) , visok Gustina pakovanja , velike brzine prekidne frekvencije , niske potrošnja energije ,primena naslagane kola dizajn,odličan kapija kontrola nad kanalom sposobnosti i smanjenja Fringe indukovane spuštanje barijera (FIBL) . Da biste primenili uređaj za simulaciju , neophodno je razviti analitički 2D model da precizno predvideti učinak dual - materijala Okolna - Gate (DMSG) MOSFET tranzistora .

Na osnovu potpuno rešenje jednačine dvodimenzionalna Poisson'ov ,novi dvodimenzionalni model sa kanala , potencijal napon praga , subthreshold ljuljaška i subthreshold tekuće za Dual -materijal okolnih -Gate (DMSG) MOSFET se uspešno razvija . Novi model je verifikovan od strane objavljuje numeričke simulacije sa bliskim sporazuma . Ovaj model se može primeniti za simulaciju SPISE zbog efikasnog računanja

Contents:

Part one:

General Features of Si MOSFET physics. The influence of geometrical and technological parameters on device operations regions. The special attention should be paid to Si crystal lattice and intrinsic parameters originating from it.

1.1 INTRODUCTION:

A field effect transistor (FET) operates as a conducting semiconductor channel with two ohmic contacts – the *source* and the *drain* – where the number of charge carriers in the channel is controlled by a third contact – the *gate*. In the vertical direction, the gatechannel-substrate structure (gate junction) can be regarded as an orthogonal two-terminal device, which is either a MOS structure or a reverse-biased rectifying device that controls the mobile charge in the channel by capacitive coupling (field effect). Examples of FETs based on these principles are metal-oxide-semiconductor FET (MOSFET), junction FET (JFET), metal-semiconductor FET (MESFET), and heterostructure FET (HFETs) [1]. In all cases, the stationary gate-channel impedance is very large at normal operating conditions. The basic FET structure is shown schematically in Figure 1.1.

The most important FET is the MOSFET. In a silicon MOSFET, the gate contact is separated from the channel by an insulating silicon dioxide (SiO_2) layer. The charge carriers of the conducting channel constitute an inversion charge, that is, electrons in the case of a *p*-type substrate (*n*-channel device) or holes in the case of an *n*-type substrate (*p*-channel device), induced in the semiconductor at the silicon-insulator interface by the voltage applied to the gate electrode. The electrons enter and exit the channel at n^+ source and drain contacts in the case of an *n*-channel MOSFET, and at p+contacts in the case of a *p*-channel MOSFET.

MOSFETs are used both as discrete devices and as active elements in digital and analog monolithic integrated circuits (ICs). In recent years, the device feature size of such circuits has been scaled down into the deep submicrometer range. Presently, the 0.13-μm technology node for complementary MOSFET (CMOS) is used for very large scale ICs (VLSIs) and, within a few years, sub-0.1-μm technology will be available, with a commensurate increase in speed and in integration scale. Hundreds of millions of transistors on a single chip are used in microprocessors and in memory ICs today.

CMOS technology combines both *n*-channel and *p*-channel MOSFETs to provide very low power consumption along with high speed. New silicon-on-insulator (SOI) technology may help achieve three-dimensional integration, that is, packing of devices into many layers,

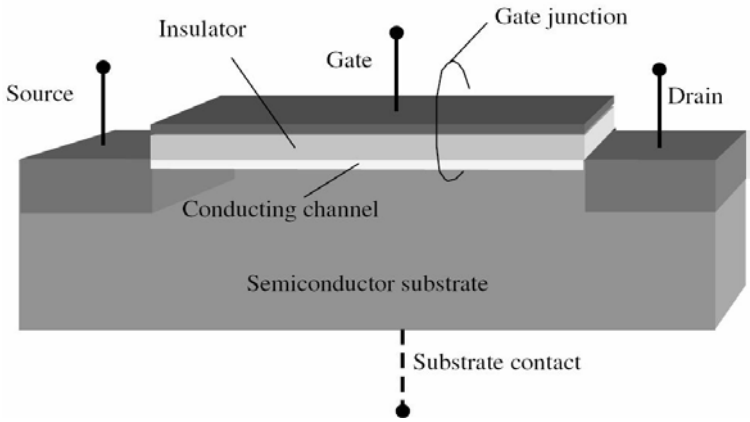


Figure 1.1 Schematic illustration of a generic field effect transistor. This device can be viewed as a combination of two orthogonal two-terminal devices.

with a dramatic increase in integration density. New improved device structures and the combination of bipolar and field effect technologies (BiCMOS) may lead to further advances, yet unforeseen. One of the rapidly growing areas of CMOS is in analog circuits, spanning a variety of applications from audio circuits operating at the kilohertz (kHz) range to modern wireless applications operating at gigahertz (GHz) frequencies [2].

1.2 THE MOS CAPACITOR

To understand the MOSFET, we first have to analyze the MOS capacitor, which constitutes the important gate-channel-substrate structure of the MOSFET. The MOS capacitor is a two-terminal semiconductor device of practical interest in its own right. As indicated in Figure 1.2, it consists of a metal contact separated from the semiconductor by a dielectric insulator. An additional ohmic contact is provided at the semiconductor substrate. Almost universally, the MOS structure utilizes doped silicon as the substrate and its native oxide, silicon dioxide, as the insulator[3-4]. In the silicon–silicon dioxide system, the density of surface states at the oxide–semiconductor interface is very low compared
to the typical channel carrier density in a MOSFET. Also, the insulating quality of the oxide is quite good.

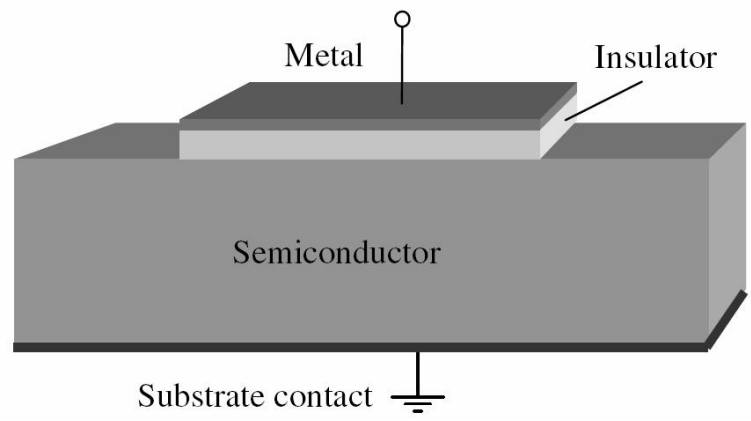


Figure 1.2 Schematic view of a MOS capacitor

We assume that the insulator layer has infinite resistance, preventing any charge carrier transport across the dielectric layer when a bias voltage is applied between the metal and the semiconductor. Instead, the applied voltage will induce charges and counter charges in the metal and in the interface layer of the semiconductor, similar to what we expect in the metal plates of a conventional parallel plate capacitor. However, in the MOS capacitor we may use the applied voltage to control the type of interface charge we induce in the semiconductor – majority carriers, minority carriers, and depletion charge [3].

Indeed, the ability to induce and modulate a conducting sheet of minority carriers at the semiconductor–oxide interface is the basis for the operation of the MOSFET.

1.2.1 Interface Charge

The induced interface charge in the MOS capacitor is closely linked to the shape of the electron energy bands of the semiconductor near the interface. At zero applied voltage, the bending of the energy bands is ideally determined by the difference in the work functions of the metal and the semiconductor. This band bending changes with the applied bias and the bands become flat when we apply the so-called flat-band voltage given by

$$V_{FB} = (\emptyset_m - \emptyset_s)/q = (\emptyset_m - X_s - E_c + E_F)/q, \qquad (1.1)$$

where $\emptyset_m$ and $\emptyset_s$ are the work functions of the metal and the semiconductor, respectively, X_s is the electron affinity for the semiconductor, E_c is the energy of the conduction band edge, and E_F is the Fermi level at zero applied voltage. The various energies involved are

indicated in Figure 1.3, where we show typical band diagrams of a MOS capacitor at zero bias, and with the voltage $V = V_{FB}$ applied to the metal contact relative to the semiconductor–oxide interface. (Note that in real devices, the flat-band voltage may be

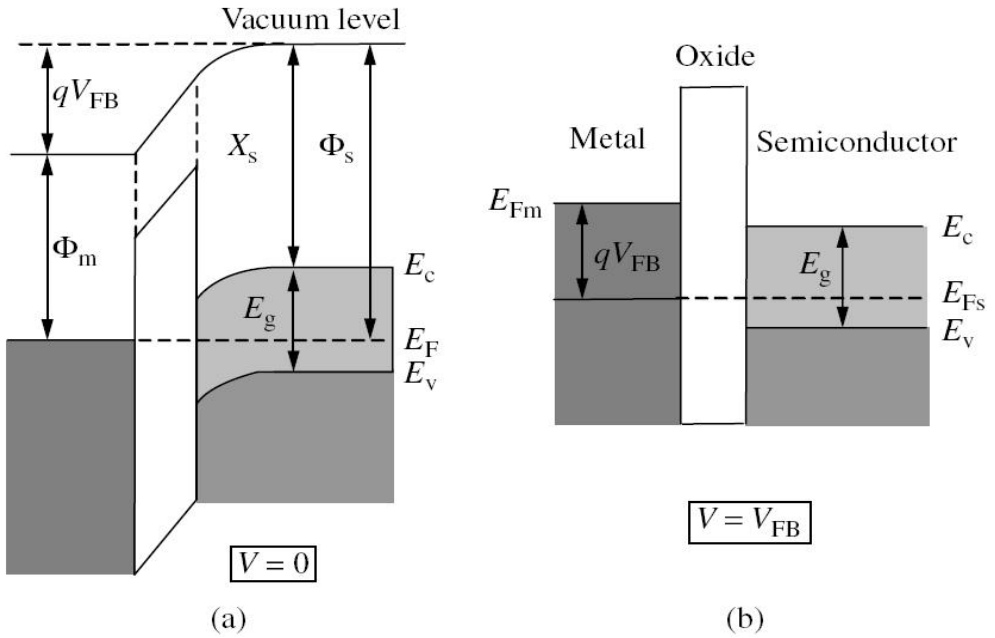


Figure 1.3 Band diagrams of MOS capacitor (a) at zero bias and (b) with an applied voltage equal to the flat-band voltage. The flat-band voltage is negative in this example affected by surface states at the semiconductor–oxide interface and by fixed charges in the insulator layer [6].

At stationary conditions, no net current flows in the direction perpendicular to the interface owing to the very high resistance of the insulator layer. Hence, the Fermi level will remain constant inside the semiconductor, independent of the biasing conditions. However, between the semiconductor and the metal contact, the Fermi level is shifted by $E_{FM} - E_{Fs}$ =qV (see Figure 1.3(b)). Hence, we have a quasi-equilibrium situation in which the semiconductor can be treated as if in thermal equilibrium.

A MOS structure with a p-type semiconductor will enter the *accumulation* regime of operation when the voltage applied between the metal and the semiconductor is more negative than the flat-band voltage (V_{FB}< 0 in Figure 1.3). In the opposite case, when $V > V_{FB}$, the semiconductor–oxide interface first becomes depleted of holes and we enter the so-called *depletion* regime. By increasing the applied voltage, the band bending becomes so large that the energy difference between the Fermi level and the bottom of the conduction band at the insulator–semiconductor interface becomes smaller than that between the Fermi level and the top of the valence band. This is the case indicated for V= 0V in Figure 1.3(a).

Carrier statistics tells us that the electron concentration then will exceed the hole concentration near the interface and we enter the *inversion* regime. At still larger applied voltage, we finally arrive at a situation in which the electron volume concentration at the interface exceeds the doping density in the semiconductor. This is the strong inversion case in which we have a significant conducting sheet of inversion charge at the interface [7].

The symbol ψ is used to signify the potential in the semiconductor measured relative to the potential at a position x deep inside the semiconductor. Note that ψ becomes positive when the bands bend down, as in the example of a $p-type$ semiconductor shown in Figure 1.4. From equilibrium electron statistics, we find that the intrinsic Fermi level E_i in the bulk corresponds to an energy separation $q\varphi_b$ from the actual Fermi level E_F of the doped $semiconductor,$

$$\varphi_b = V_{th} \ln\left(\frac{N_a}{n_i}\right), \qquad (1.2)$$

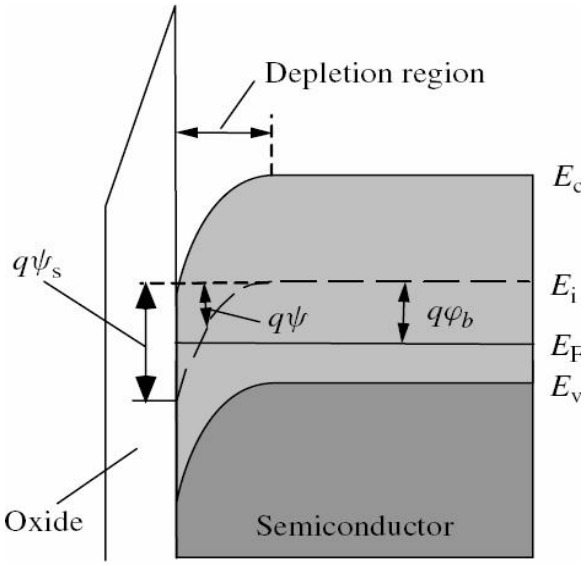


Figure 1.4 Band diagram for MOS capacitor in weak inversion($\varphi_b < \psi_s < 2\varphi_b$)

where V_{th} is the thermal voltage, N_a is the shallow acceptor density in the *p*-type semiconductor and n_i is the intrinsic carrier density of silicon. According to the usual definition, strong inversion is reached when the total band bending equals $2q\varphi_b$, corresponding to the surface potential$\psi_s = 2\varphi_b$. Values of the surface potential such that $0 < \psi_s < 2\varphi_b$ correspond to the depletion and the weak inversion regimes, ψ_s = 0 is the flat-band condition, and ψ_s< 0 corresponds to the accumulation mode.

The surface concentrations of holes and electrons are expressed in terms of the surface potential as follows using equilibrium statistics,

$P_s = N_A exp(-\psi_s/V_{th})$, (1.3)

$n_s = n_i^2/p_s = n_{po} exp(\psi_s/V_{th})$, (1.4)

Where $n_{PO} = n_i^2/N_A$ is the equilibrium concentration of the minority carriers (electrons) in the bulk.

The potential distribution $\psi(x)$ in the semiconductor can be determined from a solution of the one-dimensional Poisson's equation:

$\frac{d^2 \phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_s}$, (1. 5)

where ε_s is the semiconductor permittivity, and the space charge density $\rho(x)$ is given by

$$\rho(x) = q(p - n - N_A). \quad (1.6)$$

The position-dependent hole and electron concentrations may be expressed as

$p(x) = N_A exp(-\psi/V_{th})$, (1.7)

$n = n_{PO} exp(-\psi/V_{th})$. (1.8)

Note that deep inside the semiconductor, we have $\psi(\infty) = 0$.

In general, the above equations do not have an analytical solution for $\phi(x)$. However, the following expression can be derived for the electric field F_s at the insulator semiconductor interface, in terms of the surface potential [8].

$F_s = \sqrt{2}\frac{V_{th}}{L_{DP}} f(\frac{\psi_s}{V_{th}})$, (1. 9)

where the function f is defined by

$f(u) = \pm\sqrt{[\exp(-u) + u - 1] + \frac{n_{PO}}{V_{th}}[\exp(-u) + u - 1]}$, (1. 10)

$L_{DP} = \sqrt{\frac{\varepsilon_s V_{th}}{qN_A}}$ (1. 11)

is called the Debye length. In (1.10), a positive sign should be chosen for a positive ψ_s and a negative sign corresponds to a negative ψ_s.

Using Gauss' law, we can relate the total charge Q_s per unit area (carrier charge and depletion charge) in the semiconductor to the surface electric field by

$Q_s = -\varepsilon_s F_s$. (1.12)

At the flat-band condition (V = V_{FB}), the surface charge is equal to zero. In accumulation ($V < V_{FB}$), the surface charge is positive, and in depletion and inversion ($V > V_{FB}$), the surface charge is negative. In accumulation (when $|\psi_S|$ exceeds a few times V_{th}) and in strong inversion, the mobile sheet charge density is proportional to $\exp[|\psi_S|/(2V_{th})]$.

In depletion and weak inversion, the depletion charge is dominant and its sheet density varies as $\psi_s^{1/2}$. Figure 1.5 shows $|Q_s|$ versus ψ_s for $p-type$ silicon with a doping density of $10^{16}/cm^3$.

In order to relate the semiconductor surface potential to the applied voltage V, we have to investigate how this voltage is divided between the insulator and the semiconductor. Using the condition of continuity of the electric flux density at the semiconductor–insulator interface, we find

$$\varepsilon_s F_s = \varepsilon_i F_i \,, \qquad (1.13)$$

Where ε_i is the permittivity of the oxide layer and F_i is the constant electric field in the insulator (assuming no space charge). Hence, with an insulator thickness d_i, the voltage drop across the insulator becomes $F_i d_i$. Accounting for the flat-band voltage, the applied voltage can be written as

$$V = V_{FB} + \psi_S + \frac{\varepsilon_S F_S}{c_i}, \qquad (1.14)$$

Where $c_i = \varepsilon_i / d_i$ is the insulator capacitance per unit area.

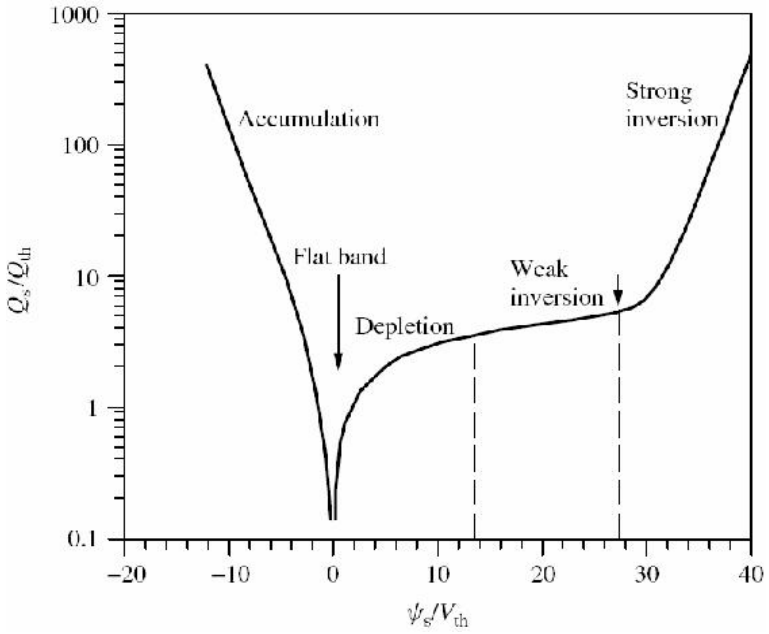


Figure 1.5 Normalized total semiconductor charge per unit area versus normalized surface potential for *p*-type Si with $N_A = 10^{16}/cm^3$. $Q_{th} = (2\varepsilon_S q N_A V_{th})^{1/2} \approx 9.3 \times 10^{-9}$ C/cm^2 and $V_{th} \approx 0.026$V at $T = 300$ K. The arrows indicate flat-band condition and onset of strong inversion .

1.2.2 Threshold Voltage:

The threshold voltage $V = V_T$, corresponding to the onset of the strong inversion, is one of the most important parameters characterizing metal-insulator-semiconductor devices.

As discussed above, strong inversion occurs when the surface potential ψ_s becomes equal to $2\varphi_b$. For this surface potential, the charge of the free carriers induced at the insulator–semiconductor interface is still small compared to the charge in the depletion layer, which is given by

$$Q_{dT} = -qN_A d_{dT} = -\sqrt{4\varepsilon_s q N_A \varphi_b} \ . \qquad (1.15)$$

Where: $d_{dT} = (4\varepsilon_s \varphi_b / qN_A)^{1/2}$ is the width of the depletion layer at threshold. Accordingly, the electric field at the semiconductor–insulator interface becomes

$$F_{sT} = -Q_{dT}/\varepsilon_s = \sqrt{4qN_A\varphi_b/\varepsilon_s} \ . \qquad (1.16)$$

Hence, substituting the threshold values of $\emptyset_s$ and F_s in (1.14), we obtain the following expression for the threshold voltage:

$$V_T = V_{FB} + 2\varphi_b + \sqrt{4\varepsilon_s q N_a \varphi_b}/c_i \ . \qquad (1.17)$$

Figure 1.6 shows typical calculated dependencies of V_T on doping level and dielectric thickness.

For the MOS structure shown in Figure 1.2, the application of a bulk bias V_B is simply equivalent to changing the applied voltage from V to $V - V_B$. Hence, the threshold

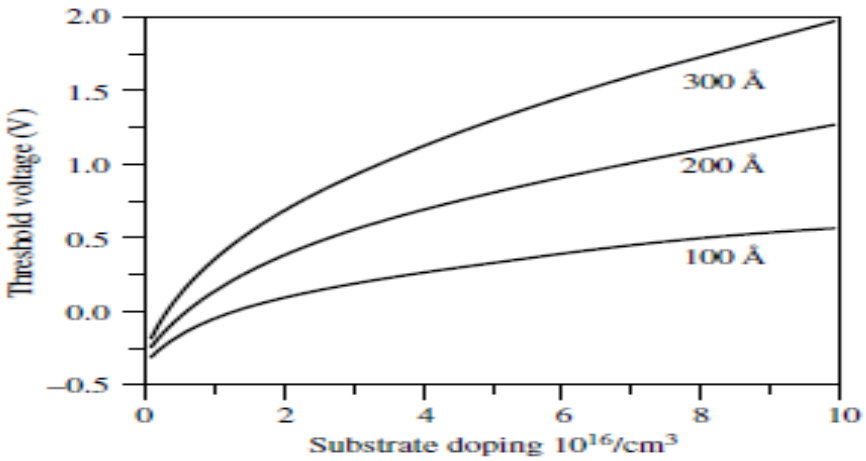


Figure 1.6 Dependence of MOS threshold voltage on the substrate doping level for different thicknesses of the dielectric layer. Parameters used in calculation: energy gap, 1.12 eV; effective density of states in the conduction band, $3.22\times10^{25}/m^3$; effective density of states in the valence band, $1.83\times10^{25}/m^3$; semiconductor permittivity, 1.05×10^{-10} F/m; insulator permittivity, 3.45×10^{-10}F/m; flat-band voltage, −1V; temperature: 300 K [9].

referred to the ground potential is simply shifted by V_B. However, the situation will be different in a MOSFET where the conducting layer of mobile electrons may be maintained at

some constant potential. Assuming that the inversion layer is grounded, V_B biases the effective junction between the inversion layer and the substrate, changing the amount of charge in the depletion layer. In this case, the threshold voltage becomes

$$V_T = V_{FB} + 2\varphi_b + \sqrt{2\varepsilon_s N_A(2\varphi_b - V_B)}/C_i \,. \qquad (1.18)$$

Note that the threshold voltage may also be affected by so-called fast surface states at the semiconductor–oxide interface and by fixed charges in the insulator layer. However, this is not a significant concern with modern day fabrication technology [10-11].

As discussed above, the threshold voltage separates the sub threshold regime, where the mobile carrier charge increases exponentially with increasing applied voltage, from the above-threshold regime, where the mobile carrier charge is linearly dependent on the applied voltage. However, there is no clear point of transition between the two regimes, so different definitions and experimental techniques have been used to determine and extract V_T. Sometimes (1.17) and (1.18) are taken to indicate the onset of so-called moderate inversion, while the onset of strong inversion is defined to be a few thermal voltages higher.

1.2.3 MOS Capacitance:

In a MOS capacitor, the metal contact and the neutral region in the doped semiconductor substrate are separated by the insulator layer, the channel, and the depletion region. Hence, the capacitance C_{mos} of the MOS structure can be represented as a series connection of the insulator capacitance $C_i = S\,\varepsilon_i/d_i$, where S is the area of the MOS capacitor, and the capacitance of the active semiconductor layer C_s,

$$c_{mos} = \frac{c_i c_s}{c_i + c_s} \,. \qquad (1.19)$$

The semiconductor capacitance can be calculated as

$$c_s = S\left|\frac{dQ_s}{d\,\phi_s}\right|, \qquad (1.20)$$

Where Q_s is the total charge density per unit area in the semiconductor and ϕ_s is the surface potential. Using (1.9) to (1.12) for Qs and performing the differentiation, we obtain

$$c_s = \frac{c_{os}}{\sqrt{2}f(\frac{\phi_s}{V_{th}})}\left\{1 - \exp\left(\frac{\phi_s}{V_{th}}\right) + \frac{n_{PO}}{N_A}\left[\!\left[\exp\left(\frac{\phi_s}{V_{th}}\right) - 1\right]\!\right]\right\}. \qquad (1.21)$$

Here, $C_s = S\varepsilon_s/LD_P$ is the semiconductor capacitance at the flat-band condition (i.e.,

For $\phi_S = 0$) and L_{DP} is the Debye length given by (1.11). Equation (1.14) describes the relationship between the surface potential and the applied bias [12-14].

The semiconductor capacitance can formally be represented as the sum of two capacitances– a depletion layer capacitance C_d and a free carrier capacitance c_{fc}. c_{fc} together with a series resistance R_{GR} describes the delay caused by the generation/recombination mechanisms in the buildup and removal of inversion charge in response to changes in the bias voltage (see following text). The depletion layer capacitance is given by

$$C_d = S\varepsilon_s/d_d\,, \qquad (1.22)$$

Where

$$d_d=\sqrt{\frac{2\varepsilon_s\,\phi_s}{qN_A}} \qquad (1.23)$$

is the depletion layer width. In strong inversion, a change in the applied voltage will primarily affect the minority carrier charge at the interface, owing to the strong dependence of this charge on the surface potential [13]. This means that the depletion width reaches a maximum value with no significant further increase in the depletion charge. This maximum depletion width d_{dT} can be determined from (1.23) by applying the threshold condition, $\phi_s = 2\varphi_b$.The corresponding minimum value of the depletion capacitance is $C_{dT}= S.\varepsilon_s/d_{dT}$. The free carrier contribution to the semiconductor capacitance can be formally expressed as

$$c_{fc} = c_s - c_d. \qquad (1.24)$$

As indicated, the variation in the minority carrier charge at the interface comes from the processes of generation and recombination mechanisms, with the creation and removal of electron–hole pairs. Once an electron–hole pair is generated, the majority carrier (a hole in $p-$type material and an electron in $n-$type material) is swept from the space charge region into the substrate by the electric field of this region. The minority carriers are swept in the opposite direction toward the semiconductor–insulator interface. The variation in minority carrier charge at the semiconductor–insulator interface therefore proceeds at a rate limited by the time constants associated with the generation/recombination processes. This finite rate represents a delay, which may be represented electrically in terms of an RC product consisting of the capacitance C_{fc} and the resistance R_{GR}, as reflected in the equivalent circuit of the MOS structure shown in Figure 1.7. The capacitance C_{fc} becomes important in the inversion regime, especially in strong inversion where the mobile charge is important. The resistance R_s in the equivalent circuit is the series resistance of the neutral semiconductor layer and the contacts.

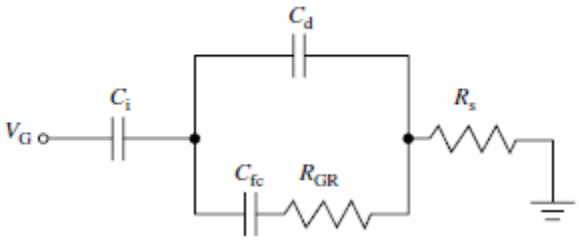


Figure 1.7 Equivalent circuit of the MOS capacitor [15].

This equivalent circuit is clearly frequency-dependent. In the low-frequency limit, we can neglect the effects of R_{GR} and R_s to obtain (using $C_s = C_d + C_{fc}$)

$$c_{mos}^{o} = \frac{c_s c_i}{c_s + c_i}. \tag{1.25}$$

In strong inversion, we have $C_s \ll C_i$ which gives

$$c_{mos}^{o} \approx c_i \tag{1.26}$$

at low frequencies.

In the high-frequency limit, the time constant of the generation/recombination mechanism will be much longer than the signal period ($R_{GR}C_{fc} \gg 1/f$) and C_d effectively shunts the lower branch of the parallel section of the equivalent in Figure 1.7. Hence, the high-frequency, strong inversion capacitance of the equivalent circuit becomes

$$c_{mos}^{\infty} = \frac{c_{dT} c_i}{c_s + c_i}. \tag{1.27}$$

The calculated dependence of C_{mos} on the applied voltage for different frequencies is shown in Figure 1.8. For applied voltages well below threshold, the device is in accumulation and C_{mos} equals c_i. As the voltage approaches threshold, the semiconductor passes the flat-band condition where C_{mos} has the value C_{FB}, and then enters the depletion and the weak inversion regimes where the depletion width increases and the capacitance value drops steadily until it reaches the minimum value at threshold given by (1.27). The calculated curves clearly demonstrate how the MOS capacitance in the strong inversion regime depends on the frequency, with a value of c_{mos}^{∞} at high frequencies to c_i at low frequencies.

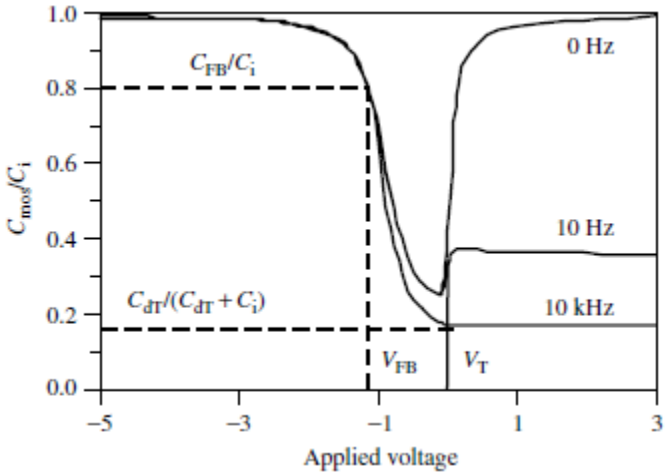


Figure 1.8 Calculated dependence of c_{mos} on the applied voltage for different frequencies. Parameters used: insulator thickness, 2×10^{-8} m; semiconductor doping density, $10^{15}/cm^3$; generation time, 110^{-8} s [15].

We note that in a MOSFET, where the highly doped source and drain regions act as reservoirs of minority carriers for the inversion layer, the time constant $R_{GR}C_{fc}$ must be substituted by a much smaller time constant corresponding to the time needed for transporting carriers from these reservoirs to get in and out of the MOSFET gate area. Consequently, high-frequency strong inversion MOSFET gate-channel $C-V$ characteristics will resemble the zero frequency MOS characteristic [16].

Since the low-frequency MOS capacitance in the strong inversion is close to C_i, the induced inversion charge per unit area can be approximated by

$$qn_s \approx c_i(V - V_T). \qquad (1.28)$$

The equation (1.28) serves as the basis of a simple charge control model (SCCM) allowing us to calculate MOSFET current–voltage characteristics in strong inversion.

From measured MOS $C-V$ characteristics, we can easily determine important parameters of the MOS structure, including the gate insulator thickness, the semiconductor substrate doping density, and the flat-band voltage. The maximum measured capacitance C_{max} (capacitance c_i in Figure 1.7) yields the insulator thickness

$$d_i \approx S\varepsilon_s/c_{dT}. \qquad (1.29)$$

The minimum measured capacitance c_{min} (at high frequency) allows us to find the doping concentration in the semiconductor substrate. First, we determine the depletion capacitance in the strong inversion regime using (1.27),

$$1/c_{min} = 1/c_{dT} + 1/c_i. \qquad (1.30)$$

From c_{dT} we obtain the thickness of the depletion region at threshold as

$$d_{dT} = S\varepsilon_s/c_{dT}. \qquad (1.31)$$

Then we calculate the doping density N_A using (1.23) with $\phi_s = 2\varphi_b$ and (1.2) for φ_b.

This results in the following transcendental equation for N_A:

$$N_A = \frac{4\varepsilon_s V_{th}}{q d_{dT}^2} \ln\left(\frac{N_A}{n_i}\right). \qquad (1.32)$$

This equation can easily be solved by iterative procedure or any of approximate analytical techniques.

Once d_i and N_A have been obtained, the device capacitance C_{FB} under flat-band conditions can be determined using $C_s = C_{so}$ ((1.21) at flat-band condition) in combination with (1.19):

$$c_{FB} = \frac{C_{so}C_i}{c_{so}+c_i} = \frac{S\varepsilon_s\varepsilon_i}{\varepsilon_i d_i + \varepsilon_i L_{DP}}. \qquad (1.33)$$

The flat-band voltage V_{FB} is simply equal to the applied voltage corresponding to this value of the device capacitance.

We note that the above characterization technique applies to ideal MOS structures.

Different nonideal effects, such as geometrical effects, nonuniform substrate doping, interface states, and mobile charges in the oxide may influence the $C-V$ characteristics of the MOS capacitor.

1.2.4 MOS Charge Control Mod:

Well above threshold, the charge density of the mobile carriers in the inversion layer can be calculated using the parallel plate charge control model of (1.28). This model gives an adequate description for the strong inversion regime of the MOS capacitor, but fails for applied voltages near and below threshold (i.e., in the weak inversion and depletion regimes). Several expressions have been proposed for a unified charge control model (UCCM) that covers all the regimes of operation, including the following [17]:

$$V - V_T = \frac{q(n_s - n_0)}{c_a} + \eta V_{th} \ln(n_s/n_0). \qquad (1.34)$$

Where: $C_a \approx c_i$ is approximately the insulator capacitance per unit area (with a small correction for the finite vertical extent of the inversion channel, see Lee et al. (1993)),

$n_0 = n_s(V = V_T)$ is the density of minority carriers per unit area at threshold, and η is the so-called sub threshold ideality factor, also known as the sub threshold swing parameter.

The ideality factor accounts for the sub threshold division of the applied voltage between the gate insulator and the depletion layer, and $1/\eta$ represents the fraction of this voltage that contributes to the interface potential. A simplified analysis gives

$$\eta = 1 + {C_D}/{C_I}, \qquad (1.35)$$

$$n_0 = \eta V_{th} c_a / 2q. \qquad (1.36)$$

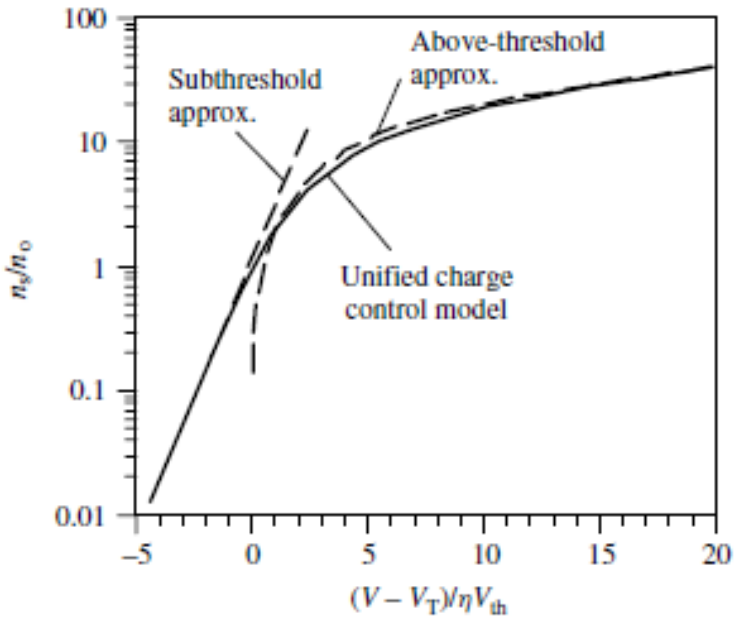


Figure 1.9 Comparison of various charge control expression for the MOS capacitor. New the Equation(1.38) is a close approximation to (1.34), while the above- and below-threshold approximations are given by (1.28) and (1.37), respectively [8].

In the sub threshold regime, (1.34) approaches the limit

$$n_s = n_0 \exp\left(\frac{V - V_T}{\eta V_{th}}\right). \qquad (1.37)$$

We note that (1.34) does not have an exact analytical solution for the inversion charge in terms of the applied voltage. However, for many purposes, the following approximate solution may be suitable:

$$n_s = 2\ln\left[1 + \tfrac{1}{2}\exp\left(\frac{V - V_T}{\eta V_{th}}\right)\right]. \qquad (1.38)$$

This expression reproduces the correct limiting behavior both in strong inversion and

in the sub threshold regime, although it deviates slightly from (1.34) near threshold. The various charge control expressions of the MOS capacitor are compared in Figure 1.9.

1.3 BASIC MOSFET OPERATION:

In the MOSFET, an inversion layer at the semiconductor–oxide interface acts as a conducting Channel . For example, in an n-channel MOSFET, the substrate is p-type silicon and the inversion charge consists of electrons that form a conducting channel between the n+ ohmic source and the drain contacts. At DC conditions, the depletion regions and the neutral substrate provide isolation between devices fabricated on the same substrate.

A schematic view of the n-channel MOSFET is shown in Figure 1.10.

As described above for the MOS capacitor, inversion charge can be induced in the channel by applying a suitable gate voltage relative to other terminals. The onset of strong inversion is defined in terms of a threshold voltage V_T being applied to the gate [15-18], electrode relative to the other terminals. In order to assure that the induced inversion channel extends all the way from source to drain, it is essential that the MOSFET gate structure either overlaps slightly or aligns with the edges of these contacts (the latter is achieved by a self-aligned process). Self-alignment is preferable since it minimizes the parasitic gate-source and gate drain, capacitances.

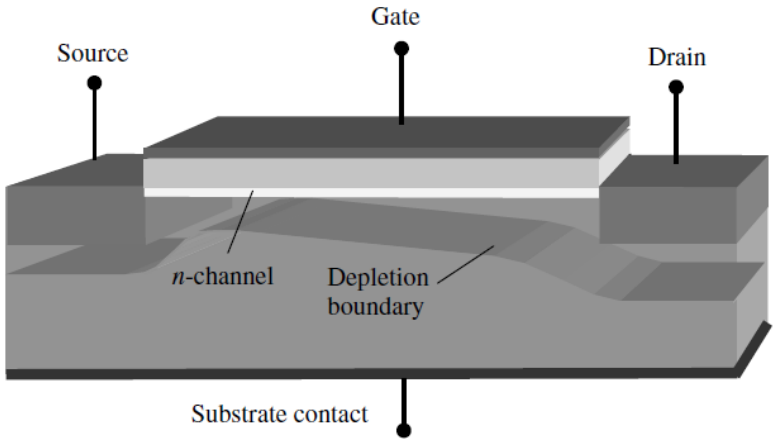


Figure 1.10 Schematic view of an n-channel MOSFET with conducting channel and depletion region.

When a drain-source bias V_{DS} is applied to an n-channel MOSFET in the above threshold conducting state, electrons move in the channel inversion layer from source to drain. A change in the gate-source voltage V_{GS} alters the electron sheet density in the channel, modulating the channel conductance and the device current. For $V_{GS} > V_T$ in an n-channel device, the application of a positive V_{DS} gives a steady voltage increase from source to drain along the channel that causes a corresponding reduction in the local gate-channel bias V_{GX} (here X signifies a position x within the channel). This reduction is greatest near drain where V_{GX} equals the gate-drain bias V_{GD} [18].

Somewhat simplified, we may say that when $V_{GD} = V_T$, the channel reaches threshold at the drain end and the density of inversion charge vanishes at this point. This is the so-called pinch-off condition, which leads to a saturation of the drain current I_{ds}. The corresponding drain-source voltage, $V_{DS} = V_{SAT}$, is called the saturation voltage. Since $V_{GD} = V_{GS} - V_{DS}$, we find that $V_{SAT} = V_{GS} - V_T$. (This is actually a result of the SCCM, which is discussed in more detail in Section 1.4.1.)

When $V_{DS} > V_{SAT}$, the pinched-off region near drain expands only slightly in the direction of the source, leaving the remaining inversion channel intact. The point of abrupt transition between the two regions, $x = x_P$, is characterized by $V_{XS}(x_P) \approx V_{SAT}$, where $V_{XS}(x_P)$ is the channel voltage relative to source at the transition point. Hence, the drain current in saturation remains approximately constant, given by the voltage drop V_{SAT} across the part of the channel that remain in inversion. The voltage $V_{DS} - V_{SAT}$ across the pinched-off region creates a strong electric field, which efficiently transports the electrons from the strongly inverted region to the drain.

Typical current–voltage characteristics of a long-channel MOSFET, where pinch-off is the predominant saturation mechanism, are shown in Figure 1.11. However, for smaller shorter MOSFET gate lengths, typically in the submicrometer range, velocity saturation will occur in the channel near drain at lower V_{DS} than that causing pinch-off. This leads to more evenly spaced saturation characteristics than those shown in this figure, more in

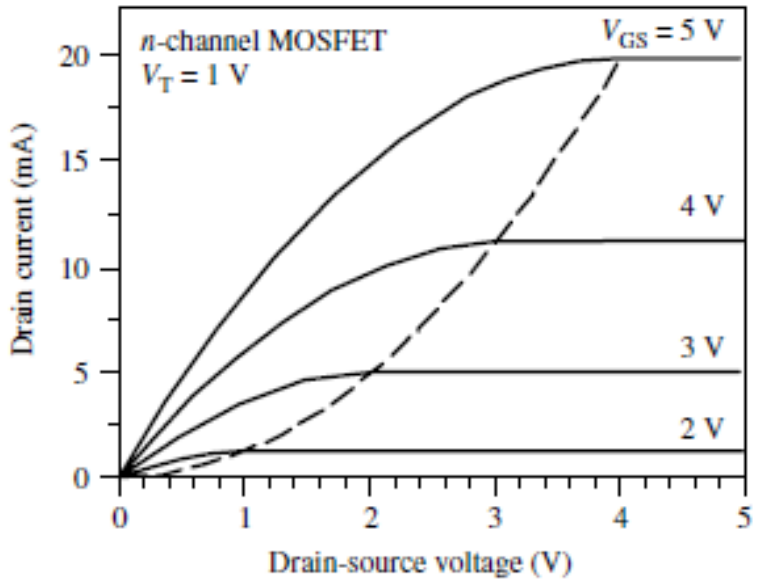


Figure 1.11 Current–voltage characteristics of an n-channel MOSFET with current saturation caused by pinch-off (long-channel case). The intersections with the dotted line indicate the onset of saturation for each characteristic. The threshold voltage is assumed to be V_T= 1V [8].

Agreement with those observed for modern devices. Also, phenomena such as a finite channel conductance in saturation, a drain bias–induced shift in the threshold voltage, and an increased subthreshold current are important consequences of smaller gate lengths .

1.4 BASIC MOSFET MODELING:

Analytical or semianalytical MOSFET models are usually based on the so-called gradual channel approximation (GCA). Contrary to the situation in the ideal two-terminal MOS device, where the charge density profile is determined from one-dimensional Poisson's equation, the MOSFET generally poses a two-dimensional electrostatic problem. The reason is that the geometric effects and the application of a drain-source bias create a lateral electric field component in the channel, perpendicular to the vertical field associated with the ideal gate structure. The GCA states that, under certain conditions, the electrostatic problem of the gate region can be expressed in terms of two coupled one-dimensional equations – a Poisson's equation for determining the vertical charge density profile under the gate and a charge transport equation for the channel. This allows us to determine self-consistently both the channel potential and the charge profile at any position along the gate. A direct inspection

of the two-dimensional Poisson's equation for the channel region shows that the GCA is valid if we can assume that the electric field gradient in the lateral direction of the channel is much less than that in the vertical direction perpendicular to the channel [18].

Typically, we find that the GCA is valid for long-channel MOSFETs, where the ratio between the gate length and the vertical distance of the space charge region from the gate electrode, the so-called aspect ratio, is large. However, if the MOSFET is biased in saturation, the GCA always becomes invalid near drain as a result of the large lateral field gradient that develops in this region. In Figure 1.12, this is schematically illustrated for a MOSFET in saturation.

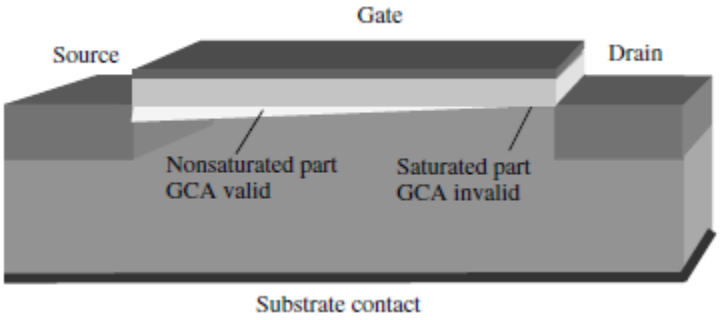


Figure 1.12 Schematic representation of a MOSFET in saturation, where the channel is divided into a nonsaturated region where the GCA is valid and a saturated region where the GCA is invalid.

We should note that the analysis that follows is based on idealized device structures.
Especially in modern MOSFET/CMOS technology, optimized for high-speed and low power applications, the devices are more complex. Additional oxide and doping regions are used for the purpose of controlling the threshold voltage and to avoid deleterious effects of high electric fields and so-called short- and narrow-channel phenomena associated with the steady downscaling device dimensions.

1.4.1 Simple Charge Control Model:

Consider an n-channel MOSFET operating in the above-threshold regime, with a gate voltage that is sufficiently high to cause inversion in the entire length of the channel at zero drain-source bias. We assume a long-channel device, implying that GCA is applicable and that the carrier mobility can be taken to be constant (no velocity saturation). As a first approximation,

we can describe the mobile inversion charge by a simple extension of the parallel plate expression (1.28), taking into account the potential variation $V(x)$ along the channel, that is,

$$qs_n(x) \approx c_i[V_{GT} - V(x)] \ , \qquad (1.39)$$

Where $V_{GT} \equiv V_{GS} - V_T$. This simple charge control expression implies that the variation of the depletion layer charge along the channel, which depends on $V(x)$, is negligible.

Furthermore, since the expression relies on GCA, it is only applicable for the nonsaturated part of the channel. Saturation sets in when the conducting channel is pinched-off at the drain side, that is, for $n_S(x = L) \geq 0$. Using the pinch-off condition and $V(x = L) = V_{DS}$ in (1.39), we obtain the following expression for the saturation drain voltage in the SCCM:

$$V_{SAT} = V_{GT}. \qquad (1.40)$$

The threshold voltage in this model is given by (1.18), where we have accounted for the substrate bias V_{BS} relative to the source. We note that this expression is only valid for negative or slightly positive values of V_{BS}, when the junction between the source contact and the p-substrate is either reverse-biased or slightly forward-biased. For high V_{BS}, a significant leakage current will take place.

Figure 1.13 shows an example of calculated dependences of the threshold voltage on substrate bias for different values of gate insulator thickness. As can be seen from this figure and from (1.18), the threshold voltage decreases with decreasing insulator thickness and is quite sensitive to the substrate bias voltages. This so-called body effect is essential for device characterization and in threshold voltage engineering. For real devices, it is important to be able to carefully adjust the threshold voltage to match specific application requirements. Equation (1.18) also shows that V_T can be adjusted by changing the doping or by using different gate metals (including heavily doped polysilicon) [19]. As discussed in Section 1.2, the gate metal affects the flat-band voltage through the work-function difference between the metal and the semiconductor. Threshold voltage adjustment by means of doping is often performed with an additional ion implantation through the gate oxide.

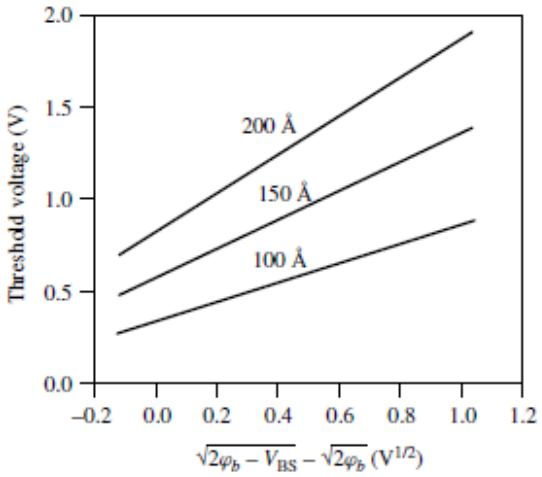


Figure 1.13 Body plot, the dependence of the threshold voltage on substrate bias in MOSFETs with different insulator thicknesses. Parameters used in the calculation: flat-band voltage −1V, substrate doping density $10^{22}/m^3$, temperature 300 K. The slope of the plots are given in terms of the body-effect parameter $\gamma = (2\varepsilon \mathrm{sqN_A})1/2$ [8].

Assuming a constant electron mobility μ_n, the electron velocity can be written as $v_n = -\mu_n dV/dx$. Neglecting the diffusion current, which is important only near threshold and in the subthreshold regime, the absolute value of the drain current can be written as

$$I_{ds} = w.\mu_n.q.n_s.F, \qquad (1.41)$$

Where $F = |dV/dx|$ is the magnitude of the electric field in the channel and W is the channel width. Integrating this expression over the gate length and using the fact that I_{ds} is independent of position x, we obtain the following expression for the current–voltage characteristics:

$$I_{ds} = \frac{w\mu_n c_i}{L} \times \begin{cases} V_{GT} - V_{DS}/2, & \text{for } V_{DS} \le V_{SAT} = V_{GT} \\ V_{GT}^2 & \text{for } V_{DS} > V_{SAT} \end{cases}. \qquad (1.42)$$

As implied above, the pinch-off condition implies a vanishing carrier concentration at the drain side of the channel. Hence, at a first glance, one might think that the drain current should also vanish. However, instead the saturation drain current $I_{d_{sat}}$ is determined by the resistance of nonsaturated part of the channel and the current across it. In fact, this channel resistance changes very little when V_{DS} increases beyond V_{SAT}, since the pinch-off point x_p moves only slightly away from the drain, leaving the nonsaturated part of the channel almost unaffected. Moreover, the voltage at the pinch-off point will always be approximately V_{SAT}

Since the threshold condition at x_p is determined by $V_G - V(x_p) = V_T$, or $V(x_p) = V_{GT} = V_{SAT}$. Hence, since the resistance of the nonsaturated part is constant and the Voltage across it is invariant, $I_{d_{sat}}$ will also remain constant. Therefore, the saturation Current I_{SAT} is determined by substituting $V_{DS} = V_{SAT}$ from (1.40)

Expression in (1.42). In reality, of course, the electron concentration never vanishes, nor does the electric field become infinite. This is simply a consequence of the breakdown of GCA near drain in saturation, pointing to the need for a more accurate and detailed analysis of the saturation regime.

The MOSFET current–voltage characteristics shown in Figure 1.11 were calculated using this simple charge control model.

Important device parameters are the channel conductance,

$$g_d = \frac{\partial I_d}{\partial V_{DS}}\Big|_{V_{GS}} = \begin{cases} \beta(V_{GT} - V_{DS}), & \text{for } V_{DS} \le V_{SAT} \\ 0, & \text{for } V_{DS} \ge V_{SAT}, \end{cases} \quad (1.43)$$

and the transconductance,

$$g_m = \frac{\partial I_d}{\partial V_{DS}}\Big|_{V_{DS}} = \begin{cases} \beta V_{DS} & \text{for } V_{DS} \le V_{SAT} \\ \beta V_{GT} & \text{for } V_{DS} \ge V_{SAT}, \end{cases} \quad (1.44)$$

Where $\beta = W \mu_n C_i / L$ is called the transconductance parameter. As can be seen from these expressions, high values of channel conductance and transconductance are obtained for large electron mobilities, large gate insulator capacitances (i.e., thin gate insulator layers), and large gate width to length ratios.

The SCCM was developed at a time when the MOSFET gate lengths were typically tens of micrometers long, justifying some of the above approximations. With today's deep submicron technology, however, the SCCM is clearly not applicable. We therefore introduce two additional models that include significant improvements. In the first of these, the Meyer model, the lateral variation of the depletion charge in the channel is taken into account. In the second, the velocity saturation model (VSM), we introduce the effects of saturation in the carrier velocity. The former is important at realistic levels of substrate doping, and the latter is important because of the high electric fields generated in short channel devices. Additional effects of small dimensions and high electric fields.

1.4.2 The Meyer Model:

The total induced charge q_s per unit area in the semiconductor of an n-channel MOSFET,

including both inversion and depletion charges, can be expressed in terms of Gauss's law as follows, assuming that the source and the semiconductor substrate are both connected to ground (see Section 1.2),

$$q_s = c_i[V_{GS} - V_{FB} - V(x)]. \quad (1.45)$$

Here, the content of the bracket expresses the voltage drop across the insulator layer. The induced sheet charge density includes both the inversion charge density $q_i = -qn_s$ and the depletion charge density q_d, that is, $q_s = q_i + q_d$. Using (1.15) and including the added channel-substrate bias caused by the channel voltage, the depletion charge per unit area can be expressed as

$$q_d = -qN_A d_d = -\sqrt{2\varepsilon_s qN_A[2\varphi_b + V(x)]}, \quad (1.46)$$

Where d_d is the local depletion layer width at position x. Hence, the inversion sheet charge density becomes

$$q_i = -qn_s = c_i[V_{GS} - V_{FB} - 2\varphi_b - V(x)] + \sqrt{2\varepsilon_s qN_A[2\varphi_b + V(x)]}, \quad (1.47)$$

A constant electron mobility is also assumed in the Meyer model. Hence, the nonsaturated drain current can again be obtained by substituting the expression for n_s in

$$I_{ds} = W\mu_n c_i qn_s(x)F(x) \quad (1.48)$$

to give (Meyer 1971) [20].

$$I_{ds} = \frac{W\mu_n c_i}{L}\left\{\left(V_{GS} - V_{FB} - 2\varphi_b - \frac{V_{DS}}{2}\right)V_{DS} - \frac{2\sqrt{2\varepsilon_s qN_a}}{3c_i}\left[(V_{DS} + 2\varphi_b)^{3/2} - (2\varphi_b)^{3/2}\right]\right\}. \quad (1.49)$$

The saturation voltage is obtained using the pinch-off condition $n_s = 0$,

$$V_{SAT} = V_{GS} - 2\varphi_b - V_{FB} + \frac{\varepsilon_s qN_a}{c_i^2}\left[1 - \sqrt{1 + \frac{2c_i^2(V_{GS} - V_{FB})}{\varepsilon_s qN_a}}\right]. \quad (1.50)$$

At low doping levels, we see that V_{SAT} approaches V_{GT}, which is the result found for the simple charge control model.

1.4.3 Velocity Saturation Model:

The linear velocity-field relationship (constant mobility) used in the above MOSFET models works reasonably well for long-channel devices. However, the implicit notion of a diverging carrier velocity as we approach pinch-off is, of course, unphysical. Instead, current saturation is better described in terms of a saturation of the carrier drift velocity when the electric field near drain becomes sufficiently high. The following two-piece model is a simple, first approximation to a realistic velocity-field relationship:

$$v(F) = \begin{cases} \mu_n F & \text{for } F < F_s \\ v_s & \text{for } F > F_s, \end{cases} \qquad (1.51)$$

Where $F = |dV(x)/dx|$ is the magnitude of lateral electric field in the channel, v_s is the saturation velocity, and $F_s = v_s/\mu_n$ is the saturation field. In this description, current saturation in FETs occurs when the field at the drain side of the gate reaches the saturation field. A somewhat more precise expression, which is particularly useful for n-channel MOSFETs, is the so-called Sodini model [22],

$$v(F) = \begin{cases} \dfrac{\mu_n F}{1+F/2F_s} & \text{for } f < 2F_s \\ v_s & \text{for } f \geq 2F_s \end{cases}. \qquad (1.52)$$

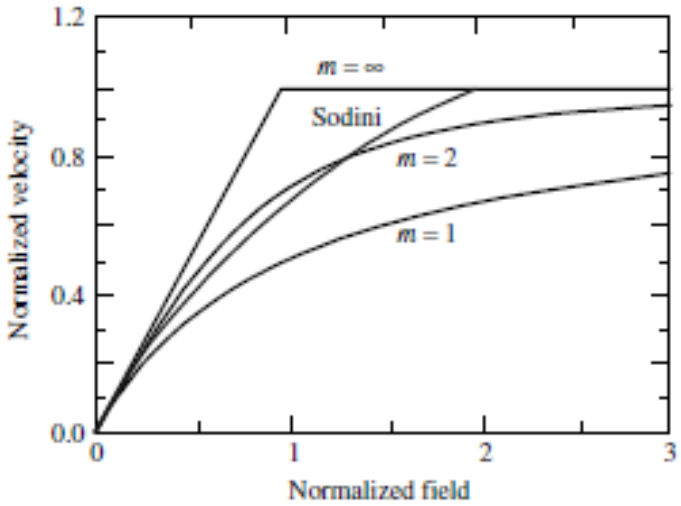


Figure 1.14 Velocity-field relationships for charge carriers in silicon MOSFETs. The electric field and the velocity are normalized to F_s and v_s, respectively. Two of the curves are calculated from (1.53) using $m = 1$ for holes and $m = 2$ for electrons. The curve marked $m = \infty$ corresponds to the linear two-piece model in (1.51). The Sodini model (1.52) is also shown.

Even more realistic velocity-field relationships for MOSFETs are obtained from:

$$v(F) = \frac{\mu F}{\left[1+\left(F/F_s\right)^m\right]^{1/m}}, \qquad (1.53)$$

where $m = 2$ and $m = 1$ are reasonable choices for n-channel and p-channel MOSFETs, respectively. The two-piece model in (1.51) corresponds to $m \to \infty$ in (1.53). Figure 1.14 shows different velocity-field models for electrons and holes in silicon MOSFETs.

Using the simple velocity-field relationship of (1.51), current–voltage characteristics can easily be derived from either the SCCM or the Meyer model, since the form of the non saturated parts of the characteristics will be the same as before (see (1.42) and (1.49)). However, the saturation voltage will now be identical to the drain-source voltage that initiates velocity saturation at the drain side of the channel. In terms of (1.51), this occurs when $F(L) = F_s$. Hence, using this condition in combination with the SCCM, we obtain the following expressions for the drain current and the saturation voltage:

$$I_{ds} = \frac{W \mu_n C_i}{L} \times \begin{cases} V_{GT}V_{DS} - V_{DS}^2, & \text{for } V_{DS} \le V_{SAT} \\ (V_{GT} - V_{SAT})V_L, & \text{for } V_{DS} > V_{SAT} \end{cases}, \qquad (1.54)$$

$$V_{SAT} = V_{GT} - V_L\left[\sqrt{1 + \left(V_{GT}/V_L\right)^2} - 1\right], \qquad (1.55)$$

Where $V_L = F_s L = L v_s/\mu_n$. The Meyer VSM leads to a much more complicated relationship for V_{SAT}.

For large values of V_L such that $V_L \gg V_{GT}$, the square root terms in (1.55) may be expanded into a Taylor series, yielding the previous long-channel result for the SCCM without velocity saturation. Assuming, as an example, that $V_{GT} = 3V$, $\mu_n = 0.08\ m^2/Vs$, and $v_s = 1 \times 10^5$ m/s, we find that velocity saturation effects may be neglected for $L \ge 2.4\mu m$. Hence, velocity saturation is certainly important in modern MOSFETs with gate lengths typically in the deep submicrometer range.

In the opposite limiting case, when $V_L \ll V_{GT}$, we obtain $V_{SAT} \approx V_L$ and $I_{d_{sat}} \approx \beta V_L V_{GT}$

. Since $I_{d_{sat}}$ is proportional to V_{GT}^2 in long-channel devices and proportional toV_{GT} in short-channel devices, we can use this difference to identify the presence of short-channel effects on the basis of measured device characteristics [22].

1.4.4 Capacitance Models:

For the simulation of dynamical events in MOSFET circuits, we also have to account for variations in the stored charges of the devices. In a MOSFET, we have stored charges in the gate electrode, in the conducting channel, and in the depletion layers. Somewhat simplified, the variation in the stored charges can be expressed through different capacitance elements, as indicated in Figure 1.15.

We distinguish between the so-called parasitic capacitive elements and the capacitive elements of the intrinsic transistor. The parasitics include the overlap capacitances between the gate electrode and the highly doped source and drain regions (C_{os} and C_{od}), the junction capacitances between the substrate and the source and drain regions (C_{js} and C_{jd}), andthe capacitances between the metal electrodes of the source, the drain, and the gate [13-16].

The semiconductor charges of the intrinsic gate region of the MOSFET are divided between the mobile inversion charge and the depletion charge, as indicated in Figure 1.15.

In addition, these charges are no uniformly distributed along the channel when drain source bias is applied. Hence, the capacitive coupling between the gate electrode and the semiconductor is also distributed, making the channel act as an RC transmission line. In practice, however, because of the short gate lengths and limited bandwidths of FETs, the distributed capacitance of the intrinsic device is usually very well represented in terms of a lumped capacitance model, with capacitive elements between the various intrinsic device terminals.

An accurate modeling of the intrinsic device capacitances still requires an analysis of how the inversion charge and the depletion charge are distributed between source, drain, and substrate for different terminal bias voltages [23]. As discussed by Ward and Dutton(1978), such an analysis leads to a set of charge-conserving and nonreciprocal capacitances between the different intrinsic terminals (nonreciprocity means $C_{ij} \neq C_{JI}$, where i and j denote source, drain, gate, or substrate).

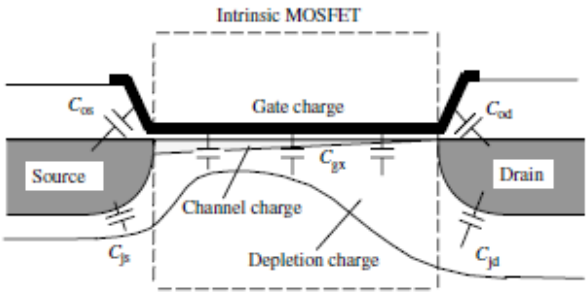


Figure 1.15 Intrinsic and parasitic capacitive elements of the MOSFET. Reproduced from Fjeldly T. A., Ytterdal T., and Shur M [8].

In a simplified and straightforward analysis by Meyer (1971) [20] based on the SCCM, a set of reciprocal capacitances ($C_{ij} = C_{ji}$) were obtained as derivatives of the total gatecharge with respect to the various terminal voltages. Although charge conservation is not strictly enforced in this case, since the Meyer capacitances represent only a subset of the Ward–Dutton capacitances, the resulting errors in circuit simulations are usually small, except in some cases of transient check of certain demanding circuits. Here, we first consider Meyer's capacitance model for the long-channel case.

In Meyer's capacitance model, the distributed intrinsic MOSFET capacitance can be split into the following three lumped capacitances between the intrinsic terminals:

$$C_{GS} = \frac{\partial Q_G}{\partial V_{GS}}\Big|_{V_{GS},V_{GB}}, \quad C_{GD} = \frac{\partial Q_G}{\partial V_{GD}}\Big|_{V_{GS}V_{GB}}, \quad C_{GB} = \frac{\partial Q_G}{\partial V_{GB}}\Big|_{V_{GS},V_{GD}}, \tag{1.56}$$

Where Q_G is the total intrinsic gate charge. The intrinsic MOSFET equivalent circuit corresponding to this model is shown in Figure 1.16.

In general, the gate charge reflects both the inversion charge and the depletion charge and can therefore be written as $Q_G = Q_{Gi} + Q_{Gd}$. However, in the SCCM for the drain current, the depletion charge is ignored in strong inversion, except for its influence on the threshold voltage (see (1.18)). Likewise, in the Meyer capacitance model, the gate-source capacitance C_{GS} and the gate-drain capacitance C_{GD} can be assumed to be dominated by the inversion charge. Here, we include gate-substrate capacitance C_{GB} in the subthreshold regime, where the depletion charge is dominant.

The contribution of the inversion charge to the gate charge is determined by integrating the sheet charge density given by (1.39), over the gate area, that is,

$$Q_{Gi} = W_{C_i} \int_0^L [V_{GT} - V(x)]\, dx\,. \qquad (1.57)$$

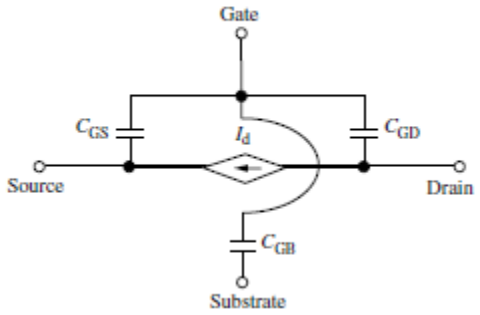


Figure 1.16 Large-signal equivalent circuit of intrinsic MOSFET based on Meyer's capacitance model [8].

From (1.41), we notice that $dx = W_{\mu_n c_i}(V_{GT} - V)\, dV/I_{ds}$, which allows us to make a change of integration variable from x to V in (1.57). Hence, we obtain for the non saturated regime

$$Q_{Gi} = \frac{W_{\mu_n c_i} C_I^2}{L I_{ds}} \int_0^{V_{DS}} (V_{DS} - V)^2 dV = \frac{2}{3} C_i \frac{(V_{GT}-V_T)^3 - (V_{GD}-V_T)^3}{(V_{GS}-V_T)^2 - (V_{GD}-V_T)^2}\,, \qquad (1.58)$$

Where C_i is the total gate oxide capacitance and where we express I_{ds} using (1.42) and replace V_{DS} by $V_{GS}-V_{GD}$ everywhere.

Using the above relationships, the following strong inversion, long-channel Meyer capacitances are obtained:

$$C_{GS} = \frac{2}{3} C_i \left[1 - \left(\frac{V_{GT}-V_{DS}}{2V_{GS}-V_{DS}}\right)^2\right], \qquad (1.59)$$

$$C_{GD} = \frac{2}{3} C_i \left[1 - \left(\frac{V_{GT}}{2V_{GS}-V_{DS}}\right)^2\right], \qquad (1.60)$$

$$C_{GB} = 0\,, \qquad (1.61)$$

We recall that $V_{SAT} = V_{GT}$ is the saturation voltage in the SCCM. The capacitances at saturation are found by replacing $V_{DS} = V_{SAT}$ in the above expressions, that is,

$$C_{GS_S} = \frac{2}{3} C_i \ , \qquad C_{GD_S} = C_{GB_S} = 0. \tag{1.62}$$

This result indicates that in saturation, a small varietal of the applied drain-source voltage does not contribute either to the gate or the channel charge, since the channel is pinched off. Instead, the entire channel charge is assigned to the source terminal, giving a maximum value of the capacitance C_{GS}. Normalized dependencies of the Meyer capacitances $C_{GS}$and C_{GD} on bias conditions are shown in Figure 1.17.

In the subthreshold regime, the inversion charge becomes negligible compared to the depletion charge, and the MOSFET gate-substrate capacitance will be the same as that of a MOS capacitor in depletion, with a series connection of the gate oxide capacitance C_i and the depletion capacitance C_d (see (1.19) to (1.23)). The applied gate-substrate voltage V_{GB} can be subdivided as follows:

$$V_{GB} = V_{FB} + \phi_s - q_{dcp}/C_i \ , \tag{1.63}$$

Where V_{FB} is the flat-band voltage, ϕ_S is the potential across the semiconductor depletion layer (i.e., the surface potential relative to the substrate interior), and $-q_{dcp}/C_i$ is the voltage drop across the oxide. In the depletion approximation, the depletion charge per unit area q_{dcp} is related to ϕ_S by

$$q_{dcp} = -\gamma C_i \phi_S^{1/2}$$

Where $\gamma = (2\varepsilon_s q N_A)^{1/2}$ is the body effect parameter. Using this relationship to substitute for ϕ_s in (1.63), we find

$$Q_{GD} = -WLq_{dcp} = \gamma C_i \left(\sqrt{\gamma^2/4 + V_{GB} - V_{FB}} - \gamma/2 \right), \tag{1.64}$$

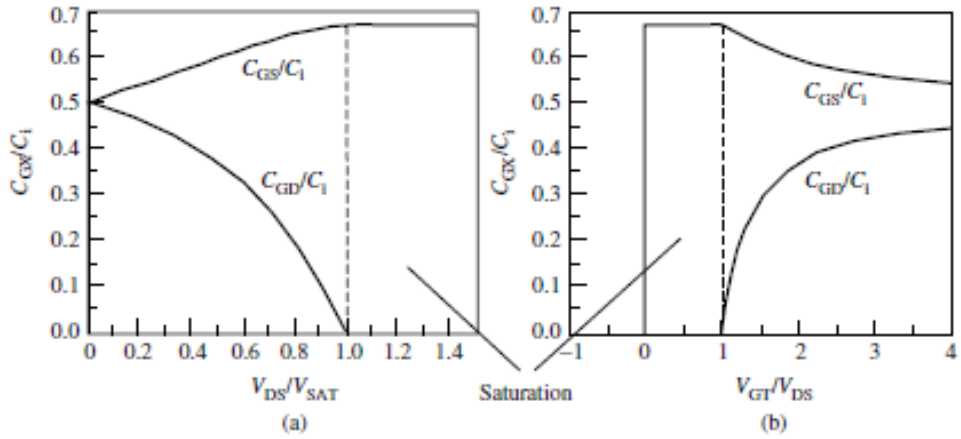


Figure 1.17 Normalized strong inversion Meyer capacitances according to (1.59) to (1.62) versus (a) drain-source bias and (b) gate-source bias. Note that $V_{SAT} = V_{GT}$ in this model [8].

From which we obtain the following subthreshold capacitances:

$$C_{GB} = \frac{C_i}{\sqrt{1+4(V_{GB}-V_{FB})/\gamma^2}}\ , \qquad C_{GS} = C_{GD} = 0\,. \tag{1.65}$$

We note that (1.65) gives $C_{GB} = C_i$ at the flat-band condition, which is different from the flat-band capacitance of (1.33). This discrepancy arises from neglecting the effects of the free carriers in the subthreshold regime in the present simplified treatment. For the same reason, we observe the presence of discontinuities in the Meyer capacitances at threshold. Discontinuities in the derivatives of the Meyer capacitances occur at the onset of saturation as a result of additional approximations. Such discontinuities should be avoided in the device models since they give rise to increased simulation time and conversion problems in circuit simulators.

In the MOSFET VSM, the above-threshold capacitance expressions derived on the basis of the SCCM are still valid in the nonsaturated regime $V_{DS} \leq V_{SAT}$. The capacitance values at the saturation point are found by replacing V_{DS} in (1.59) and (1.60) by V_{SAT} from (1.55), yielding

$$C_{GS_S} = \frac{2}{3} C_i \left[1 - \left(\frac{V_{SAT}}{2V_L}\right)^2\right], \tag{1.66}$$

$$C_{GD_S} = \frac{2}{3} C_i \left[1 - \left(1 - \frac{V_{SAT}}{2V_L}\right)^2\right]. \quad (1.67)$$

However, well into saturation, the intrinsic gate charge will change very little with increasing V_{DS}, similar to what takes place in the case of saturation by pinch-off (see preceding text). Hence, the real capacitances have to approach the same limiting values in saturation as the Meyer capacitances, that is,$C_{GS}/c_i \rightarrow 2/3$ and $C_{GD}/c_i \rightarrow 0$. In fact, since the behavior of C_{GS} and C_{GD} in the VSM and in the SCCM coincide for $V_{DS} < V_{SAT}$ and have the same asymptotic values in saturation, the Meyer capacitance model offers a reasonable approximation for the MOSFET capacitances also in short channel devices. This suggests a separate "saturation" voltage for the capacitances close to the long-channel pinch-off voltage ($\approx V_{GT}$), which is larger than V_{SAT} associated with the onset of velocity saturation.

1.4.5 Comparison of Basic MOSFET Models:

The I–V characteristics shown in Figure 1.18 were calculated using the three basic MOSFET models discussed above – the simple charge control model (SCCM), the Meyer I–V model (MM), and the velocity saturation model (VSM). The same set of MOSFET parameters were used in all cases. We note that all models coincide at small drain-source voltages. However, in saturation, SCCM always gives the highest current. This is a direct consequence of omitting velocity saturation and spatial variation in the depletion charge in SCCM, resulting in an overestimation of both carrier velocity and inversion charge. The characteristics for VSM and MM clearly demonstrate how inclusion of velocity saturation and distribution of depletion charge, respectively, affect the saturation current.

The intrinsic capacitances according to Section 1.4.4 are shown in Figure 1.19. Meyer's capacitance model can be used in conjunction with all the MOSFET models illustrated in Figure 1.18 (SCCM, MM and VSM). In the present device example, we note that velocity saturation and depletion charge may be quite important. Therefore, we emphasize that SCCM is usually applicable only for long-channel, low-doped devices, while MM applies to long-channel devices with an arbitrary doping level. VSM gives a reasonable description of short-channel devices, although important short-channel effects such as channel-length modulation and drain-induced barrier lowering (DIBL) are still unaccounted for in these

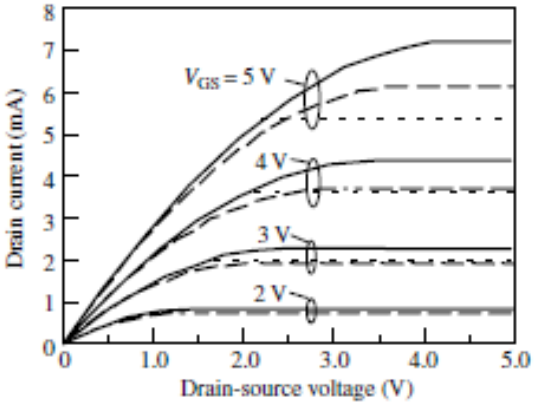


Figure 1.18 Comparison of I–V characteristics obtained for a given set of MOSFET parameters using the three basic MOSFET models: simple charge control model (solid curves), Meyer's I–V model (dashed curves), and velocity saturation model (dotted curves). The MOSFET device parameters are L = 2μm, $w = 20\mu m$, d_i= 300A° ; μ_n= 0. 06m^2/Vs, v_s= 10^5 m/s; N_A= $10^{22}/m^3$, V_T= 0. 43V; V_{FB}= −0. 75 V; ε_i= 3. 45 ×10^{-11} F/m; ε_s= 1. 05 ×10^{-10}F/m; n_i= 1. 05 ×$10^{16}/m^3$. [8]

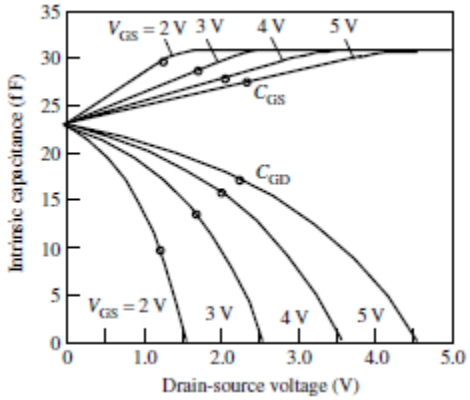


Figure 1.19 Intrinsic MOSFET C–V characteristics for the same devices as in Figure 1.18, obtained from the Meyer capacitance model. The circles indicate the onset of saturation according to (1.66) and (1.67). [8]

1.4.6 Basic Small-signal Model:

So far, we have considered large-signal MOSFET models, which are suitable for digital electronics and determining the operating point in small-signal applications. The small signal regime is, of course, a very important mode of operation of MOSFETs as well as for other

active devices. Typically, the AC signal amplitudes are so small relative to the DC values of the operating point that a linear relationship can be assumed between an incoming signal and its response. Normally, if sufficiently accurate large-signal models are available, the AC designers will use such large-signal models also for small-signal applications, since this mode is readily available in circuit simulators such as SPICE.

However, in cases when suitable large-signal models are unavailable or when simple hand calculations are needed, it is convenient to use a dedicated small-signal MOSFET model based on a linearized network.

Figure 1.20 shows an intrinsic, common-source, small-signal model for MOSFETs.

The model is generalized to include inputs at both the gate and the substrate terminal, and the response is observed at the drain [24].

. The network elements are obtained as first derivatives of current–voltage and charge–voltage characteristics, resulting in fixed small-signal conductance's, transconductance, and capacitances for a given operating point.

To build a more complete model, some of the extrinsic parasitics may be added, including the gate overlap capacitances and the source and drain junction capacitances, shown in Figure 1.15, and the source and drain series resistances. At very high frequencies, in the radio frequency (RF) range, the junction capacitances become very important since

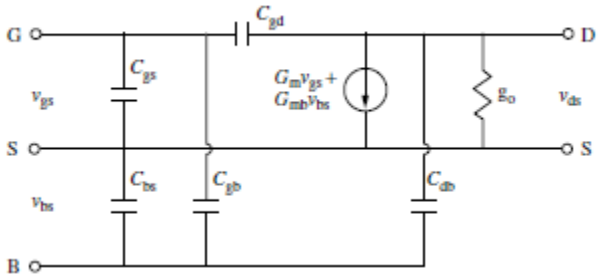


Figure 1.20 Basic small-signal equivalent circuit of an intrinsic, common-source MOSFET [24].

They couple efficiently to the MOSFET substrate. Other important parasitics in this range are the gate resistance and the series inductances associated with the conducting paths[1-3].

2.1 MOSFET Fabrication:

Semiconductor devices have long been used in electronics since the late nineteenth century.

The galena crystal detector, invented in 1907, was widely used to build crystal radio sets. However, the idea of placing multiple electronic devices on the same substrate material came only after the late 1950s. In 1959, the first integrated circuit (IC) was constructed, which started a new era of modern semiconductor manufacturing. In less than 50 years, the IC technology, represented primarily by the complementary-metal-oxide-semiconductor (CMOS) process, has gone through the periods from producing very simple chips containing a few bipolar or MOS components to fabricating ultra-large-scale-integrated (ULSI) CMOS circuits with very high device densities from millions of transistors a chip for some circuits such as microprocessors to more than several billions of transistors a chip for some circuits such as memories. As predicted by Moore's law created in the early 1970s, the number of transistors per chip for a microprocessor has continued to double approximately every 18 to 24months. Taking Intel's processors as an example, the number of transistors on a chip has increased more than 3200 times, from 2300 on the 4004 microprocessor in 1971 to 7.5 million on the Pentium II processor in 1996, and to 55 million on the Pentium 4 processor in 2001. At the same time, the minimal dimension of the transistors has reduced from about 20μm in 1960 to 0.35μm in 1996, and more rapidly recently, to 0.13μm in 2001, resulting in an amazing improvement in both speed and cost of the circuits [25].

The development of IC technology was driven mainly by the digital circuit (microprocessor and memory) market. Recently, however, CMOS technology has been extensively used in the analog circuit design because of the low cost of fabrication and compatibility of integrating both analog and digital circuits on the same chip, which improves the overall performance and reliability and may also reduce the cost of packaging. It has been the dominant technology to fabricate digital ICs and will be the mainstream technology for analog and mixed-signal applications. Currently, circuit designers are even exploring emerging pure CMOS approaches – integrating digital blocks, analog and radio-frequency (RF) circuits on a single chip to implement the so-called mixed-signal (MS) or system on- chip (SOC) solutions.

In today's IC industry, much of the design efforts, including layout generators, device models, and technology files, have been automated in the design tools provided by either foundries or design automation vendors. However, a basic understanding of semiconductor devices and fabrication processes is essential to optimize the circuits, especially analog/RF circuits. We first discuss the major process steps in CMOS fabrication. Then we will go

through a typical digital process flow to understand the MOSFET structures and the concepts of MOSFET fabrication. Finally, additional fabrication steps for other components, mainly passive devices, in an analog/RF process .

2.2 TYPICAL PLANAR DIGITAL CMOS PROCESS FLOW:

The polysilicon gate CMOS process has been widely used for IC fabrication. A MOSFET process flow in a baseline polysilicon gate CMOS fabrication is described in the flowchart in Figure 2.1. The mask operations are illustrated in the figure.

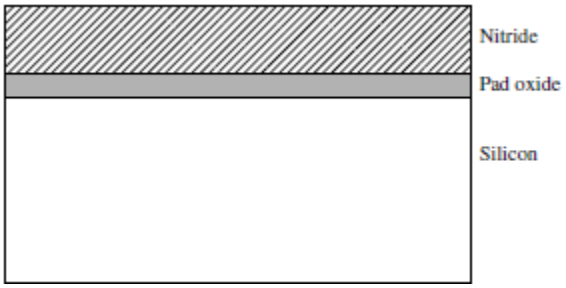
2.2.1 Starting material:

We discuss CMOS technology that is fabricated from silicon, a very common and widely distributed element on earth. The mineral quartz consists entirely of silicon dioxide, also called silica. Ordinary sand is composed mainly of tiny grains of quartz and is therefore also mostly silica. Despite the abundance of its compounds, elemental silicon does not exist naturally. The element can be artificially produced by heating silica and carbon in an electric furnace. The carbon unites with the oxygen contained in the silica, leaving molten silicon. As it is solidified, it will be in a polycrystalline structure, that is, there is no regular crystal structure throughout the block of the material but simply small areas of crystals at different orientations to neighboring crystal areas. Impurities and disordering of the metallurgical-grade polysilicon make it unsuitable for semiconductor manufacture as a substrate material. The polysilicon can be refined in a purification process to produce an extremely pure semiconductor grade material. Once the material has been purified, it can be further processed into single crystal bars by using the so-called Czochralski method, in which the purified material is completely molten and the seed crystal is dipped into the surface of the melt and slowly withdrawn and rotated. The speed of pull and the rate of cooling will determine the diameter of the final rod of the material. Dopant material can be introduced into the melt in the required ratio. Since ICs are formed upon the surface of a silicon crystal within a limited depth ($<10\mu m$), the crystal bar is customarily sliced into numerous thin circular pieces called wafers. The larger the wafer, the more ICs it can have, and so the lower the fabrication cost. Most modern processes currently employ 200-mm (8) wafers. However, process lines for 300-mm (12) wafers have been announced to operate in 2002 by the semiconductor foundry industry [24-26].

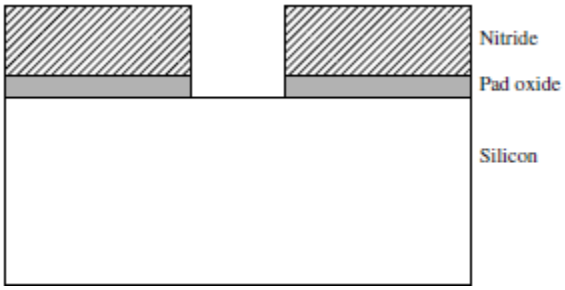
Although a certain amount of dopant material can be introduced into the material during the crystallization process, there is a limit on the doping level that can be introduced if a consistent dopant concentration is to be maintained throughout the material. To obtain the highly doped regions required by some of the active devices, a further crystal growth process called epitaxy is performed to provide a thin epitaxial region on the top of the “native” wafer. A continuous crystal structure has to be maintained, so the resulting wafer is still a single crystal throughout. Epitaxy allows the formation of buried layers.

The formation of an n+ buried layer is one of the key steps in most bipolar and BICMOS processes. CMOS ICs are normally fabricated on a p-type (100) substrate doped with boron. To provide a better immunity against CMOS latch-up, the substrate is usually doped as high as possible, limited by solid solubility, to minimize the substrate resistivity.

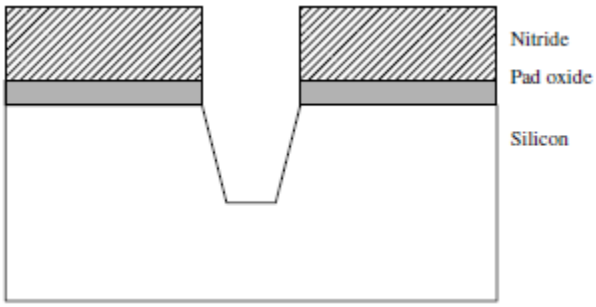
In principle, this kind of p-type wafer can be used directly for fabrication. However, a lightly doped p-type epitaxial layer is usually formed to maintain the latch-up immunity but have more precise control of the electric properties of the substrate material and hence control of the MOSFET electric characteristics.



(1) Substrate wafer after the pad oxide growth and nitride deposition

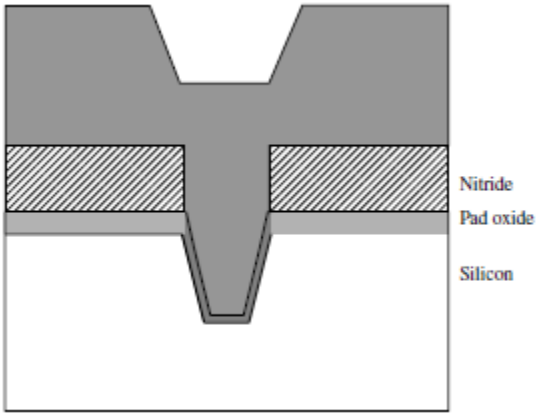


(2) Pad oxide and nitride removing for STI etch

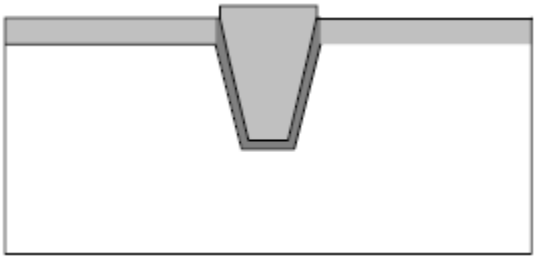


(3) STI etch

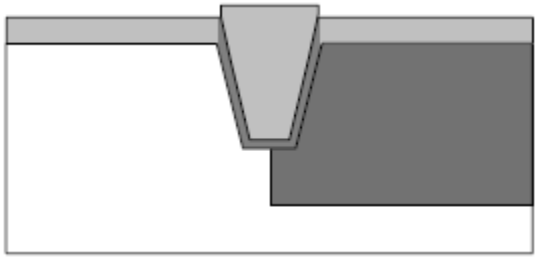
Figure 1.21 Illustration of the process flow for MOSFETs in a baseline CMOS technology



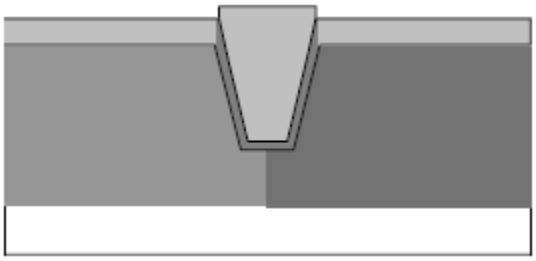
(4) High-density plasma oxide deposition



(5) After CMP and nitride removing



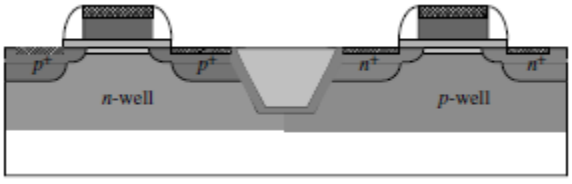
(6) n-well formation



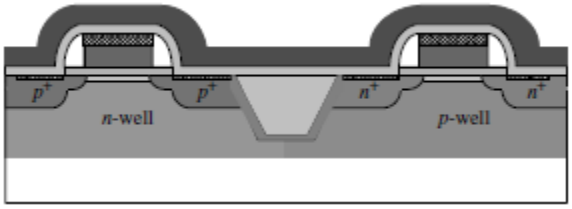
(7) p-well formation

Figure 1.21(continued)

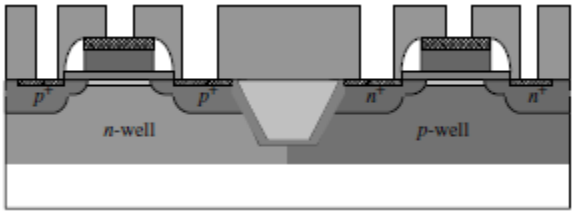
(12) Nitride spacer and source/drain implantation for both nFET and pFET



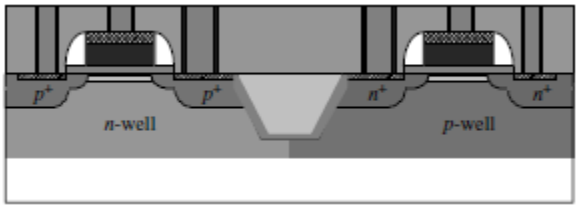
(13) Source/drain salicidation



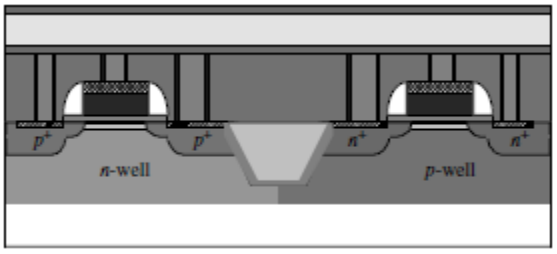
(14) Isolation layer deposition



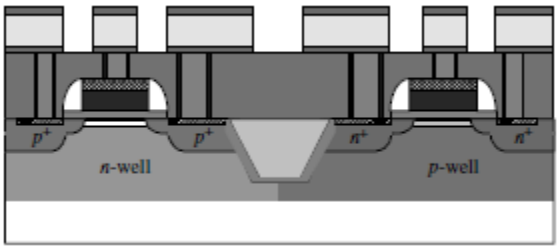
(15) Contact etch



(16) Metallization for source/drain and gates



(17) Metal 1 layer deposition



(18) Metal 1 etch

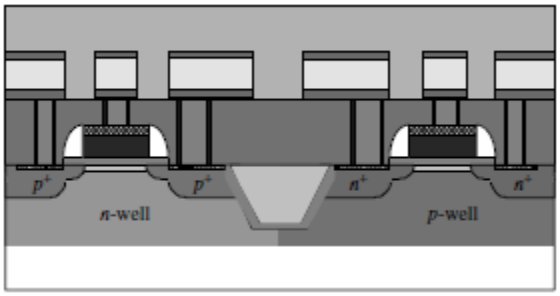
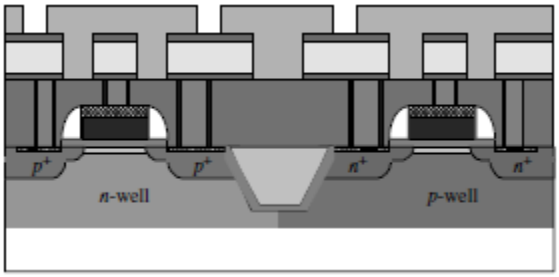
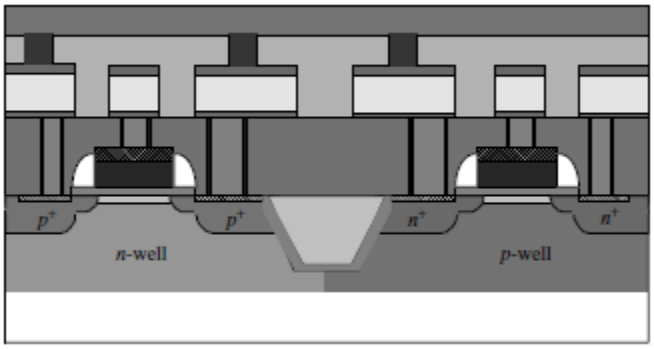


Figure 1.21 (continued)

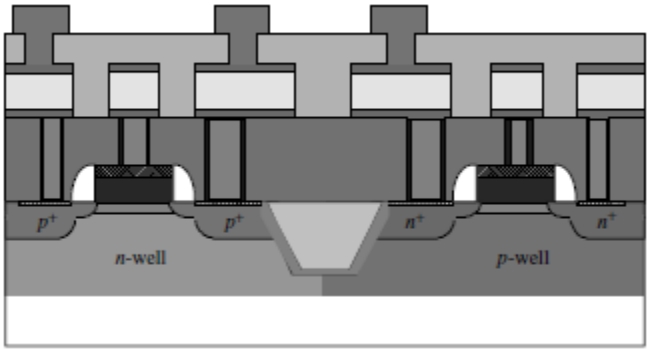
(19) Interlayer isolation dielectric deposition



(20) Via etch

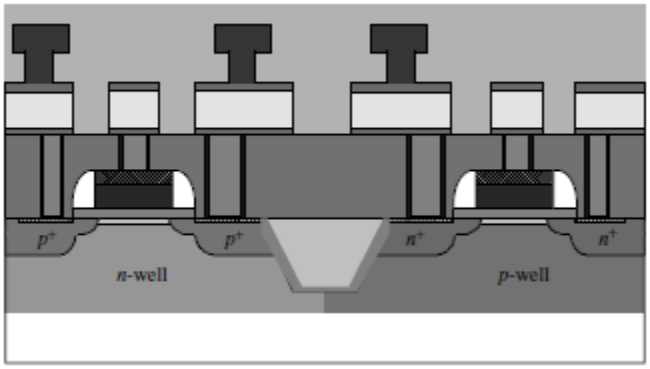


(21) Metal 2 deposition

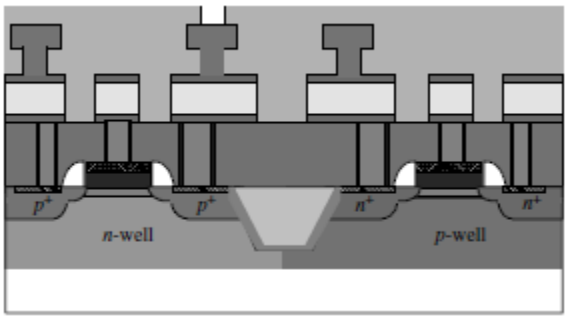


(22) Metal 2 etch

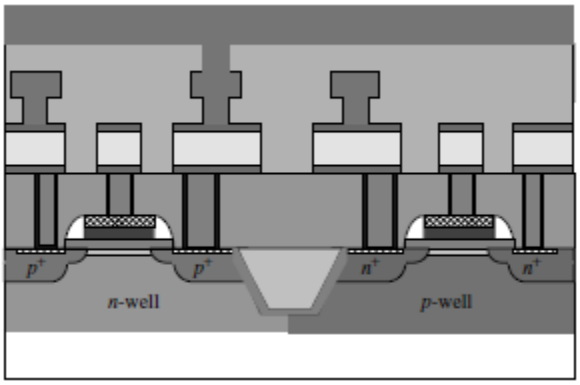
Figure 1.21 (continued)



(23) Higher-level interlayer dielectric deposition

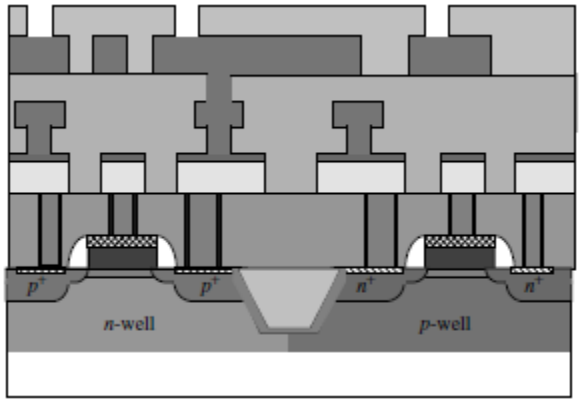


(24) Higher-level via etch



(25) High-level metal deposition

Figure 2.1 (continued)



(26) Passivation layer deposition and pad open

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Part Two:

Specific properties of SiC (with special attention paid to 4H SiC 6H SiC crystal lattice). The comparison of SiC parameters relevant for I-V characteristic modeling with corresponding data for Si.

2.1: INTRODUCTION:

why not Silicon:

All vehicles contain power converters as rectifiers, power supplies, battery chargers, etc. Separating HEVs from conventional vehicles, however, is the electrical traction drive. This drive, as the vital part of a HEV, carries the most power among all the HEV power converters.

All of the electronics in a vehicle must continue to operate under harsh conditions with the most detrimental condition such as high temperature. Since heat is generated by the engine, the motor, the semiconductor device losses, and the environment, all of the electronics have to be cooled so that they will continue to perform. Note that the maximum junction temperature limit for most Si electronics is 150°C; therefore, the temperature of the Si chips and power

devices should remain belew this value. Even then, the variation in the electrical characteristics of Si devices with temperature and time is still a big reliability.

Three standard options for device cooling are natural air, forced air, or water-cooled heatsinks. However, as the temperature of the environment increases, the cooling capacity of the cooling system decreases. The power rating of the converter determines the type of heatsink to use. For low power converters, bulky natural air heatsinks are sufficient whereas high power converters require the more expensive, but smaller liquid-cooled heatsinks.

However, the latter requires a pump to circulate the coolant as well as a radiator and a fan to cool it. A heatsink typically occupies one-third of the total volume for a power converter and usually weighs more than the converter itself.

Building electronics that can withstand higher temperatures is one way of decreasing the cooling requirements,cost and size of the converter, but Si devices have reached their theoretical temperature limits.

A major source of heat affecting the vehicular electronics is heat generated by the semiconductors themselves, especially the power semiconductors. These power devices have losses associated with conducting and switching high currents. The amount of loss depends on the type of power devices utilized. In high power transportation applications, like the traction drive, Insulated Gate Bipolar Transistors (IGBT) and PiN diodes are presently used. Both are bipolar devices and have higher losses compared to their unipolar counterparts like Schottky diodes and Metal Oxide Semiconductor Field Transistor (MOSFET). Although, the aforementioned unipolar devices have superior properties compared to bipolar devices, they are not used in traction drives since they do not exist at high power ratings. Building higher voltage rating Schottky diodes and MOSFETs would not be feasible because as the breakdown voltage increases, the device requires a large silicon die area and this results in reduced manufacturing yields and increased costs. For higher breakdown voltages, a material with a higher electric breakdown field is required.

The switching frequency of the devices is also limited due to the heat generated by the devices, primarily the switching losses. Higher frequency operation is preferred because of filtering requirements, less audible noise, and smaller passive components. The outputs of high frequency power converters are smoother, and a small filter would be sufficient enough to filter the harmonics.

Additionally, with high frequency the size of the passive components decreases so there is an overall gain in size and weight. Moreover, with higher frequency, the converters could work at an inaudible frequency range, which would be comfortable for the user. While some Si bipolar devices can operate around 20 kHz and unipolar Si devices can operate at higher frequencies, the problem is that they do not exist at higher voltage or power ratings.

Why Silicon Carbide?

As seen above, increasing the effectiveness of Si to meet the needs of the transportation industry is not viable because it has reached its theoretical limits.

However, it is already proven that even the first SiC-based power devices surpass Si theoretical limits. SiC power devices can work in harsh environments where Si power devices can work in harsh environments where Si power devices cannot function. SiC power devices,

with their close-to-ideal characteristics, offer great performance. Some of the advantages compared with Si based power devices are as follows:

• SiC unipolar devices are thinner, and they have lower on-resistances. At low breakdown voltages (~ 50 V), these devices have specific on-resistances of 1.12 μΩ,around 100 times less than their Si counterparts. At higher breakdown voltages. (~ 5000 V), this goes up to 29.5 μΩ, 300 times less than comparable Si devices. With lower R_{on}, SiC power devices have lower conduction losses; therefore, higher overall converter efficiency is attainable[1-4].

• SiC unipolar devices are thinner, and they have lower on-resistances, which consequently results in lower conduction losses and therefore higher overall efficiency.

• SiC-based power devices have higher breakdown field; e.g., Si Schottky diodes are commercially available typically at voltages lower then 300V, but the first commercial SiC Schottky diodes are already rated at 600V.

• SiC has a higher thermal conductivity (4.9W/cm-k for SiC and 1.5 W/cm-k for Si); therefore , SiC power devices have a lower junction-to-case thermal resistance, R_{th-jc} (0.02 k/w for SiC and 0.06k/w for Si); therefore device temperature increase is slower.

• SiC can operate at high temperatures. SiC device operation at up to 600^{o}c is mentioned in the literature. Si devices, on the other hand, can operate at a maximum junction temperature of only 150^{o}c.

• Forward and reverse characteristics of SiC power devices vary only slightly with temperatures and time; therefore, they are more reliable.

• SiC is extremely radiation hard; i.e. radiation does not degrade the electronic properties of SiC, therefore, a SiC converter can be used in aerospace applications decreasing the weight of the vehicle due to reduced radiation shielding.

• SiC-based bipolar devices have excellent reverse recovery characteristics. With less reverse recovery current, the switching losses and EMI are reduced, and there is less or no need for snubbers. As a result, there is no need to use soft-switching techniques to reduce the switching losses[5].

• Because of low switching losses, SiC-based devices can operate at higher frequencies (> 20khz) not possible with Si-based devices in power levels of more than a few tens of kilowatts[6-9].

Although SiC has these advantages compared with Si, the present disadvantages limit its widespread use. Some of these disadvantages are

•Low processing yield because of micropipe defects. The best wafers available have <1/cm2, but they are more expensive than the typical wafer with<10/cm2 .

•High cost– The first SiC Schottky diodes (Spring 2001) cost about $50 for a 600V, 4 A Schottky diode (similar Si pn diode <<$1). Recently (Spring 2002) , the prices of SiC Schottky diodes have come down to $7/each.

• Limited availability - only Schottky diodes at relatively low power are commercially available).

• Need for high temperature packaging techniques that have not yet been developed[10].

Although SiC do have above listed advantages, it do posses some disadvantages which hinder its development. Following are some of the disadvantages:
• Processing yield is lower due to micropipe defects.
• Higher device cost due to unavailability of large wafers.
• Need for high temperature packaging technique in order to utilise SiC to its full potential.

These disadvantages are normal considering that SiC technology has not matured yet. The same disadvantages existed for Si when it was thought that it could replace germanium (Ge), and today few remember the initial processing
problems of Si. The advantages already outweigh the disadvantages. As far as the power electronics is concerned, the future will be SiC!

Silicon Carbide (SiC):

Silicon Carbide is the only chemical compound of carbon and silicon. It was originally produced by a high temperature electro-chemical reaction of sand and carbon. Silicon carbide is an excellent abrasive and has been produced and made into grinding wheels and other abrasive products for over one hundred years. Today the material has been developed into a high quality technical grade ceramic with very good mechanical properties. It is used in abrasives, refractories, ceramics, and numerous high-performance applications. The material can also be made an electrical conductor and has applications in resistance heating, flame igniters and electronic components. Structural and wear applications are constantly developing[11].

Key Properties SiC:

- ✓ Low density
- ✓ High strength
- ✓ Low thermal expansion
- ✓ High thermal conductivity
- ✓ High hardness
- ✓ High elastic modulus
- ✓ Excellent thermal shock resistance
- ✓ Superior chemical inertness

Typical Uses

- ✓ Fixed and moving turbine components
- ✓ Suction box covers
- ✓ Seals, bearings
- ✓ Ball valve parts
- ✓ Hot gas flow liners
- ✓ Heat exchangers
- ✓ Semiconductor process equipment

2.2 History of SiC:

Silicon carbide (SiC) is naturally synthesized in the atmospheres of carbon rich red giant stars and by supernova remnants. No natural crystals can be

found on Earth and therefore SiC never attracted man's interest as other crystals like diamond did.

Jons Jacob Berzelius, also known for his discovery of silicon, was most probably the first to synthesize SiC. He published in 1824 a paper in which he assumed there was a chemical bond between silicon and carbon in one of the samples he had produced [12]. But it was not before 1892 that SiC came into focus as a useful material. E. G. Acheson was looking for a suitable material that could substitute expensive diamonds needed for grinding and cutting purposes. He mixed coke and silica in a furnace and found a crystalline product characterized by great hardness, refractability, and infusibility. This product was shown to be a compound of silicon and carbon and was called "carborundum" [13].

In 1907, H. J. Round produced the first Light Emitting Diode (LED) based on SiC. He reported that "on applying a potential of 10 volts between two points on a crystal of carborundum, the crystal gave out a yellowish light" [14].

In 1912, H. Baumhauer used the word "polytype" to describe the ability of SiC to crystallize into different forms varying only in their stacking order in one direction. The evolution of SiC as an electronic material then took several decades. In 1955, Lely presented a new method to grow high quality SiC crystals. This triggered the development of SiC as a semiconductor material and SiC became even more popular than Si and Ge. However, the difficulty in obtaining high-purity SiC wafers and the rapid success of the Si technology caused a drop in the interest in SiC. In 1978, Tairov and Tsvetkov then managed to produce high purity SiC substrates by seeded sublimation growth [15]. The first SiC wafer had been made. Another major step forward was made in 1983 when Nishino, Powell, and Hill realized the first heteroepitaxy of SiC on Si [16]. In 1987, this technique was further improved and the next stage of SiC evolution started when high-quality heteroepitaxy was performed at low temperatures on off-axis substrates using "step-controlled epitaxy" [17]. Cree Inc. was founded the same year and two years later, the company introduces the world's first blue LED and began to sell SiC wafers. Along with better epitaxy, the improvement of the

diameter and quality of the wafers continued until the production of 4 inch SiC single crystals was reached in 1999. SiC Schottky diodes and high-frequency MESFETs (Metal Semiconductor Field Effect Transistor) are now commercially produced but research on electronic SiC-based devices is still active in view of many possible applications.

Applications of electronic SiC-based devices:

The requirements of present high-performance power electronic systems are exceeding the power density, efficiency, and reliability of silicon-based devices. Conventional silicon devices require heavy and bulky heat sinks to reach their operational temperature limits at approximatively 350 ◦C, are highly susceptible to harsh environments such as intense radiations, and have a switching limit in the range of a few gigahertz (GHz). On the other hand, SiC devices could operate at temperatures up to 600 ◦C, at switching frequencies in the 10-100 GHz range and at increased power densities. These lighter, more compact high density power devices operating in harsh environments or at high temperatures would meet the requirements spanning many areas of both the military and civilian sectors.

While very few SiC devices are currently commercially available, the field of power electronics attracts a lot of interest. For example, high-power converters and motor drives able to operate in harsh environments are key components in the U.S. military project of developing hybrid-electric armed robotic vehicles.

NASA is also interested in SiC power converters for spacecraft and satellite applications to increase the payload capability in lightweight solar arrays. These SiC power converters would increase the operational temperature range while reducing the required but heavy and bulky heat exchangers. Energy companies and geological exploration instrumentation would also benefit from SiC improved motor drives and sensors' capabilities in deep earth drilling where hostile environments and extreme temperatures make the use of silicon electronics impossible.

Another area where SiC superior properties are desirable is high-frequency electronics.

Most micro-wave communications and radar electronics systems currently use GaAs devices offering superior performance over silicon. However, fast-switching capability coupled with high power density and high operating temperature make SiC high-frequency devices ideal for military aircraft requiring lightweight high-performance electronic radar systems. Commercial communications industries such as air traffic control, weather radar stations and cell phone base stations, would also benefit from higher performance radio-frequency SiC devices.

Integrated circuits is yet another field where SiC is expected to play a major role. Nowadays, for example, sensor and control electronics used in conjunction with jet or rocket engines must be removed from the target area, carefully shielded, protected and cooled. SiC devices would offer for instance the possibility to mount electronic controls directly on or into a jet engine, therefore increasing reliability and performance while reducing complexity, costs, and weight. Landing long-term, fully operational probes in hostile high-temperature environments is another attractive aspect for space exploration.

Apart from these cutting-edge niche markets, domestic applications would also benefit from SiC devices' ability to work in harsch, high-temperature environments.

In the computer industry, thermal issues are the main concerns when transferring technology from the desktop system to the laptop. With transistor

junctions operating at 600 ◦C instead of 80◦C in the case of current commercial electronics, these issues would be greatly reduced. All the achievements in developing SiC technology in the case of military hybrid-electric combat vehicles could be directly applicable to domestic vehicles. And SiC devices would also allow sensor and control electronics to be mounted onboard directly on the engine block of automobiles without being shielded or kept away from the engine compartment because of thermal issues. All these possible applications rely on the superior physical properties of SiC.

2.3 Physical properties of SiC:

SiC is the only known binary compound of silicon and carbon and possesses one-dimensional polymorphism called polytypism. In a polytypic compound, similar sheets of atoms or symmetrical variants are stacked on top of each other.

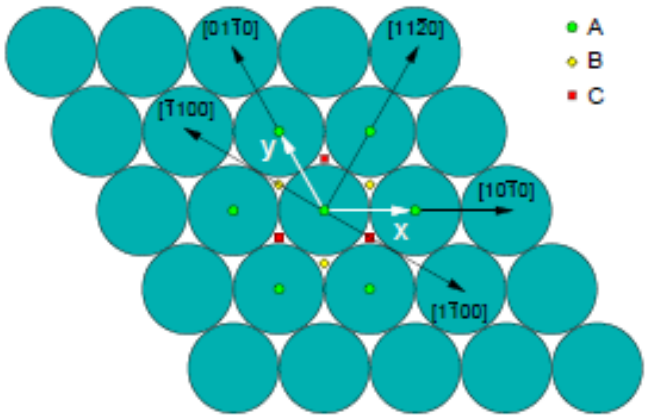


Figure 2.1: A close-packed hexagonal plane of spheres centered on points A. A second ident plane can be placed on top of the first one, with the centers of spheres over either points B or C.

The differences between the polytypes arise only in the direction perpendicular to the sheets. In SiC, each sheet represents a bilayer of C atoms right atop Si atoms. The sheets can be represented as a close-packed array of Si-C units forming a two-dimensional pattern with sixfold symmetry. Using the notations for hexagonal crystal structures, the first sheet can be defined as the basal c-plane with Miller-indexed directions according to Fig. 1.1. There are then two possibilities for arranging the second sheet on top of the first one in a close-packed configuration. The second sheet can be displaced along, for example, direction [$\bar{1}$100] until the spheres lie on positions B or along, for example, direction [1$\bar{1}$00] until the spheres lie on positions C. If a sheet is denoted A, B, C depending on the positions of its spheres, all polytypes can then

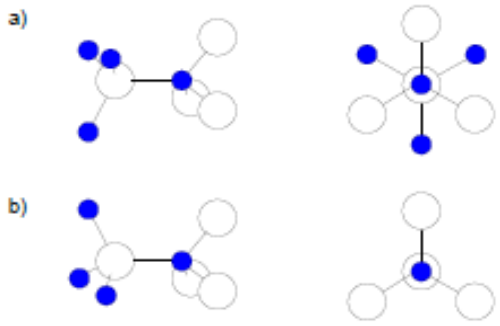


Figure 2.2: Side view and view along the stacking direction for (a) the cubic ("k") type of bond where the bonds are rotated and (b) the hexagonal ("h") type where the bonds are aligned.

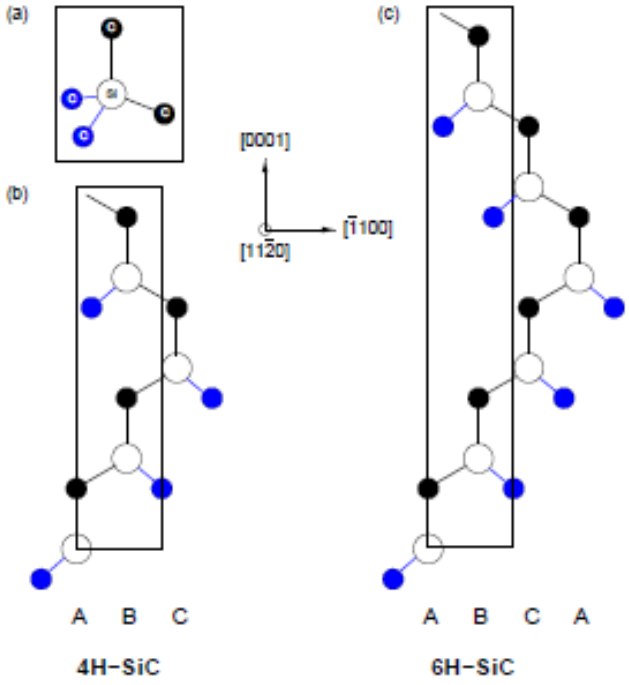


Figure 2.3: (a) The basic structural unit in SiC is a tetrahedron of four carbon atoms with a silicon atom in the middle. Stacking sequence of bilayers of Si and C atoms of (b) 4H- and (c) 6H-SiC.

The blue disks are the projections of the blue C atoms in (a) and are shown to indicate the orientations of the tetrahedra. The projection of the unit cell on the (11^{-20}) is also shown.

be described as different stackings of A, B, C sheets with the restriction thatsheets with the same rotation cannot be stacked upon each other.

In the SiC polytypes, the basic structural unit consists of a primarily covalentlybonded tetrahedron of four C (or Si) atoms with a Si (C) atom at the center.

The bond length between the Si-C atoms is approximately 1.89 °A whereas the distance between the Si-Si or C-C atoms is approximately 3.08 °A. These tetrahedra join to each other at the corners to form the SiC crystals. The tetrahedra have threefold symmetry around the axis parallel to the stacking direction. A tetrahedra stacked upon a first one can then either have the same orientation (and be called “untwinned tetrahedra”) or be rotated 180◦ around the stacking direction (“twinned tetrahedra”). This local arrangement defines a bilayer environment that can be either hexagonal (h) or cubic (k, from the german “kubisch”) [18] depending on the surrounding bilayers (Cf. Fig. 1.2).

More than 250 SiC polytypes have been identified [8], with some having stac

Table 2.1: Material properties of Si, 6H SiC, and 4H SiC at 300 K [19-38].

Property	Si	GaAs	4H-SiC	6H-SiC	2H-GaN	2H-AlN	Diamond
Bandgap at 300 K (eV)	1.11	1.43	3.26	3.02	3.39	6.2	5.45
Lattice parameters (Å)	5.43	5.65	a = 3.08 c = 10.08	a = 3.08 c = 15.12	a = 3.19 c = 5.18	a = 3.11 c = 4.98	3.56
Max. operating temp. (°C)	350	460	1200	1200			1100
Melting point (°C)	1410	1240	Sublimes > 2800	Sublimes > 2800		2275	Graphitization > 1500
Electron mobility (10^{-4} m^2/Vs)	1400	8500	900	600	900	1100	2200
Hole mobility (10^{-4} m^2/Vs)	600	400	40	40	150		1600
Breakdown electric filed (10^8 V/m)	0.3	0.4	2.2	2.5	3.3	11.8	10
Thermal cond. (W/m K)	150	54	490	490	130	200	2000
Saturation drift velocity (10^5 m/s)	1.0	2.0	2.7	2.0	2.9	1.8	2.7
Dielectric constant	11.8	12.8	10	9.7	8.9	8.5	5.5
Mohs hardness	7	4-5	9.2-9.3				10

ing sequences of several hundreds of bilayers. The crystal structures of SiC can be cubic, hexagonal or rhombohedral. In this thesis, we focus on the two polytypes particularly suited for electronics, namely 4H- and 6H-SiC. These two polytypes are named according to Ramsdell's notation [39]. where the number stands for the periodicity in the stacking direction (i.e. the number of letters A, B, C needed to define the unit cell) and the letter relates to the crystal structure, here H for hexagonal. Following the ABC notation, 4H-SiC has a stacking sequence labeled ABCB and ABCACB for 6H-SiC (Fig. 1.3). According to the notations for hexagonal crystal structures, the lattice parameter a along the [$10\bar{1}0$] is 3.08 °A for both 4H-SiC and 6H-SiC and c along [0001] is 10.06 °A and 15.11 °A for 4H-SiC and 6H-SiC, respectively (cf Ref. [40] for more details on structural parameters).

These two hexagonal polytypes share many desirable mechanical, thermal, and electronic properties.

Table 1.1 compares these quantities of primary importance in electronics to those of conventional silicon and highlights why SiC is a candidate of choice for high-temperature, high-speed, high-frequency, and high-power applications: it has a wide band gap, high thermal conductivity, high saturated electron drift velocity, and high breakdown electric field. SiC is also hard, chemically stable, and resistant to radiation damage.

For industrial purposes, SiC can be n-type doped using nitrogen or phosphorus as donors and p-type doped using boron, aluminium or gallium as acceptors.

Despite these desirable bulk properties, SiC-based devices are still facing many performance challenges.

2.4 Chemical bonding and crystal structure of SiC :

The physical and electronic properties of SiC make it an excellent semiconductor material for high temperature, radiation resistant, and high-power/high-frequency electronic devices. Electronic devices based on SiC can operate at extremely high temperatures without suffering from intrinsic conduction effects because of the wide energy band gap. Also, this property allows SiC to emit and detect short wavelength light, which makes the fabrication of blue light emitting diodes and UV photo detectors possible, even though the indirect band gap makes the efficiency low. SiC can withstand an electric field over eight times greater than Si or GaAs without undergoing avalanche breakdown. SiC is an excellent thermal conductor. At room temperature, SiC has a higher thermal conductivity than any metal. This property enables SiC devices to operate at extremely high power levels and still dissipate the large amounts of excess heat generated. SiC devices can operate at high frequencies (RF and microwave) because of the high-saturated electron drift velocity in SiC.

SiC is a IV-IV compound semiconductor with a covalent bonding of about 12% ionicity. It exist in more than 200 polytypes . The main building block for all forms is a tetrahedron consisting of a carbon atom bonded to four silicon atoms as shown in Fig.2.4

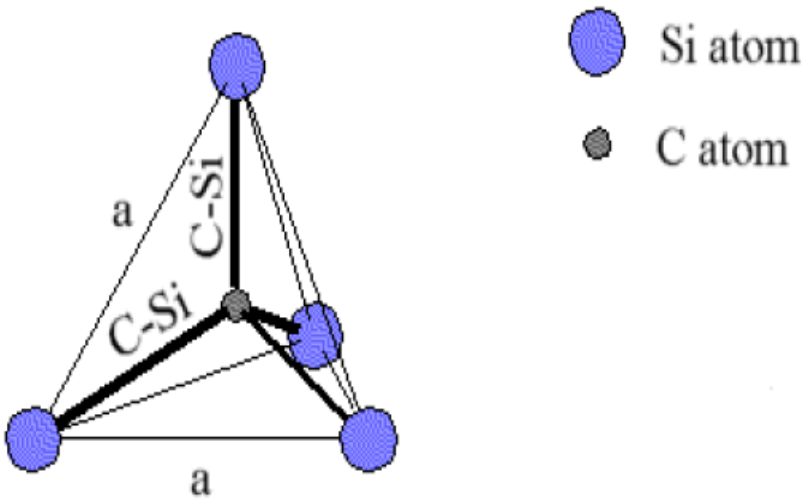


Figure: 2.4 Chemical bonding in SiC .Unit cell representation of SiC –a = 3.8A [41-42]

2.5 SiC Material Properties:

2.5.1. Crystal Structures and Polytypes:

SiC consists of both the Si and C atoms, which are group IV element materials. Each Si atom shares electrons with four C atoms, which means that each atom is bonded covalently to four neighbors, and vice versa. The basic structural unit is already shown in Fig.2.1 The approximate bond length between Si and C atoms is 1.89 Å and the length between Si-Si or C-C atoms is 3.08 Å.

SiC has a properties known as a polytypism. It means that the material can possess more than one crystal structure. Each crystal structure is called a polytype. The different polytypes are defined by the stacking sequence. For instance, 2H, 4H, and 6H is hexagonal structure and has an AB, ABAC, ABCACB stacking sequence, respectively. Similarly, 3C is cubic with ABC stacking sequence.

In Fig. 2.3 the stacking sequence is shown for the three most common polytypes ,3C,6H and 4H. If the first double layer is called the A position ,the next layer that can be placed according to a closed packed structure will be placed on the B position or the C position. The different polytypes will be constructed by permutations of these three positions. For instance will the 2H-SiC polytype have a stacking sequence ABAB … The number thus denotes the periodicity and the letter the resulting structure which in this case is hexagonal. The 3C- SiC polytype is the only cubic polytype and it has a stacking sequence ABCABC …or ACBACB …A common crystalline defect is the so called Double Positioning Boundary(DPB), which is

commonly seen in 3C-SiC grown on on –axis 6H- SiC substrates. The defect arises when is lands of the two possible stacking sequences ABCABC and ACBACB meet.

When the stacking sequence is drawn in this manner a zig zag pattern is revealed. The surrounding lattice does not, however, look the same for each position. In the Fig.2.5, the A position has a different surrounding lattice than the B and C positions. We call this position the hexagonal site, h. It is simply characterized as the turning point of the zig zag pattern.

The other two positions (B and C) are called cubic, k1 and k2. An impurity replacing a host atom at one of the three sites will obtain a different binding energy depending on the site it replaces. A very illustrative example is the nitrogen donor in 6H-SiC. The hexagonal site gives rise to the P-level of the nitrogen donor with a binding energy of approximately 85 meV. The two cubic sites will give the R- and S-levels with binding energies around 138 meV and 142 meV, respectively. In the 4H-SiC polytype there are only two in-equivalent sites, one hexagonal and one cubic (Fig.2.5). Two levels of the nitrogen donor are in this case called P and Q. In 3C there is of course only one cubic site and in 2H there is only one hexagonal site (Fig.2.5). The 6H-SiC polytype can thus be characterized as being 33% hexagonal, whereas the 4H- and 2H-SiC polytypes are 50% and 100% hexagonal, respectively.

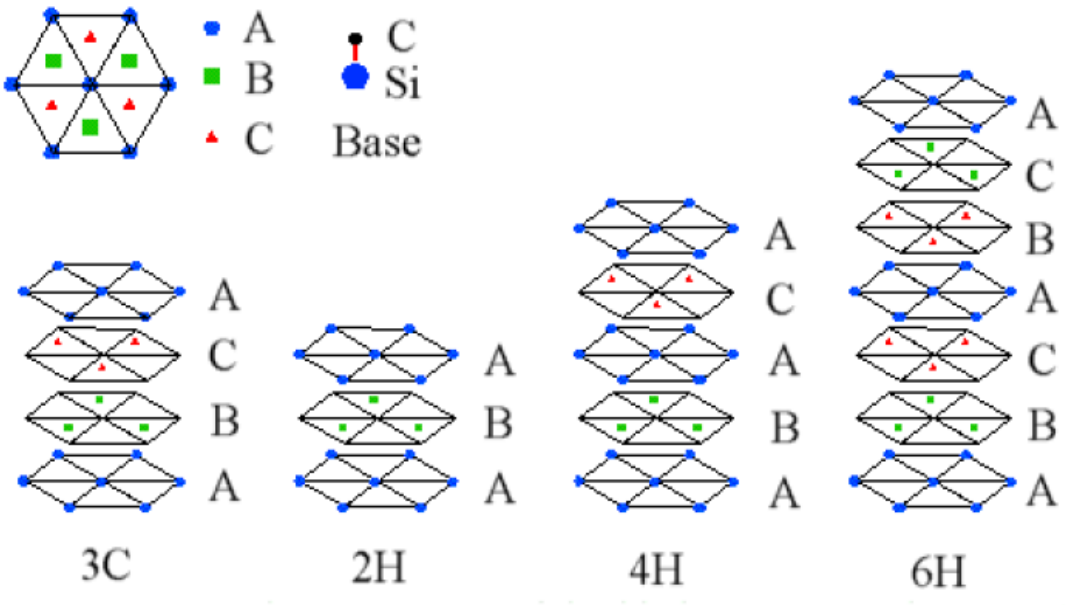
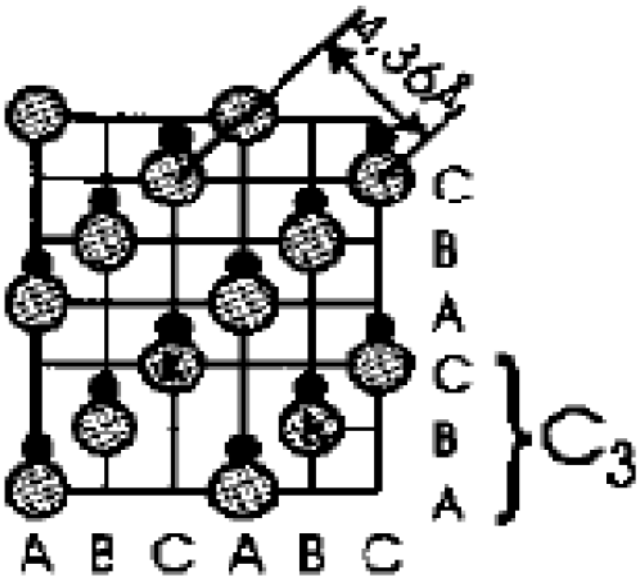


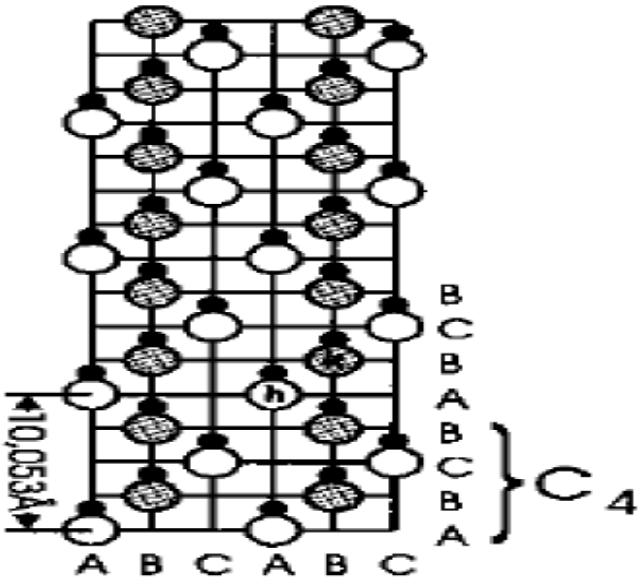
Figure. 2.5:- The stacking sequence of double layer of the three most common SiC polytypes [43].

There are basically of Silicon namely 3C ,4H, 6H. The structure is shown below in Fig. 2.6:-

a) 3C



b)4H



c)6H

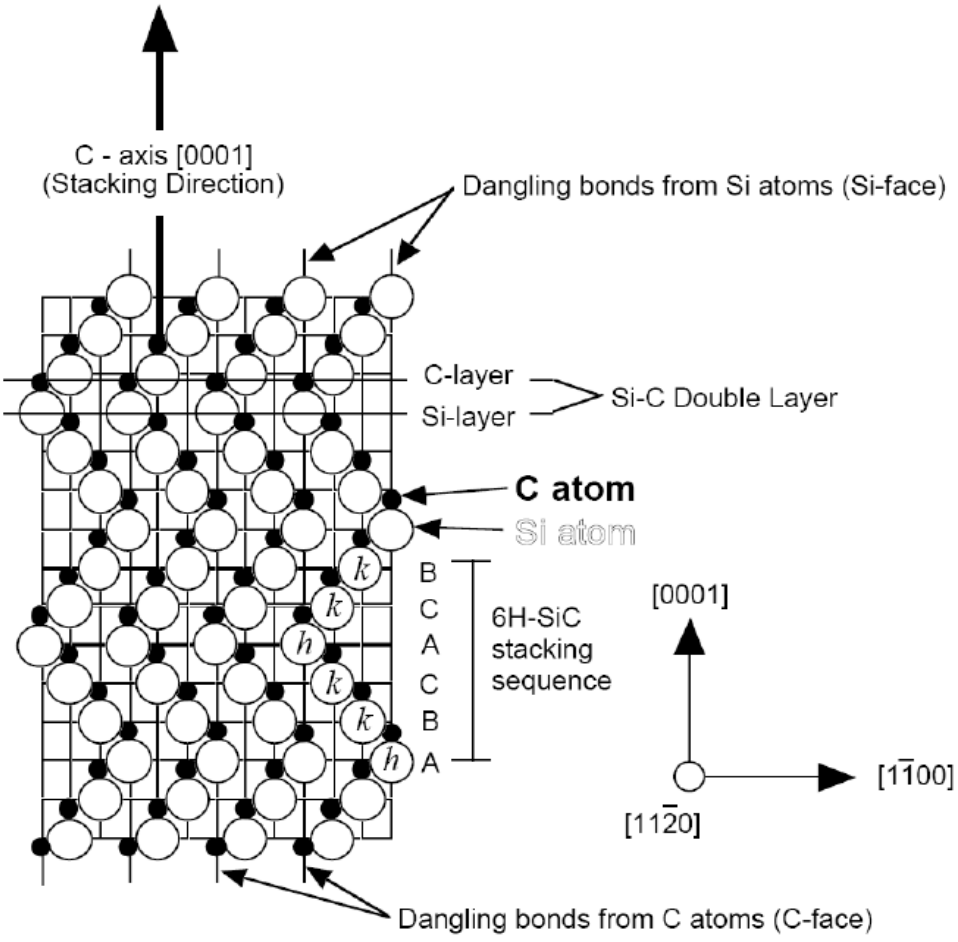


Figure:2.6 Structure of 3C,4H,6H[44]

2.5.2. SiC Structural Defects:

There is no perfect crystal. Even in the thermodynamic equilibrium a crystal structure contains point defects by the absence of atoms or presence of extra atoms. In a compound semiconductor such as SiC, antisite defect, i.e. Si substitutes for C sites and vice versa, will be also present. These defects may alter the electrical and optical properties.

If a host atom is removed from the lattice, a vacancy is formed. This results in four unsaturated bonds, which have impact on electrical properties of the crystal. If the atom is inserted (either host or impurity atom) into an interstitial site, Schottky interstitial is formed. In the case of the interstitial atom staying in the vicinity of the vacancy, the Frenkel interstitial is formed. The distortion energy associated with the interstitials is reduced.

Dislocations are one-dimensional line defects and they extend through the entire

lattice. There are two main types of dislocations, with screw and edge character. The specification depends on the mechanism of their formation and the so-called Burgers vector b. The dislocation is a local distortion of the crystal and due to stress. It is required to move by one lattice constant. An edge dislocation is formed by removing from the crystal a half of atoms plane terminating on the dislocation line and then joining the two planes in the way to restore order in the crystal, see Fig.2.7.

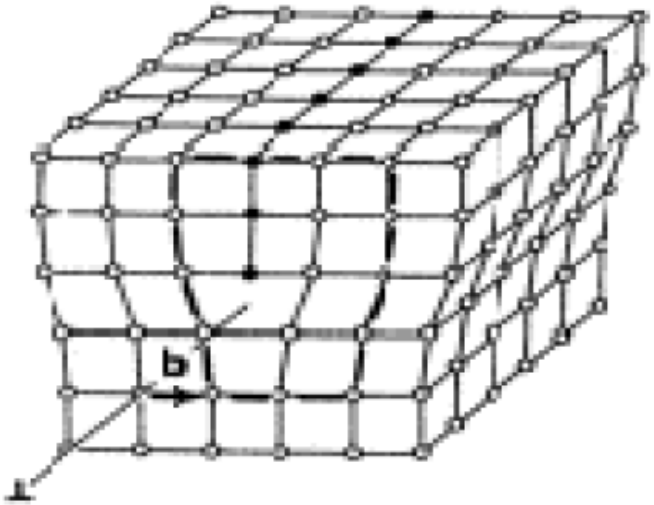


Figure 2.7 Edge dislocation

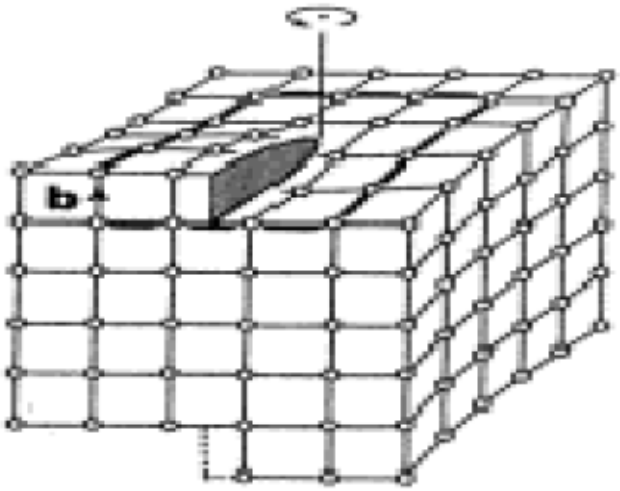


Figure 2.8 Screw dislocation

A screw dislocation can be explained in the following manner. The crystal has been slipped above the dislocation line by a lattice vector parallel to the line and then rejoined to the part below the dislocation line to restore crystalline order, see Fig.2.9. To define a Burgers vector one considers a closed contour in the perfect crystal passing over the lattice sites containing a series of Bravais vectors. The same sequence of the Brava is vectors is traversed onto the location around the dislocation
line. If the series is not completed i.e. the contour is not closed, the remaining Bravais vector, is called the Burgers vector b of the dislocation. For the edge dislocation the Burgers vector is perpendicular to the dislocation line, while for the screw dislocation it is parallel (compare Fig.2.8 and Fig.2.9). Dislocations influence crystal growth and they have impact on electron transport and mechanical properties.
A structural defect, which has attracted most attention in the SiC research, is the micropipe. It is a hollow core propagating along the [0001] direction. The diameter of the micropipe is several or tens of micrometers. The usual density in the bulk crystals varies between $10 - 100\mathrm{cm}^{-2}$. The recent scientific reports show a tremendous decrease in the micro pipe density to as low as $1.1\,\mathrm{cm}^{-2}$. in 2 inch wafers [45].
This severe defect tends to agglomerate into groups and/or at domain boundaries, while there are large areas where the micropipe densities approach zero. The micropipes are known to degrade the device performance and yield, e.g. they reduce the breakdown voltage of Schottky diodes [46, 47].

2.6 Crystal Growth Basis of SiC:

At present the research in crystal growth centers around increasing the growth rate, increasing the wafer diameter, and reducing material defects. In 1955, a laboratory sublimation process for growing a-SiC crystals was developed. In this process the nucleation of individual crystals is uncontrolled and the resulting crystals are randomly-sized hexagonal-shaped a-SiC platelets[48].To avoid this type of defect the modified sublimation process for growing SiC single crystals is introduced.

In 1987, a research group under R. F. Davis at North Carolina State University (NCSU) announced the successful implementation of a seeded growth sublimation process , a modification to the original sublimation process[49].

In the modified sublimation process, only one large crystal is grown, and this crystal consists of a single polytype. In this process, which is the basis of current commercial growth systems, a charge of polycrystalline SiC is heated in a graphite crucible containing argon at 200 Pa. A temperature gradient is established, with the polycrystalline SiC at about 2400 C and a seed crystal at about 2200 C. At these temperatures, SiC sublimes from the polycrystalline source and condenses on the cooler seed crystal.

The students from the NCSU group founded a small company, Cree Research, to produce SiC wafers commercially. In 1990 single crystal wafers of 6H-SiC were introduced. At present, 35 mm diameter wafers of both 4H and 6H SiC are commercially available from Cree Research (Durham, NC, USA) and from Advanced Technology Materials, Inc. (Danbury, CT, USA) [50].

The modified method is currently used to produce commercial grade 4H-SiC. Limited progress has been made in producing 3C-SiC substrates in the laboratory using 3C-SiC seeds grown by chemical vapor deposition (CVD) on Si wafers. Difficulties in producing 3C-SiC wafers by sublimation method may be due to high temperatures used in the sublimation method, which promote the crystallization of hexagonal and rhombohedral polytypes.

Polycrystalline SiC wafers can be fabricated using sintered pressed powders or using CVD.

2.6.1 Epitaxial Growth:

Chemical Vapor Deposition (CVD) is undoubtedly the most common technique for growing epitaxial SiC films. 6H-SiC and 4H-SiC are grown homoepitaxially on 6H-SiC and 4H-SiC wafers respectively. 3C-SiC is usually grown heteroepitaxially on Si or on 6H-SiC. Growth of 3C-SiC on Si substrates has been demonstrated in the 1960s using processes that were based on carbonization of Si at high temperatures in a hydrocarbon gas. The carbonization process is self limiting; therefore growth of only very thin films, of the order of hundreds of nanometers is practical. For a thicker film, a two step deposition process is employed where; step two involves film growth using silicon containing precursor gas. Modified CVD technique capable of growing films up to 100 microns thick with a background doping level of 1x10e14 cm-3. However single crystalline 3C-SiC grown on Si substrates has a lot of defects due to lattice mismatch etc.

2.6.2 Selective Doping:

Since the diffusion coefficients of aluminum and nitrogen are so low that thermal diffusion is impractical due to this selective doping of SiC is accomplished by ion implantation. The two Common p-type dopants, aluminum and boron, produce relatively deep acceptor levels (211 meV and 300 meV respectively), but aluminum is generally used because of its smaller ionization energy[18]. To minimize amorphization during implantation, it is common to implant at elevated temperatures, typically around 650 C for nitrogen and up to 1100 C for aluminum. Boron can be successfully implanted at room temperature [51].

2.6.3 Ohmic Contact Formation:

Ohmic contacts are of great importance to power devices, since the high current densities give rise to intolerable voltage drops across even small resistances. Ohmic contacts to n-type material are typically formed by annealed nickel. The contacts are annealed at high temperatures, typically between 850 - 1050 C, in argon or vacuum.

Specific contact resistivities < 5x10-6 Ohm-cm2 can be obtained to heavily doped n-type layers .Contacts to p-type material have been more difficult. The p-type contacts are typically formed by annealed aluminum, or by a bilayer of aluminum covered with titanium.

Anneal temperatures are similar to those used for nickel contacts, but the contact resistivities are in the 10-3 to 10-5 Ohm-cm2 range, depending on doping density . Very recently, Ostling and Lundberg reported contact resistivities to p-type 6HSiC in the mid-10-6 Ohm-cm^2 range using sequential electron beam evaporation of cobalt and silicon, followed by a two-step vacuum annealing process at 500 C and 900C. The thermal integrity of the metallization system is of importance for high temperature applications. Nickel ohmic contacts used for n-type material have been shown to be stable to very high temperatures (negligible change in resistance after 329 hours at 650 C or after short thermal cycles to 1300 C) but aluminum ptype

contacts will not be capable of high temperature operation.

2.6.4 Silicon Carbide Production:

Silicon Carbide is derived from powder or grain, produced from carbon reduction of silica. It is produced as either fine powder or a large bonded mass, which is then crushed. To purify (remove silica) it is washed with hydrofluoric acid.

There are three main ways to fabricate the commercial product. The first method is to mix silicon carbide powder with another material such as glass or metal, this is then treated to allow the second phase to bond. Another method is to mix the powder with carbon or silicon metal powder, which is then reaction bonded. Finally silicon carbide powder can be densified and sintered through the addition of boron carbide or other sintering aid. It should be noted that each method is suited to different applications.

2.7 Advantage of SiC Devices:

The most beneficial advantages that SiC-based electronics are in the areas of high temperature device operation and high-power device operation.

2.7.1 High Temperature and Power Operation:

Silicon carbide is not attacked by any acids or alkalis or molten salts up to 800°C. In air, SiC forms a protective silicon oxide coating at 1200°C and is able to be used up to 1600°C. The high thermal conductivity coupled with low thermal expansion and high strength give this material exceptional thermal shock resistant qualities. The wide band gap energy and low intrinsic carrier concentration of SiC allow SiC to maintain semiconductor behavior at much higher temperatures than silicon .

The high breakdown field and high thermal conductivity of SiC coupled with high operational junction temperatures theoretically permit extremely high power densities and efficiencies to be realized in SiC devices. Figures 1.5 and 1.6 demonstrate the theoretical advantage of SiC's high breakdown field compared to silicon in shrinking the drift-region and associated parasitic on-state resistance of a 3000 V rated unipolar Power MOSFET device [52],[53]. The high breakdown field of SiC relative to silicon enables the blocking voltage region to be roughly 10 times thinner and 10 times heavier-doped, permitting a roughly 100-fold decrease in the dominant blocking region (N-Drift Region) resistance R_D of Figure1.5 for the SiC device relative to identically rated 3000 V silicon Power MOSFET [54].

2.8. Drift Diffusion Modeling and Numerical Analysis:

In this chapter, I will present the drift-diffusion model which serves as the basis for the

numerical simulation of a SiC MOSFET device. I begin by reviewing the drift-diffusion equations and how they are used for the specific case of simulating a MOSFET device. I will also present the discretization scheme for these equations and the numerical methods that have been used to solve them.

2.8.1.Drift Diffusion Model:

The drift diffusion equations serve as the basic building blocks for semiconductor device modeling and can be derived directly from Maxwell's equations and the Boltzmann transport equation of kinetic theory. They are, in essence, equations derived from the Boltzmann transport equation by doing certain approximations. The drift diffusion equations consist of the Poisson's equation, the equations for electron and hole currents, and the current continuity equations for electrons and holes. In this section, These equations have been described in brief and then elaborated a little on the numerical methodology that is implemented to solve them for a SiC MOSFET device.

The drift diffusion equations serve as the basic building blocks for semiconductor device modeling and can be derived directly from Maxwell's equations for electromagnetic radiation and the Boltzmann transport equation of kinetic theory. They are, in essence, equations derived from the Boltzmann transport equation by doing certain approximations. The drift diffusion equations consist of the Poisson's equation, the equations for electron and hole currents, and the current continuity equations for electrons and holes. In this section, These equations have been described in brief and then elaborate a little on the numerical methodology that is implemented to solve them for a SiC MOSFET device.

2.8.1.a. Poisson's Equation:

The first of the drift-diffusion equations is the Poisson's equation. It relates the electrostatic potential (∅), to the net charge density (ρ) inside a semiconductor [52][53][54][56].

$$\vec{\nabla}.\left(\varepsilon\vec{\nabla}\emptyset\right) = -\rho \qquad (2.1)$$

ρ is the net charge density and ε is the dielectric permittivity of the material in which the charge

is present. Inside the semiconductor, the charge particle concentration consists of negatively

charged electron concentrations (n), positively charged hole concentrations (p) and the ionized
dopant concentrations (D). The dopants are further separated into positively charged donors (N_D^+)
and the negatively charged acceptors (N_A^-). Substituting these values for the net charge density,
the Poisson equation can be rewritten as:

$$\vec{\nabla}.\left(\varepsilon\vec{\nabla}\emptyset\right) = -q(n - p - D) \qquad (2.2)$$

where, q is the net charge on a single electron, and

$$D = N_D^+ - N_A^- \qquad (2.3)$$

The electron (n) and hole (p) concentrations are written in terms of the electron and hole quasi-Fermi levels ($\emptyset n$ and $\emptyset p$).

$$n = n_i \exp\left(\frac{\emptyset - \emptyset_n}{V_T}\right) \qquad (2.5)$$

where, n_i is the intrinsic carrier concentration and V_T is the thermal voltage.

2.8.1.b. Current Equations:

There are two phenomena causing current flow in a semiconductor: (i) Drift and (ii) Diffusion. Presence of an electric field in a semiconductor will cause the free electrons and holes to drift along the field lines. This method produces a current which is known as the drift current.

If there is concentration gradient of the electron or hole concentrations, the electrons and holes will flow from the higher concentration region to their lower concentration region generating a current. This current is termed as the diffusion current. The contribution of carrier transport due to drift can be formulated as:

$$\vec{J}_{n_{drift}} = -qn\,\overrightarrow{v_n} \qquad (2.6)$$

$$\vec{J}_{p_{drift}} = -qn\,\overrightarrow{v_p} \qquad (2.7)$$

where $\overrightarrow{v_n}$ and $\overrightarrow{v_p}$ are the drift velocities of electrons and holes respectively, due to an applied electric field. These velocities can be expressed in terms of the mobilities (μ_n and μ_p), and the applied field ($\overrightarrow{E}$).

$$\overrightarrow{v_n} = \mu_n \overrightarrow{E} \quad (2.8)$$

$$\overrightarrow{v_p} = \mu_p \overrightarrow{E} \quad (2.9)$$

The diffusion component of carrier transport is due to random and gradients in the mobile charge concentration, and is described by the following:

$$\vec{J}_{n_{diff}} = -q\nabla(nD_n) \quad (2.10)$$

$$\vec{J}_{n_{diff}} = -q\nabla(nD_p) \quad (2.11)$$

D_n and D_p are the electron and hole diffusion coefficients respectively. They can be related to the electron and hole mobilities by Einstein relations:

$$D_n = \mu_n \frac{k_B T}{q} \quad (2.12)$$

$$D_p = \mu_p \frac{k_B T}{q} \quad (2.13)$$

Here, k_B is the Boltzmann's constant, and T is the temperature.

Combining both, drift and diffusion components, the total expression for the electron and hole currents inside a semiconductor is given as:

$$\vec{J}_n = \vec{J}_{n_{drift}} + \vec{J}_{n_{diff}} = qn\mu_n \overrightarrow{E} + q\vec{\nabla}(nD_n) \quad (2.14)$$

$$\vec{J}_p = \vec{J}_{p_{drift}} + \vec{J}_{p_{diff}} = qp\mu_p \overrightarrow{E} + q\vec{\nabla}(pD_p) \quad (2.15)$$

Writing the electric field E as a gradient of the electrostatic potential, $\overrightarrow{E} = -\vec{\nabla}\emptyset$, the current equations can be rewritten as:

$$\vec{J}_n = -qn\mu_n + q\vec{\nabla}\emptyset(nD_n) \quad (2.16)$$

$$\vec{J}_p = -qp\mu_p + q\vec{\nabla}\emptyset(pD_p) \quad (2.17)$$

2.8.1.c. Continuity Equations:

The continuity equations are based on the conservation of mobile charge. They relate the time change in mobile charge concentration to the gradient of the current density, and the rates of generation and recombination of carriers. For electrons, the continuity equation is written as,

$$\frac{\partial n}{\partial t} = \frac{1}{q}\vec{\nabla}.\vec{J}_n - R_n + G_n = 0 \quad (2.18)$$

The continuity equation for holes is given by

$$\frac{\partial p}{\partial t} = \frac{1}{q}\vec{\nabla}.\vec{J}_p - R_p + G_p = 0 \quad (2.19)$$

where G_n and G_p are the electron and hole generation rates, R_n and R_p are the electron and hole recombination rates respectively, and $\vec{\nabla}.\vec{J}_n$ and $\vec{\nabla}.\vec{J}_p$ are the net flux of electrons and holes in and outof the specific volume. The current continuity equations simply state that the total current flow into or out of a volume of space is equal to the time varying charge density within that volume plus any additions due to generation or recombination that may occur.

2.8.1.d. Steady State Drift Diffusion Model:

In steady state, there is no net change in electron and hole concentration over time.
Hence, the continuity equations for electrons and holes can be equated to zero.

$$\frac{\partial n}{\partial t} = \frac{1}{q}\vec{\nabla}.\vec{J}_n - R_n + G_n = 0 \quad (2.20)$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\vec{\nabla}.\vec{J}_p - R_p + G_p = 0 \quad (2.21)$$

Substituting the formulae for $\vec{J}_n$ and $\vec{J}_p$ from the current equations in the above equations, we have,

$$\vec{\nabla}.\left[-n\mu_n\vec{\nabla}\emptyset + \vec{\nabla}(nD_n)\right] - R_n + G_n = 0 \quad (2.22)$$

$$\vec{\nabla}.\left[-p\mu_p\vec{\nabla}\emptyset + \vec{\nabla}(pD_p)\right] - R_p + G_p = 0 \quad (2.23)$$

Equations 2.20 and 2.21 together with the Poisson's equation (2.1) form the steady state drift diffusion system of equations. These equations are to be solved for the electrostatic potential(∅), the electron concentration (n) and the hole concentration (p) inside the device. It is apparent from the above equations that the mobility, generation and recombination of electrons and holes play important roles in the physics of carrier transport in a device.

2.8.1.e. Generation and Recombination:

For SiC MOSFET simulation, two types of recombination mechanisms have been modeled. The recombination occurring due to trap centers (Shockley-Read-Hall) and due to direct particle recombination (Auger). The generation of particles due to impact ionization is also included.

Shockley-Read-Hall (SRH) Recombination:

The capture and emission of holes and electrons by traps that reside in the mid-band energy zone is modeled using the well known Shockley-Read-Hall (SRH) recombination mechanism. The SRH recombination rate is given by

$$R^{SRH} = \frac{np - n_i^2}{\tau_p(n+n_i)+\tau_n(p+n_i)} \quad (2.24)$$

where, τ_n and τ_p are the minority carrier lifetimes of electrons and holes respectively. Theminority carrier lifetimes for SiC are on order of a few nanoseconds. They are typically around two orders of magnitude less than those for Si.

For a n-doped SiC slab, when there is a current flowing through the device, the electron concentration is much higher than the hole concentration (n >> p). If the carrier lifetimes of

electrons and holes are taken to be equal $(\tau_n \approx \tau_p)$, then the SRH recombination rate can be written as

$$R^{SRH} \approx \frac{np}{\tau_p n} = \frac{p}{\tau_p} \qquad (2.25)$$

At room temperature, the intrinsic carrier concentration of 4H-SiC is around $2\times10^{-8}\text{cm}^{-3}$.

For a slab of SiC doped with n-type impurity of the order of 10^{18} donor atoms per cubic centimeters, at room temperature, the hole concentration is going to be around $(10^{-8})^2/10^{18}$ which is approximately 10^{-30}cm^{-3}. Hence, it is easy to see that the SRH recombination rate in SiC is going to be very small (around $10^{-20}\text{cm}^{-3}/\text{s}$).

Auger Recombination:

SiC is an indirect bandgap semiconductor. Hence the probability of a direct band-to-band recombination by transfer of energy to another carrier is very small. Hence, this recombination mechanism, known as the Auger recombination is rare in SiC devices. In the direct recombination process, a free electron in the conduction band combines with a free hole in the valence band, and the net momentum of the two particle system is carried off by a third free particle, which can be an electron or a hole. The Auger recombination rate is given by

$$R^{Auger} = (np - n_i^2)(c_n n + c_p p) \qquad (2.26)$$

where, $c_n$and $c_p$are the coefficients representing interactions in which the remaining carrier isan electron and a hole respectively.

Impact Ionization Generation:

Generation of particles occurs when a particle with high energy collides with a bonded particle resulting in one additional free electron and one additional free hole. This type of generation is referred to as impact ionization generation. In SiC, it is seen that the free particles do not attain very high energy due to the very high bandgap. Hence, the impact ionization generation rate is very small. The impact ionization generation rate is modeled as proportional to the carrier current density [57].

$$G^{II} = \frac{1}{q}(\alpha_n \left|\vec{J}_n\right| + \alpha_p \left|\vec{J}_p\right|) \quad (2.27)$$

$$\alpha_{n,p} = \alpha_{n,p}^{\infty} \exp\left(\frac{-b_{n,p}}{|\vec{E}|}\right) \quad (2.28)$$

$G^{II}$is the net impact ionization generation rate, $a_{n(p)}$ is the per unit length generation coefficient for electrons (holes), and $b_{n(p)}$ is the electric field at which impact ionization generation becomes significant.

2.8.2. Numerical Methods for Drift-Diffusion Simulation of SiC MOSFETs:

In this section I will describe the numerical methods used for solving the drift diffusion equations for the specific case of a SiC MOSFET device. In order to solve the coupled partial differential equations comprising the drift diffusion system of equations, a proper methodology has to be followed. The equations are solved for 2D structure, which is a section cut parallel to the channel of the MOSFET. These equations are solved for the electrostatic potential($\emptyset$), the electron concentration (n) and the hole concentration (p) at discreet mesh points inside the device,in the source, drain, bulk and the oxide regions. Appropriate boundary conditions for $\emptyset$, n and p,based on the applied voltages at the various regions, are built in to the system.

2.8.2.a. Boundary Conditions:

The MOSFET device structure is shown in figure 2.1. It is divided into the source, the drain, the bulk, the oxide and the interface regions, where the semiconductor equations are to be solved. The boundary regions are the regions where external voltage is applied or an artificial boundary is created.

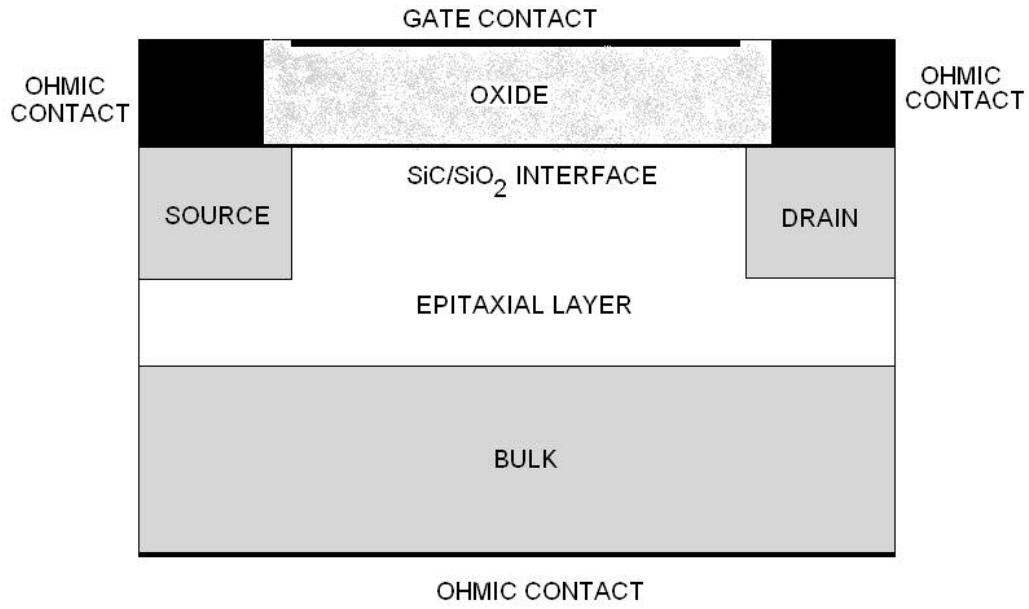


Figure 2.9. 4H-SiC MOSFET device structure.

Ohmic Contact:

The source, bulk and drain contacts shown in figure 2.1 are modeled as Ohmic contacts.
It means, there is no resistance of the contact itself. Hence, all the voltage applied at these contacts is transferred to the semiconductor below. The boundary condition for the electrostatic potential is therefore given by

$$\emptyset_c = V_c + \emptyset_n \qquad (2.29)$$

for Ohmic contacts on n-type material and

$$\emptyset_c = V_c + \emptyset_p \qquad (2.30)$$

for Ohmic contact on p-type material.

Here, $\emptyset_n$ and $\emptyset_p$ are the built in potentials for n-type and p-type semiconductors in thermal equilibrium. For an n-type material with a doping of N_D^+, the built in potential is simply

$$\emptyset_n = V_T \ln \frac{N_D^+}{n_i} \qquad (1.31)$$

and for a p-type semiconductor doped of N_A^-, the built in potential is

$$\emptyset_p = -V_T \ln \frac{N_A^-}{n_i} \qquad (2.32)$$

where, n_i is the intrinsic carrier concentration at temperature T and V_T is the thermal voltage.

As there is no power loss in the Ohmic contact, and the carriers are at thermal equilibrium, we can say that there exists charge neutrality in the contact volume. Hence, the total charge density is equal to zero.

$$\rho = q(p - n + D) = 0 \qquad (2.33)$$

Where, $D = N_D^+ - N_D^-$

Since we are at thermal equilibrium, $np = n_i^2$. Hence, for a n-type semiconductor at the Ohmic contact,

$$p = \frac{n_i^2}{n} \qquad (2.34)$$

And

$$n = \frac{D}{2} + \frac{\sqrt{D^2 + 4n_i^2}}{2} \qquad (2.35)$$

Similarly, for a p-type semiconductor region at the Ohmic contact,

$$p = \frac{n_i^2}{p} \qquad (2.36)$$

And

$$p = \frac{-D}{2} + \frac{\sqrt{D^2 + 4n_i^2}}{2} \qquad (2.37)$$

2.9. Gate Contact:

There are no mobile charge carriers inside the gate oxide. Hence, only the Poisson's equation is solved inside the oxide with the zero charge density considered. The semiconductor equations are not solved for n and p inside the oxide; hence no boundary conditions are needed for n and p at the gate contact. The boundary condition for the electrostatic potential on the gate contact is defined as:

$$\emptyset_G = V_G + VGB \qquad (2.38)$$

V_G is the applied gate voltage and VGBis the built-in gate voltage. It is equal to the metal-semiconductor work function difference between the gate metal and the semiconductor epilayer of the 4H-SiC MOSFET. The 4H-SiC MOSFET used for measurements has a n-type polysilicon gate doped at $10^{20}\text{cm}^{-3}$and an p-type epilayer doped at $5 * 10^{15}\ \text{cm}^{-3}$. Hence, as shown in Figure 2.2, the work function, which is the difference between the Fermi levels of the polysilicon gate and the 4H-SiC epilayer, can be written as:

$$E_F^{si} = x_{si} + \frac{E_g^{si}}{2} - \psi_B^{si}$$

$$= x^{si} + \frac{E_g^{si}}{2} - k_B T \ln\left(\frac{N_D^{poly}}{n_i^{si}}\right) \qquad (2.39)$$

$$= 4.06\text{eV}$$

$$E_F^{4H-sic} = x^{4H-sic} + \frac{E_g^{4H-sic}}{2} - +\psi_B^{4H-sic}$$

$$= x^{4H-sic} + \frac{E_g^{4H-sic}}{2} + k_B T \ln\left(\frac{N_A^{epi}}{n_i^{4H-sic}}\right) \qquad (2.40)$$

$$= 6.97\text{eV}$$

$$\phi_{MS} = -q\left(E_F^{si} - E_F^{4H-sic}\right) = 2.91 = VGB \qquad (2.41)$$

Here,$x_{si} = 4.05\text{eV}$, $x_{4H-SiC} = 3.95\text{eV}$, $E_g^{si} = 1.1\text{eV}$, $E_g^{4H-SiC} = 3.2\text{eV}$, $N_D^{poly} = 10^{20}\text{cm}^{-3}, N_A^{epi} = 5 * 10^{15}\text{cm}^{-3}, n_i^{si} = 1.2 * 10^{10}\text{cm}^{-3}, n_i^{4H-SiC} = 1.88 * 10^{-8}\text{cm}^{-3}, T = 300^0\text{K}, q = 1.6 * 10^{-19}\text{C},$ and $k_B = 1.38 * 10^{-23}\text{J}^0\text{K}^{-1}$

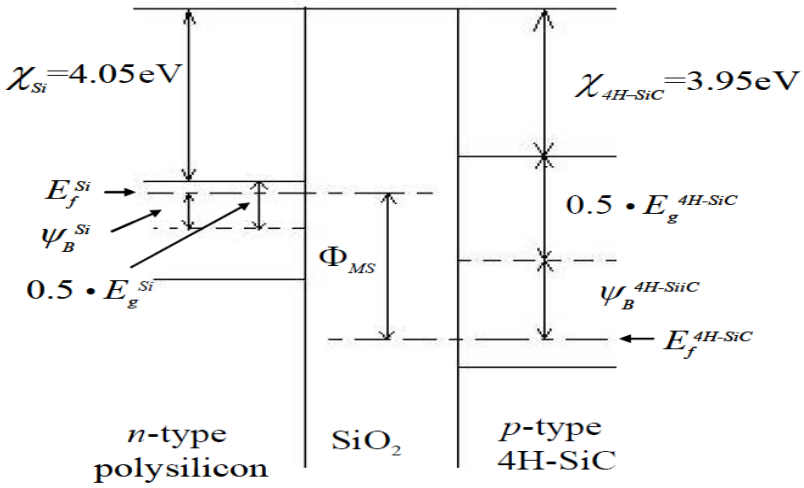


Figure 2.10. Work function difference between n-type polysilicon gate and p-type epi-layer 4H-SiCMOSFET.

2.10.Artificial Boundaries:

Artificial boundaries consist of all boundaries in which the device structure ceases to exist for simulation purposes, but in reality, this boundary may not exist on the device physically.

The artificial boundaries are placed far enough away from the carrier transport activity where the change in electrostatic potential, electron concentration and hole concentration, across the boundary, is negligible. Hence at the artificial boundaries, we have the conditions

$$\frac{\partial \emptyset}{\partial \mathrm{N}} = \frac{\partial \mathrm{n}}{\partial \mathrm{N}} = \frac{\partial \mathrm{p}}{\partial \mathrm{N}} = 0 \qquad (2.42)$$

Where $\frac{\partial}{\partial \mathrm{N}}$ is the derivative taken in the direction normal to the artificial boundary.

2.2.2. Finite Difference Discretization of the Semiconductor Equations:

In order to solve the system of coupled differential equations comprising the drift diffusion model, each equation must be discretized in space. The Poisson's equation is solved inside the semiconductor and the oxide, whereas the current continuity equations are solved only inside the semiconductor. At the semiconductor-oxide interface, the Gauss's law is implemented in order to solve for the electrostatic potential.

Each equation is discretized in two dimensions using the finite difference method where each position, (x, y), in the device is mapped to a mesh point, (i , j). The position of x, at the i^{th} mesh line is designated by the notation x_i; likewise, the position of y, at the j^{th} mesh line is designated by the notationy_j.

If necessary, additional points can be defined as lying between two consecutive mesh points. These points are designated by$\left(i \pm \frac{1}{2}, j\right)$ or$\left(i, j \pm \frac{1}{2}\right)$. The distance between two mesh points are designated by the variables $h_i$andk_j.

$$h_i = x_{i+1} - x_i \qquad (2.43)$$

$$k_j = y_{j+1} - y_j \qquad (2.44)$$

Other variables will be defined for the purposes of simplifying the writing of the discretized equations.

2.10.1.Poisson's Equation :

Poisson's equation gives an analytical representation of the relationship between electrostatic potential ($\emptyset$) and the net charge distribution.

Semiconductor-Insulator Interface

At the semiconductor-oxide interface, it is assumed that there are no free electrons and holes, and that the difference in the electric displacement vectors in the insulator and the semiconductor is equal to the effective surface charge.

$$\hat{a}_{surf} - (\vec{D}_i - \vec{D}_S) = Q_{surf} \qquad (2.45)$$

where, $\vec{D}$ is the electric displacement vector and Q_{surf} is the effective surface charge density at

the semiconductor-oxide interface, and $\hat{a}_{surf}$ is a unit vector in the direction of the semiconductor-oxide interface.

This equation can be rewritten in form of Gauss's law by writing the electric fields at the semiconductor-oxide interface.

$$\boldsymbol{\varepsilon_{ox}E_{ox} - \varepsilon_s E_s = Q_{surf}} \qquad (2.46)$$

Here, the electric fields are the fields perpendicular to the interface. Writing them using the electrostatic potentials, we have

$$\boldsymbol{\varepsilon_{ox}\left(-\frac{\partial \emptyset}{\partial y}\right)_{ox} - \varepsilon_s\left(-\frac{\partial \emptyset}{\partial y}\right)_s = Q_{surf}} \qquad (2.47)$$

Writing the discretized forms of the first order derivatives we have the equation for the electrostatic potential at the interface.

$$\boldsymbol{F^{\emptyset}_{i,j_{ox}} = \emptyset_{i,j_{ox+1}}\left(\frac{\varepsilon_s}{k_{j_{ox}}}\right) + \emptyset_{i,j_{ox-1}}\left(\frac{\varepsilon_{ox}}{k_{j_{ox-1}}}\right) - \emptyset_{i,j_{ox}}\left(\frac{\varepsilon_s}{k_{j_{ox}}} + \frac{\varepsilon_{ox}}{k_{j_{ox-1}}}\right) + Q_{surf} = 0} \qquad (2.48)$$

where, $\boldsymbol{j_{ox}}$ represents the mesh-line j which defines the interface. Q_{surf} is the net effective surface charge at the mesh-point $(\boldsymbol{i, j_{ox}})$. It is the sum of the fixed oxide charge and the interface trapped charge at that mesh-point**.**

Inside the Oxide

There is no charge present inside the oxide. Hence, the Poisson's equation will look like a simple Laplacian.

$$\boldsymbol{\nabla^2 \emptyset = 0} \qquad (2.49)$$

Finite difference discretization of the above equation has the following form.

$$\boldsymbol{F^{\emptyset}_{i,j} = \frac{\emptyset_{i+1,j}}{h_1^2} + \frac{\emptyset_{i-1,j}}{h_2^2} + \frac{\emptyset_{i,j+1}}{k_1^2} + \frac{\emptyset_{i,j-1}}{k_2^2} - \emptyset_{i,j}\left(\frac{1}{h_1^2} + \frac{1}{h_2^2} + \frac{1}{k_1^2} + \frac{1}{k_2^2}\right) = 0} \qquad (2.50)$$

where,

$$\boldsymbol{h_1^2 = \frac{h_1(h_i + h_{i-1})}{2}}, \boldsymbol{h_2^2 = \frac{h_{i-1}(h_i + h_{i-1})}{2}}, \boldsymbol{k_1^2 = \frac{k_1(k_j + k_{j-1})}{2}}, \boldsymbol{k_2^2 = \frac{k_{j-1}(k_j + k_{j-1})}{2}} \qquad (2.51 - 54)$$

Inside the Semiconductor

Rewriting the Poisson's equation inside the semiconductor,

$$\nabla^2 \emptyset_{i,j} = -\frac{q}{\varepsilon_s}\left(-n_{i,j} exp\left(\frac{\emptyset_{i,j}-\emptyset_{n_i j}}{V_{T_{i,j}}}\right) + n_{i,j} exp\left(\frac{\emptyset_{i,j}-\emptyset_{p_i j}}{V_{T_{i,j}}}\right) + D_{i,j}\right) \quad (2.55)$$

Finite difference discretization of the above equation has the following form.

$$F_{i,j}^{\emptyset} = \frac{\emptyset_{i+1,j}}{h_1^2} + \frac{\emptyset_{i-1,j}}{h_2^2} + \frac{\emptyset_{i,j+1}}{k_1^2} + \frac{\emptyset_{i,j-1}}{k_2^2} - \emptyset_{i,j}\left(\frac{1}{h_1^2} + \frac{1}{h_2^2} + \frac{1}{k_1^2} + \frac{1}{k_2^2}\right)$$
$$+\frac{q}{\varepsilon_s}\left(-n_{i,j} exp\left(\frac{\emptyset_{i,j}-\emptyset_{n_i j}}{V_{T_{i,j}}}\right) + n_{i,j} exp\left(\frac{\emptyset_{i,j}-\emptyset_{p_i j}}{V_{T_{i,j}}}\right) + D_{i,j}\right) = 0$$

(2.56)

2.10.2.Steady State Electron Current Continuity Equations:

The steady state electron and hole current continuity equations are solved at all mesh-points inside the semiconductor. They are discretized by the Scharfetter-Gummel scheme. The temperature term in the equation is modeled as a local temperature $T_{i,j}$ .If the drift diffusion equations are coupled with the heat flow equation, then we would be able to extract the heat characteristics of the device. But I have not used the heat flow equation in my simulations, so the local temperature is in effect constant, and is equal to the operating temperature of the device.

The Scharfetter-Gummel discretization of the steady state electron current continuity equation is given as

$$F_{i,j}^{n} = \beta\left(\alpha_{i+\frac{1}{2}}\right)\frac{\mu_{n_{i+\frac{1}{2}j}} V_{T_{i+1,j}} n_{i+1,j}}{h_1^2}\beta\left(-\alpha_{i-\frac{1}{2}}\right)\frac{\mu_{n_{i-\frac{1}{2}j}} V_{T_{i-1,j}} n_{i-1,j}}{h_2^2} + \beta\left(\alpha_{j+\frac{1}{2}}\right)\frac{\mu_{n_{i+j+\frac{1}{2}}} V_{T_{i,j+1}} n_{i,j+1}}{k_1^2} +$$
$$\beta\left(-\alpha_{j+\frac{1}{2}}\right)\frac{\mu_{n_{i-j+\frac{1}{2}}} V_{T_{i,j-1}} n_{i,j-1}}{k_2^2} - \left(R_{i,j} - G_{i,j}\right) - n_{i,j} V_{T_{i,j}}\left[\beta\left(-\alpha_{i+\frac{1}{2}}\right)\frac{\mu_{n_{i+\frac{1}{2}j}}}{h_1^2} + \beta\left(\alpha_{i-\frac{1}{2}}\right)\frac{\mu_{n_{i-\frac{1}{2}j}}}{h_2^2} +\right.$$
$$\left.\beta\left(-\alpha_{j+\frac{1}{2}}\right)\frac{\mu_{n_{i,j+\frac{1}{2}}}}{k_1^2} + \beta\left(\alpha_{j-\frac{1}{2}}\right)\frac{\mu_{n_{i,j-\frac{1}{2}}}}{k_2^2}\right] = 0 \quad (2.57)$$

$n_{i,j}$ is the electron concentration at mesh-point (i, j).

$\beta(\gamma)$ is the Bernoulli function defined **as**

$$\beta(\gamma) = \frac{\gamma}{ex(\gamma)-1} \qquad (2.58)$$

And

$$\propto_{i+\frac{1}{2}} = \frac{\emptyset_{i+1,j}-\emptyset_{i,j}}{V_{T_{i,j}}} , \propto_{i-\frac{1}{2}} = \frac{\emptyset_{i,j}-\emptyset_{i-1,j}}{V_{T_{i,j}}} , \propto_{j+\frac{1}{2}} = \frac{\emptyset_{i,j+1}-\emptyset_{i,j}}{V_{T_{i,j}}} , \propto_{j-\frac{1}{2}} = \frac{\emptyset_{i,j}-\emptyset_{i,j-1}}{V_{T_{i,j}}} \qquad (2.59 - 52)$$

The mobility terms in the above equation are written as

$$\boldsymbol{\mu_{n_{i\pm\frac{1}{2}j}} = \frac{\mu_{n_{xi\pm\frac{1}{2}j}}+\mu_{n_{xi\pm,j}}}{2} \ and \ \mu_{n_{i,j\pm\frac{1}{2}}} = \frac{\mu_{n_{yi,j\pm1}}+\mu_{n_{yi,j}}}{2}} \qquad (2.63, 64)$$

Here, $\boldsymbol{\mu_{n_{xi,j}}}$ and $\boldsymbol{\mu_{n_{yi,j}}}$ stand for the x-direction and the y-direction electron mobility respectively, at mesh-point (*i*, *j*)

2.10.3.Steady State Hole Current Continuity Equations:

The hole current continuity equation can be discretized the same way as the electron current continuity equation.

$$F_{I,J}^{p} = \boldsymbol{\beta\left(-\alpha_{i+\frac{1}{2}}\right)\frac{\mu_{p_{i+\frac{1}{2}j}}V_{T_{i+1,j}}p_{i+1,j}}{h_1^2}\beta\left(\alpha_{i-\frac{1}{2}}\right)\frac{\mu_{p_{i-\frac{1}{2}j}}V_{T_{i-1,j}}p_{i-1,j}}{h_2^2}+\beta\left(-\alpha_{j+\frac{1}{2}}\right)\frac{\mu_{p_{i+j+\frac{1}{2}}}V_{T_{i,j+1}}p_{i,j+1}}{k_1^2}+}$$
$$\boldsymbol{\beta\left(\alpha_{j-\frac{1}{2}}\right)\frac{\mu_{p_{i-j+\frac{1}{2}}}V_{T_{i,j-1}}p_{i,j-1}}{k_2^2}-\left(R_{i,j}^{p}-G_{i,j}\right)-p_{i,j}V_{T_{i,j}}\left[\beta\left(\alpha_{i+\frac{1}{2}}\right)\frac{\mu_{p_{i+\frac{1}{2}j}}}{h_1^2}+\beta\left(-\alpha_{i-\frac{1}{2}}\right)\frac{\mu_{p_{i-\frac{1}{2}j}}}{h_2^2}+}$$
$$\boldsymbol{\beta\left(-\alpha_{j+\frac{1}{2}}\right)\frac{\mu_{p_{i,j+\frac{1}{2}}}}{k_1^2}+\beta\left(\alpha_{j-\frac{1}{2}}\right)\frac{\mu_{p_{i,j-\frac{1}{2}}}}{k_2^2}\Big]=0} \qquad (2.65)$$

The mobility terms in the above equation are written as

$$\boldsymbol{\mu_{p_{i\pm\frac{1}{2}j}} = \frac{\mu_{p_{xi\pm1,j}}+\mu_{p_{xi,j}}}{2} \ and \ \mu_{p_{i,j\pm\frac{1}{2}}} = \frac{\mu_{p_{yi,j}}+\mu_{p_{yi,j}}}{2}} \qquad (2.66, 67)$$

Here, $\boldsymbol{\mu_{p_{xi,j}}}$ and $\boldsymbol{\mu_{p_{yi,j}}}$stand for the x-direction and the y-direction hole mobility respectively, at mesh-point (*i*, *j*)

2.11. Numerical Methods

There are two numerical methods that are used to solve the set of discretized equations shown in the section above. The first method is an iterative Gummel Block method which starts with an initial guess for $\emptyset$, $\emptyset_n$ and $\emptyset_p$, at all mesh-points inside the device and solves the three equations consecutively, to get to a solution. This solution acts like the initial guess for the next solver, which is the Newton solver. The Newton solver solves for all three variables $\emptyset$, $\emptyset_n$ and $\emptyset_p$ at all mesh-points simultaneously, using the Gauss-Newton Algorithm.

2.11.1.Gummel Block Method:

The Poisson, electron current continuity, and the hole current continuity equations are solved for the electrostatic potential ($\emptyset$), electron quasi-Fermi level ($\emptyset_n$), and the hole quasi-Fermi level ($\emptyset_p$), respectively, one after the other, using an iterative solver.

First, the discretized Poisson's equation is solved for _ at all points in the mesh using an iterative method. In this case, $\emptyset_n$ and $\emptyset_p$ are kept constant. Next, using the new $\emptyset$ calculated over the mesh, the discretized electron current continuity equation is solved for _ *n* over the mesh. In this case, $\emptyset$ and $\emptyset_p$ are not allowed to change. Finally, using the new $\emptyset$ and $\emptyset_n$ values, the hole current continuity equation is solved at all mesh points and the new $\emptyset_p$ is obtained.

The discretized finite-difference equations are solved using the iterative Gauss-Seidel method. Here, as an example, I show how the solution for $\emptyset$ is obtained iteratively.

The discretized Poisson's equation is arranged in the form shown below

$$\boldsymbol{f_{\emptyset}}\left(\emptyset^{\boldsymbol{k}},\ \emptyset_{\boldsymbol{n}}, \emptyset_{\boldsymbol{p}}\right) = \mathbf{0} \qquad (2.68)$$

where, *k* denotes the current iteration. The solver begins with an initial guess for $\emptyset$ at all mesh points in the device.

According to Newton's method for solving nonlinear equations, we can write

$$\boldsymbol{f_{\emptyset}}\left(\emptyset^{\boldsymbol{k+1}},\ \emptyset_{\boldsymbol{n}}, \emptyset_{\boldsymbol{p}}\right) = \boldsymbol{f_{\emptyset}}\left(\emptyset^{\boldsymbol{k}},\ \emptyset_{\boldsymbol{n}}, \emptyset_{\boldsymbol{p}}\right) + \Delta\emptyset^{\boldsymbol{k}}.\left(\frac{\boldsymbol{\partial f_{\emptyset}}}{\boldsymbol{\partial \emptyset}}\right)^{\boldsymbol{k}} = \mathbf{0} \qquad (2.69)$$

Hence, we have,

$$\Delta\emptyset^{\boldsymbol{k}} = \frac{-(f_{\emptyset})^{\boldsymbol{k}}}{\left(\frac{\partial f_{\emptyset}}{\partial \emptyset}\right)^{\boldsymbol{k}}} \tag{2.70}$$

and

$$\emptyset^{\boldsymbol{k+1}} = \emptyset^{\boldsymbol{k}} + \Delta\emptyset^{\boldsymbol{k}} \tag{2.71}$$

Here, $\emptyset = \emptyset_{i,j}$ = electrostatic potential at the mesh point (*i, j*). The iterations continue till the error $\Delta\emptyset^{\boldsymbol{k}}$ falls below a prescribed error criterion.

Once convergence is reached for the electrostatic potential, a similar method is used to solve for the electron quasi-Fermi level ($\emptyset_{\boldsymbol{n}}$) and then for the hole quasi-Fermi level ($\emptyset_{\boldsymbol{p}}$). Once we have convergence for all three, we switch to the faster Newton's method.

2.11.2.Newton Method:

Unlike the Block Gummel Method, the drift-diffusion equations remain coupled in this method. So $\emptyset$, $\emptyset_{\boldsymbol{n}}$ and $\emptyset_{\boldsymbol{n}}$ are computed simultaneously. This is accomplished by defining a Jacobian matrix and solving for the changes in the three variables between iterations. This process is represented as matrix equation as

$$\begin{bmatrix} \frac{\partial F_{\emptyset}^{k}}{\partial \vec{\emptyset}} & \frac{\partial F_{\emptyset}^{k}}{\partial \overrightarrow{\emptyset_n}} & \frac{\partial F_{\emptyset}^{k}}{\partial \overrightarrow{\emptyset_p}} \\ \frac{\partial F_{\emptyset_n}^{k}}{\partial \vec{\emptyset}} & \frac{\partial F_{\emptyset_n}^{k}}{\partial \overrightarrow{\emptyset_n}} & \frac{\partial F_{\emptyset_n}^{k}}{\partial \overrightarrow{\emptyset_p}} \\ \frac{\partial F_{\emptyset_p}^{k}}{\partial \vec{\emptyset}} & \frac{\partial F_{\emptyset_p}^{k}}{\partial \overrightarrow{\emptyset_n}} & \frac{\partial F_{\emptyset_p}^{k}}{\partial \overrightarrow{\emptyset_p}} \end{bmatrix} \begin{bmatrix} \Delta\overrightarrow{\emptyset^{k}} \\ \Delta\vec{\emptyset}_n^{k} \\ \Delta\vec{\emptyset}_p^{k} \end{bmatrix} = - \begin{bmatrix} F_{\emptyset}^{k} \\ F_{\emptyset_n}^{k} \\ F_{\emptyset_p}^{k} \end{bmatrix} \tag{2.71}$$

where, the vectors $\vec{\emptyset}$, $\overrightarrow{\emptyset_n}$, $\overrightarrow{\emptyset_p}$ signify that the matrix operation is performed for all non-boundary

mesh points of the variables $\emptyset$, $\emptyset_n$ and $\emptyset_p$. Once the above matrix equation is solved, the new values for $\emptyset$, $\emptyset_n$ and $\emptyset_p$ are obtained as

$$\emptyset^{k+1} = \emptyset^{k} + \Delta\emptyset^{k},\ \emptyset_n^{k+1} = \emptyset_n^{k}\ and\ \emptyset_p^{k+1} = \emptyset_p^{k} + \Delta\emptyset_p^{k} \tag{2.73, 74, 75}$$

$F_{\emptyset}, F_{\emptyset_n}$ *and* $F_{\emptyset_p}$ are as shown in equations 2.48, 2.50, 2.56, 2.57, and 2.65. The Jacobian matrix is made up of the derivatives of these functions with respect to $\emptyset$, $\emptyset_n$ and $\emptyset_p$.

The Newton solver is allowed to iterate till it reaches the specified convergence condition for all three variables. Then the current is calculated inside the channel, at the drain contact, at the source contact and at the substrate contact. If the current is continuous across the device, then the simulation is proper and all relevant data is stored in various files. A simple flowchart for the simulator is shown in Figure 2.11.

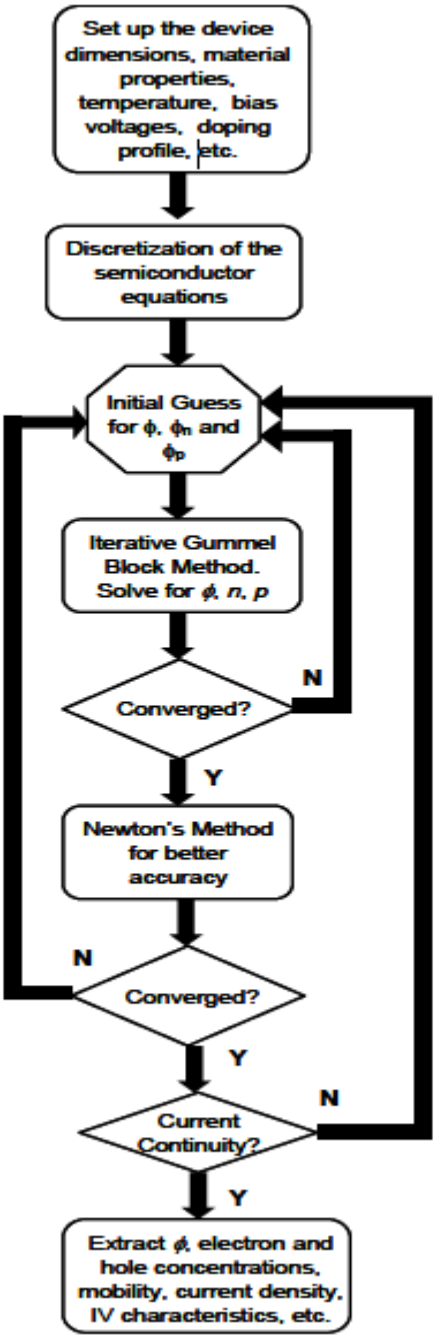


Figure 2.11. Flowchart for solving the drift-diffusion semiconductor equation system

2.12. 2D Mesh

A 2D non-uniform mesh has been created for discretizing the drift-diffusion equations for the MOSFET structure. The mesh is very fine near the drain and the source junctions where there is rapid change in potential and charge concentration. Whereas, near the center of the device,

the mesh is coarse as there is not much variation in these physical quantities there. In order to capture the physics of the inversion layer, the mesh is kept very fine near the interface. The mesh spacing is kept as low as 2Å near the interface. This has enabled me to extract detailed physics of the inversion layer. For example, mobility variations as a function of depth near the interface, or the current density variation as a function of depth in a 4H-SiC MOSFET. The mesh is carefully crafted so that the electrostatic potential does not vary by more than then thermal voltage within adjacent mesh points.

2.13. Based Improvement of the Analytical Model for Vertical DIMOS Transistor in 4H-Silicon Carbide:

In this section we will examine a physically based improvement of the analytical model for a vertical double implanted metal-oxide-semiconductor (DIMOS) transistor in 4H-Silicon Carbide (4H-SiC) is suggested. Special attention has been paid to its vertical section, i.e. to its geometrical profile. The answer to the question where this vertical region starts narrowing and how abruptly it happens has been found exploiting some fundamental principles of physics. This has made possible to considerably reduce the number of free parameters appearing in the construction of current-voltage characteristics.

During the last decade Silicon Carbide (SiC) has appeared as one of the most promising materials for design and fabrication of different devices widely used in microelectronics and Nan electronics [58, 66]. It turned out to be very successful in overcoming the limitations and shortcomings of the Si-based devices. Due to a high melting point (~3100K) and high thermal conductivity (~490 $MV/K.m$) it is very convenient for fabrication of high temperature and high power devices, while a high electric breakdown field (220MV/m) and a high electron saturated velocity (~$2.7x10^5 m/s$) recommend it for use either in switching devices or in widely known other electronic purposes as well [59]. One of such structures is a vertical double implanted metal-oxide-semiconductor transistor (DIMOS) in 4H-Silicon Carbide (it has been chosen because of its almost two times larger mobility in comparison to 6H-SiC). It can carry large currents during the "on" state and, due to its vertical drift section, it is capable of sustaining large "blocking" voltages during the "off' state. In spite of many papers reporting on the investigation of such structures, their level of development can still be regarded as modest and insufficient. The first step necessary to be performed is to properly investigate the relevant physical phenomena and describe them in terms of reliable and simple enough model of current-voltage characteristic for such structures in order to enable its incorporation into more complex nanoelectronic

circuits [58,60,67].

A structure considered is shown in Figure 2.12. In addition to usual MOSFET elements such as gate, source, drain and oxide layer, the substrate itself consists or n+ region embedded in p body, which is then surrounded by 4H-SiC n drill region. Just beneath the oxide layer very narrow channel is formed thus connecting n+ and drift regions [67].

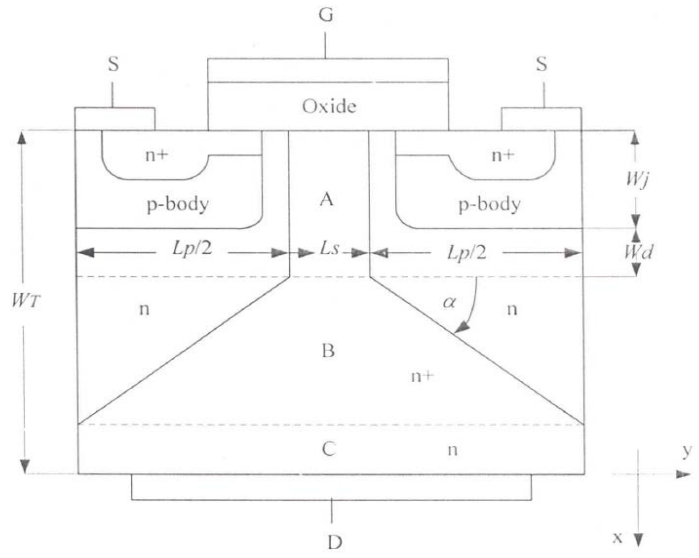


Figure 2.12.A cross section of a vertical DIMOS structure investigated

The corresponding model for current-voltage characteristic is developed from regional analyses and can be exposed as follows [61,67]:

a) Channel in triode region

$$I_D = \frac{W.\mu_n.C_{ox}}{2L\left(1+\frac{\mu_n.V_{ch}}{2v_S.L}\right)}[2(V_{GS}-V_T)V_{ch}-(1+\delta)V_{ch}^2] \qquad (2.76a)$$

$$V_{ch} \le \frac{V_{GS}-V_T}{1+\delta}, \qquad \delta = \frac{C_{do}}{C_{ox}}$$

In saturation

$$I_D = \frac{W.\mu_n.C_{ox}}{2L\left(1+\frac{\mu_n}{2v_S.L}.\frac{V_{GS}-V_T}{1+\delta}\right)}.\frac{(V_{GS}-V_T)^2}{1+\delta} \qquad (2.76b)$$

where W is the channel width, L is the channel length, V_{ch} is the channel voltage, V_T is the threshold

voltage, V_{GS} is the gate voltage, C_{ox} and C_{do} are the oxide capacitance and the body depletion capacitance respectively, μ_n is the electron mobility and v_s the electron saturation velocity.

b) Drift region consists of three parts: an accumulation region A created between two p bodies, a drift region B with a varying cross-section and a drift region C with constant cross-section whose width covers the whole sample. The corresponding voltage drops are given by the following relations [62]:

$$V_A = \int_0^{W_A=W_j+W_d} E_x . d_x = \frac{I_D.(W_j+W_d)}{W.L_d.e.N_D.\mu_n.-\frac{I_D}{E_c}} \quad (2.77a)$$

$$V_B = \frac{I_D}{2.W.e.N_D.\mu_n.ctg\propto} . ln\left(\frac{w.e.N_D.\mu_n.(L_d+L_P)-\frac{I_D}{E_c}}{w.e.N_D.L_d.\mu_n.-\frac{I_D}{E_c}}\right) \quad (2.77b)$$

$$V_c = \frac{I_D.\left(W_T-W_j-W_d-\frac{L_P}{2}.tg\propto\right)}{w.e.N_D.L_d.\mu_n.(L_d+L_P)-\frac{I_D}{E_c}} \quad (2.77c)$$

where W_j is the depth of n+ contact region, W_d is the depth of depletion region, W_T is the total epilayer thickness, L_d is the length of accumulation region and L_P is the p-body length (Figure 2.12.). The voltage drop between drain and source is simply calculated as $V_{DS} = V_{ch} + (V_A + V_B + V_C)$, and the drain current is equal to the total channel current I_{ch}. The voltages and the currents of the above two sets of equations are implicitly related and several solving procedures are developed, but these techniques will not be in the focus of this paper. The careful reader will observe at least two important facts: first, all over the literature devoted to this problem the reader is left without any proof, or even hint, why the accumulation region depth W_A must be equal (or approximately equal) to $(W_j + W_d)$; second, no serious attempt to calculate or estimate the value of the angle a (or tg$\propto$) has ever been made. These two parameters are simply left to be adjusted to the experimental data without any explanation.

2.13.1. Drift region analysis:

As expected, this analysis will start with the Poisson's equation written in the following form:

$$\frac{\partial^2 V}{\partial X^2} + \frac{\partial^2 V}{\partial y^2} = 0 (= e(N_D - n)) \quad (2.78)$$

emphasizing that the substrate is supposed to be electrically neutral all over drift region. In the accumulation region A, the constant current along x-axis (negative direction) implies the existence of

nonzero electric field only; their mutual dependence is given by formula known from the literature [61]:

$$I_D = \frac{e.W.N_D.\mu_n.L_d}{1+\frac{1}{E_C}.\left|\frac{dV}{dx}\right|} = -\frac{e.W.N_D.\mu_n.L_d}{1+\frac{1}{E_C}.\frac{dV}{dx}}.\frac{dV}{dx} \qquad (2.79a)$$

Which immediately gives:

$$\frac{dV}{dx} = -\frac{I_D}{e.W.N_D.\mu_n.L_d-\frac{I_D}{E_c}}; \qquad \frac{dV}{dy} = 0; \quad 0 \le x \le W_A\,; \quad |y| \le \frac{L_d}{2} \qquad (2.79b)$$

The situation with the middle section B of drift region is not so simple. Due to its varying cross-section, the nonzero horizontal electric field also exists. Similar to accumulation region A vertical electric field can be expressed in terms of drift current:

$$\frac{dV}{dx} = -\frac{I_D}{e.W.N_D.\mu_n.(L_d+2(x-W_A)ctg\propto)-\frac{I_D}{E_c}}; \qquad W_A \le x \le W_A+\frac{L_P}{2}.tg\propto; \qquad |y| \le \frac{L_P}{2}+(x-W_A)tg\propto$$

(2.80)

Total derivatives should be substituted by partial ones and therefore we are able to straightforward calculate:

$$\frac{\partial^2 V}{\partial X^2} = \frac{I_D.e.W.N_D.\mu_n.ctg\propto}{(e.W.N_D.\mu_n.(L_d+2(x-W_A).ctg\propto)-\frac{I_D}{E_c})^2} = -\frac{\partial^2 V}{\partial y^2} \qquad (2.81)$$

$$\frac{\partial V}{\partial y} \approx -\frac{2.I_D.e.W.N_D.\mu_n.ctg\propto}{\left[e.W.N_D.\mu_n.(L_d+2(x-W_A).ctg\propto)-\frac{I_D}{E_c}\right]^2}.\mathrm{y} + \mathrm{c(x)} \qquad (2.82a)$$

where, for the sake of symmetry conditions, *c(x)* equals zero along the entire drift region. The expression for horizontal electric field finally becomes:

$$\frac{\partial V}{\partial y} \approx -\approx -\frac{2.I_D.e.W.N_D.\mu_n.ctg\propto}{\left[e.W.N_D.\mu_n.(L_d+2(x-W_A).ctg\propto)-\frac{I_D}{E_c}\right]^2}.\mathrm{y} \qquad (2.82b)$$

Or more conveniently written:

$$\left|\frac{\partial V}{\partial y}\right| = \frac{2.e.W.N_D.\mu_n.ctg\propto}{e.W.N_D.\mu_n.(L_d+2(x-W_A).ctg\propto)-\frac{I_D}{E_c}}.\left|\frac{\partial V}{\partial x}\right|.|y| \qquad (2.82c)$$

The situation in the bottom (C) section of drift region is analogous to that in the accumulation

(A) region; therefore the corresponding expressions arc slightly modified:

$$\frac{dV}{dx} = -\frac{I_D}{e.W.N_D.\mu_n.(L_d+L_P)-\frac{I_D}{E_c}} \; ; \qquad \frac{dV}{dy} = 0 \; ; \qquad W_A + \frac{L_P}{2}.tg \propto \leq x \leq W_A \; ; \qquad |y| \leq \frac{L_d}{2} + \frac{L_P}{2}$$

(2.83)

At this point we shall stop the investigation of Poisson's equation and its consequences. The question that naturally arises is how is it possible to use these results in order to achieve the missing parameters W_A,$tg \propto$. Our idea is to construct the quantity called "action' and then exploit the famous "least action" principle (also called the principle of minimal/maximal action) [69]:

$$S(t_1, t_2) = \int_{t_2}^{t_1} L(q, q^{\cdot}, t).dt \qquad (2.84)$$

Shortly, among all possible trajectories the real one fulfils the condition of minimal (or sometimes maximal) action. Due to stationary character of current flow (Lagrange function L does not depend explicitly on time), one is allowed to conclude that minimal action *S(t I, f2)* corresponds to minimal Lagrangian function *L;* therefore the missing parameters W_A,$tg \propto$ will be determined from the following set of equations [69, 70]:

$$\frac{\partial L}{\partial W_A} = 0 \; ; \quad \frac{\partial L}{\partial tg \propto} = 0 \qquad (2.85)$$

The Lagrangian function L is constructed by means of' its density, i.e. the density of the Lagrangian, according to the following expression:

$$L = \int_V l.dV = W.\iint_{S_{xy}} dx.dy.l \qquad (2.86)$$

where S_{xy} denotes the horizontal cross-section of our structure shown in figure 2.12. Magnetic field being neglected and having on minded that the drift region is considered electrically neutral (with the equal amount *of* ionized donors and mobile electrons), the density of the Lagrangian turns out to depend only on electric field strength [70]:

$$l = \frac{1}{2}.\varepsilon.\left|\underset{E}{\rightarrow}\right|^2 = \frac{1}{2}.\varepsilon.\left(\left(\frac{\partial V}{\partial x}\right)^2 + \left(\frac{\partial V}{\partial y}\right)^2\right) \qquad (2.87)$$

where ε being the dielectric constant of our sample. By use *oC* relation (2.87), the Lagrangian function

(2.86) can be rewritten as follows:

$$L = \frac{1}{2}.\varepsilon.W.\int_0^{W_T} dx \int_{-L(x)}^{L(x)} dy.\left(\left(\frac{\partial V}{\partial x}\right)^2 + \left(\frac{\partial V}{\partial y}\right)^2\right) \tag{2.88}$$

At this point the achievements of the investigation of Poisson's equation should be implemented into relation (2.88). The result can be expressed in the following way:

$$L = L_1 + L_2 + L_3 + L_4 \tag{2.89}$$

Where:

$$L_1 = \frac{1}{2}.\varepsilon.W.\int_0^{W_A} dx \int_{-\frac{L_d}{2}}^{\frac{L_d}{2}} dy.\left(\frac{\partial V}{\partial x}\right)^2 = \frac{1}{2}.\varepsilon.W.\int_0^{W_A} dx \int_{-\frac{L_d}{2}}^{\frac{L_d}{2}} dy.\left(\frac{I_D}{e.W.N_D.\mu_n.L_d - \frac{I_D}{E_c}}\right)^2$$

$$= \frac{1}{2}.\varepsilon.W.W_A.L_d.\left(\frac{I_D}{e.W.N_D.\mu_n.L_d - \frac{I_D}{E_c}}\right)^2 \tag{2.90a}$$

$$L_2 = \frac{1}{2}.\varepsilon.W.\int_{W_A}^{W_A+\frac{L_P}{2}tg\propto} dx \int_{-\frac{L_d}{2}+(x-W_A).tg\propto}^{\frac{L_d}{2}+(x-W_A).tg\propto} dy.\left(\frac{{I_D}^2}{e.W.N_D.\mu_n.\left(L_d+2(x-W_A).tg\propto-\frac{I_D}{E_c}\right)^2} + \frac{(I_D.2.e.W.N_D.\mu_n.ctg\propto)^2}{e.W.N_D.\mu_n.\left(L_d+2(x-W_A).tg\propto-\frac{I_D}{E_c}\right)^4}\right) \tag{2.90b}$$

$$L_3 = \frac{1}{2}.\varepsilon.W.\int_{W_A+\frac{L_d}{2}.tg\propto}^{W_T} dx \int_{-\frac{L_d+L_P}{2}}^{\frac{L_d+L_P}{2}} dy.\frac{{I_D}^2}{\left(e.W.N_D.\mu_n.\left((L_d+L_P)-\frac{I_D}{E_c}\right)\right)^2} =$$

$$\frac{1}{2}.\varepsilon.W.\frac{{I_D}^2.(L_d+L_P)}{\left(e.W.N_D.\mu_n.\left((L_d+L_P)-\frac{I_D}{E_c}\right)\right)^2}.\left(W_T - W_A - \frac{L_P}{2}tg\propto\right) \tag{2.90c}$$

Although the expressions seem clumsy, all the necessary integrations are performed by means of straightforward substitutions. The relations (2.90a) and (2.90c) are obtained almost

by heart, while the calculation of (2.90b)needs some more space and time. Nevertheless, the results can be written in the following form:

$$L_2 =$$

$$\frac{1}{4}.\varepsilon.W.\left(\frac{I_D}{e.W.N_D.\mu_n}\right)^2.\left(tg \propto \right.$$

$$.\left(ln\frac{e.W.N_D.\mu_n.(L_d+L_P)-\frac{I_D}{E_c}}{e.W.N_D.\mu_n.L_d-\frac{I_D}{E_c}}+\left(\frac{I_D}{E_c}\right).\left(\frac{1}{e.W.N_D.\mu_n.L_d-\frac{I_D}{E_c}}-\frac{1}{e.W.N_D.\mu_n.(L_d+L_P)-\frac{I_D}{E_c}}\right)\right)+ctg \propto$$

$$.\left(\frac{1}{3}.ln\frac{.W.N_D.\mu_n.(L_d+L_P)-\frac{I_D}{E_c}}{e.W.N_D.\mu_n.L_d-\frac{I_D}{E_c}}\right)+\left(\frac{I_D}{E_c}\right).\left(\frac{1}{e.W.N_D.\mu_n.L_d-\frac{I_D}{E_c}}-\frac{1}{e.W.N_D.\mu_n.(L_d+L_P)-\frac{I_D}{E_c}}\right)+$$

$$\frac{1}{2}.\left(\frac{I_D}{E_c}\right)^2.\left(\frac{1}{\left(e.W.N_D.\mu_n.L_d-\frac{I_D}{E_c}\right)^2}-\frac{1}{\left(e.W.N_D.\mu_n.(L_d+L_P)-\frac{I_D}{E_c}\right)^2}\right)+$$

$$\left.\frac{1}{3}.\left(\frac{I_D}{E_c}\right)^3.\left(\frac{1}{\left(e.W.N_D.\mu_n.L_d-\frac{I_D}{E_c}\right)^3}-\frac{1}{\left(e.W.N_D.\mu_n.(L_d+L_P)-\frac{I_D}{E_c}\right)^3}\right)\right) \qquad (2.90d)$$

In order to write the entire Lagrangian function, in a more concise form, it is useful to introduce following abbreviations:

$$\lambda_d = e.W.N_D.\mu_n.L_d-\frac{I_D}{E_c};\quad \lambda_{dp} = e.W.N_D.\mu_n.(L_d+L_P)-\frac{I_D}{E_c} \qquad (2.91)$$

The Lagrangian function then becomes:

$$L = L_1+L_2+L_3+L_4 = \frac{1}{2}\varepsilon.W.W_A.\frac{L_d.{I_D}^2}{{\lambda_d}^2}+\frac{1}{4}.\varepsilon.W.\left(\frac{I_D}{e.W.N_D.\mu_n}\right)^2.\left(tg \propto.\left(\ln\frac{\lambda_{dp}}{\lambda_d}+\left(\frac{I_D}{E_c}\right).\left(\frac{1}{\lambda_d}-\right.\right.\right.$$

$$\left.\left.\left.\frac{1}{\lambda_{dp}}\right)\right)+ctg \propto.\left(\frac{1}{3}\ln\frac{\lambda_{dp}}{\lambda_d}+\left(\frac{I_D}{E_c}\right).\left(\frac{1}{\lambda_d}-\frac{1}{\lambda_{dp}}\right)+\frac{1}{2}\left(\frac{I_D}{E_c}\right)^2.\left(\frac{1}{\lambda_d}-\frac{1}{\lambda_{dp}}\right)^2+\frac{1}{3}\left(\frac{I_D}{E_c}\right)^3.\left(\frac{1}{\lambda_d}-\frac{1}{\lambda_{dp}}\right)^3\right)\right)+$$

$$\frac{1}{2}.\varepsilon.W.\left(W_T-W_A-\frac{L_P}{2}.tg\alpha\right)\frac{(L_d+L_P).{I_D}^2}{{\lambda_{dp}}^2} \qquad (2.92)$$

This form of Lagrangian function is convenient enough to be used in the sense or relation (2.85):

$$\frac{\partial L}{\partial W_A} = \frac{1}{2}\varepsilon.W.\frac{(L_d+L_P).{I_D}^2}{{\lambda_{dp}}^2} \qquad (2.93)$$

Due to the "quasi/saturation effect", λ_d never approaches zero (it asymptotically tends to it), and therefore the expression (2.93) is easily verified to be always positive. It means that $L(W_A)$ rises whenever W_A gets larger over the whole available range and has no local minimum/maximum. This can be understood as a conclusion that $L(W_A)$ becomes minimal if W_A approaches as small as possible value imposed by some additional (geometric) constraint. The narrowing of our currant flow profile demands some additional energy to be spent. Therefore this narrowing happens not earlier than it is caused by some external constraints (i.e. the existence of n^+ regions and p-bodies accompanied by corresponding depletion layers). Based upon these arguments, the depth of accumulation region A is finally chosen to be:

$$W_A \approx W_j + W_d \tag{2.94}$$

The dependence of Lagrangian function L on the angle $\propto$ is also very simple and its first derivative with respect to $tg \propto$ becomes:

$$\frac{\partial L}{\partial tg\propto} = \frac{1}{4}\varepsilon.W.\left(\frac{I_D}{e.W.N_D.\mu_n}\right)^2.\left(\ln\frac{\lambda_{dp}}{\lambda_d} + \left(\frac{I_D}{E_c}\right).\left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}}\right)\right) - \frac{1}{tg^2\propto}.\left(\frac{1}{3}\ln\frac{\lambda_{dp}}{\lambda_d} + \left(\frac{I_D}{E_c}\right).\left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}}\right) + \frac{1}{2}\left(\frac{I_D}{E_c}\right)^2.\left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}}\right)^2 + \frac{1}{3}\left(\frac{I_D}{E_c}\right)^3.\left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}}\right)^3\right) - \frac{1}{4}.\varepsilon.W.\frac{(L_d+L_P).L_P.{I_D}^2}{{\lambda_{dp}}^2} \tag{2.95a}$$

The relation (2.85) demands this derivative to become zero, hence making it straightforward to determine $tg\alpha$:

$$tg\alpha = \sqrt{\frac{\frac{1}{3}\ln\frac{\lambda_{dp}}{\lambda_d} + \left(\frac{I_D}{E_c}\right).\left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}}\right) + \frac{1}{2}\left(\frac{I_D}{E_c}\right)^2.\left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}}\right)^2 + \frac{1}{3}\left(\frac{I_D}{E_c}\right)^3.\left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}}\right)^3}{\ln\frac{\lambda_{dp}}{\lambda_d} + \left(\frac{I_D}{E_c}\right).\left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}}\right) - \frac{(e.W.N_D.\mu_n)^2.(L_d+L_P).L_P}{{\lambda_{dp}}^2}}} \tag{2.95b}$$

It can also be easily verified that the denominator and the numerator of the expression under square root in the relation (2.95b) are both positive, thus providing the absence of any problems considering the existence of reasonable value for $tg\alpha$.

In this way, we have succeeded to determine two missing parameters W_A $tg\alpha$, in terms of drain current as a varying parameter and a set of fixed technological parameters describing our sample. The only constraint with respect to I_D that survives is the same one as at the beginning of our analysis (also indispensable for the validity of relation (2.95b) (and valid even in quasi-saturation):

$$\lambda_d = e.W.N_D.\mu_n.L_d - \frac{I_D}{E_c} > 0 \qquad (2.96)$$

2.13.2. Construction of the model for current-voltage characteristic:

Having solved the problems concerning the transport profile in the vertical (drift) region of our sample, one has become capable of constructing the analytical model for currant-voltage characteristic. The first step is to just keep in sight relations (2.76a) and (2.76b) describing two symmetrically placed horizontal channels. It is also worth noticing that the question whether the entire device operates in saturation mode or in triode regime will not be uniquely answered to by the fact that the channel transport itself is saturated or not, while quasi-saturation also plays an important role. Anyhow, relation (2.76) can be rearranged in order to provide the explicit dependence of channel voltage upon drain current [61, 67]:

$$V_{ch} = \frac{V_{GS}-V_T-\frac{I_D}{2W.C_{OX}.v_S}}{1+\delta} - \sqrt{\left(\frac{V_{GS}-V_T-\frac{I_D}{2W.C_{OX}.v_S}}{1+\delta}\right)^2 - I_D.\frac{2L}{W.C_{ox}.\mu_n}} \qquad (2.97)$$

Now, for each specific value of drain current, the channel voltage can be easily calculated. Another step is to determine voltage drop over drift region by means of relation (2.77).If the abbreviations (2.91) are used, the relation (2.77) can be rewritten in a more concise form:

$$V_A = \frac{(W_j+W_d).I_D}{\lambda_d} \qquad (2.97a)$$

$$V_B = \frac{I_D}{2.e.W..N_D.\mu_n ctg\alpha}.\ln\frac{\lambda_{dp}}{\lambda_d} \qquad (2.98b)$$

$$V_c = \frac{\left(W_T-(W_j+W_d)-\frac{L_P}{2}tg\propto\right)}{\lambda_{dp}} \qquad (2.98c)$$

Finally, by means of relations (2.97) and (2.98), the drain-source voltage can be simply written as:

$$V_{DS} = V_{ch} + (V_A + V_B + V_c) \qquad (2.99)$$

naturally in saturation as well as in triode region of characteristic. In this case, current-voltage characteristic is obtained in an inverse form as $V_{DS}(I_D)$. Therefore it would better be named as voltage-current characteristic.

2.13.3. Numerical results and discussion:

The model itself has been tested for a specific set of geometric and technological parameters describing the investigated structure [63]:

$W = 400\mu m$ $\quad W_j = 30\mu m$ $\quad N_D = 4 * 10^{21} m^{-3}$

$L = 1\mu m$ $\quad W_d = 2\mu m$ $\quad N_A = 4 * 10^{23} m^{-3}$

$v_s = 0.08 m^2/Vs$ $\quad L_d = 20\mu m$ $\quad E_c = 3MV/m$

$\mu_n = 0.08 m^2/Vs$ $\quad L_p = 50\mu m$ $\quad \varepsilon_r = 3.9$

$\sigma = 0$ $\quad W_T = 70\mu m$ $\quad W_j = ?$

$V_{GS} - V_T = 1V$ $\quad t_{ox} = 50nm$ $\quad tg \propto = ?$

Among these parameters, special attention has to be paid to carriers' mobility. The value nominated above is valid in bulk, while its value in drift region as well as in the channel can be considerably smaller. Drain current is supposed not to exceed the value imposed by quasi-saturation effect $(\lambda_d > 0)$, while theoretical limits for a $(tg \propto)$ are given by following relations:

$$0 \leq tg \propto \leq \frac{W_T - W_A}{\frac{L_p}{2}} = 1.52 \quad \text{or} \quad 0 \leq \propto \leq 57^{\circ} \qquad (2.100)$$

The dependences $tg \propto = f(I_D)$ and $\propto = \varphi(I_D)$ calculated according to the relation (95b) are shown in figures (2.13a) and (2.13b) respectively, with a carriers' mobility μ_n considered as a varying parameter, being degraded even to the third of its bulk value. The causes of this degradation might be different, only the influence of doping level N_D and the anisotropy of the sample to be mentioned. The

4H-SiC is known to be very anisotropic; it means that mobility, critical field strength and ionization coefficients are different in c-directions compared to a and b ones. This fact will surely make int1uence on the calculated values of the investigated quantities, but is not expected to put any doubt on the procedure itself[59, 66]. On the other hand, μ_n always appears together with W in our calculations (because of multiplication the possible decrease of W will cause the same effect as mobility degradation). The result worth mentioning is that the angle $\propto$ remains in the range $(40^\circ - 50^\circ)$ for almost all reasonable values of drain current and carriers' mobility. Figures 2a and 2b suggest a slight increase of the calculated angle $\propto$ with the increase of drain current for each specific value of carriers' mobility μ_n. Figures 2.14a and 2.14b show the dependence of the angle $\propto$ and $tg \propto$ on carriers' mobility μ_n varying in the reasonable range for different values of drain current considered as a parameter. As expected, the decrease of carriers' mobility is accompanied by a slight increase of the angle $\propto$. Dramatic increase of the calculated angle will not happen until the balance of chosen values for the parameters of our structure is considerably broken causing λ_d falls close to zero (but still remaining positive), thus drain current *approaching its upper limit (quasi-* saturation effect). In figure 2.15, the dependence of voltage drop along drift region on drain current $V_{drift} = f(I_D)$ has been plotted for various values of μ_n. Comparing it to the calculated values of the channel voltage, it becomes obvious that the prevailing part (90% at least) of drain-source voltage drop belongs to (vertical) drift region, thus making it an excellent candidate for the construction of huge capacity "blocking voltage" reservoir.

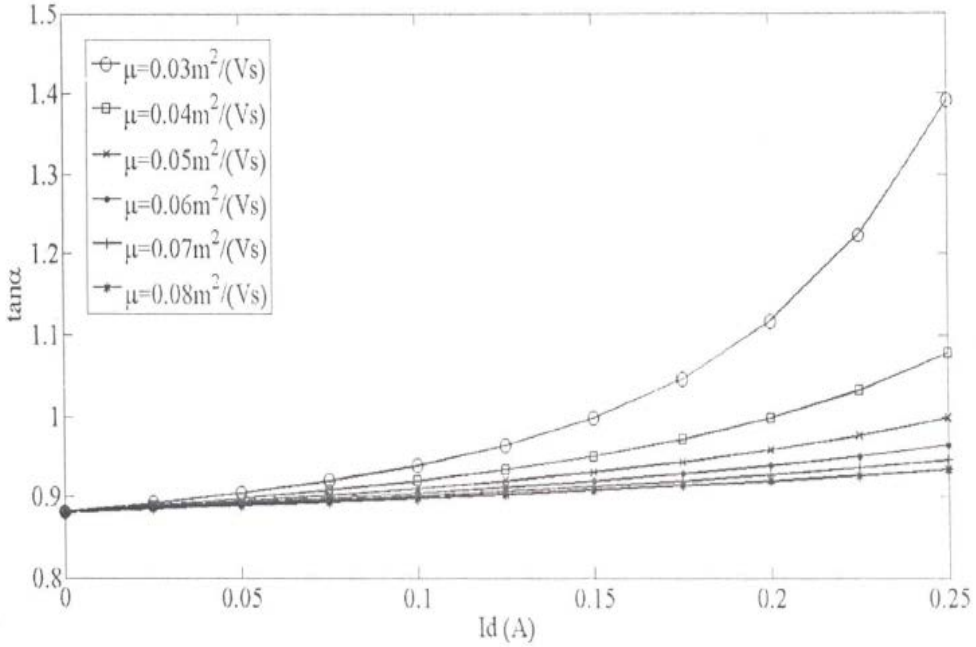


Figure 2.13a. $tg \propto$ versus I_D, for different values of parameter μ_n

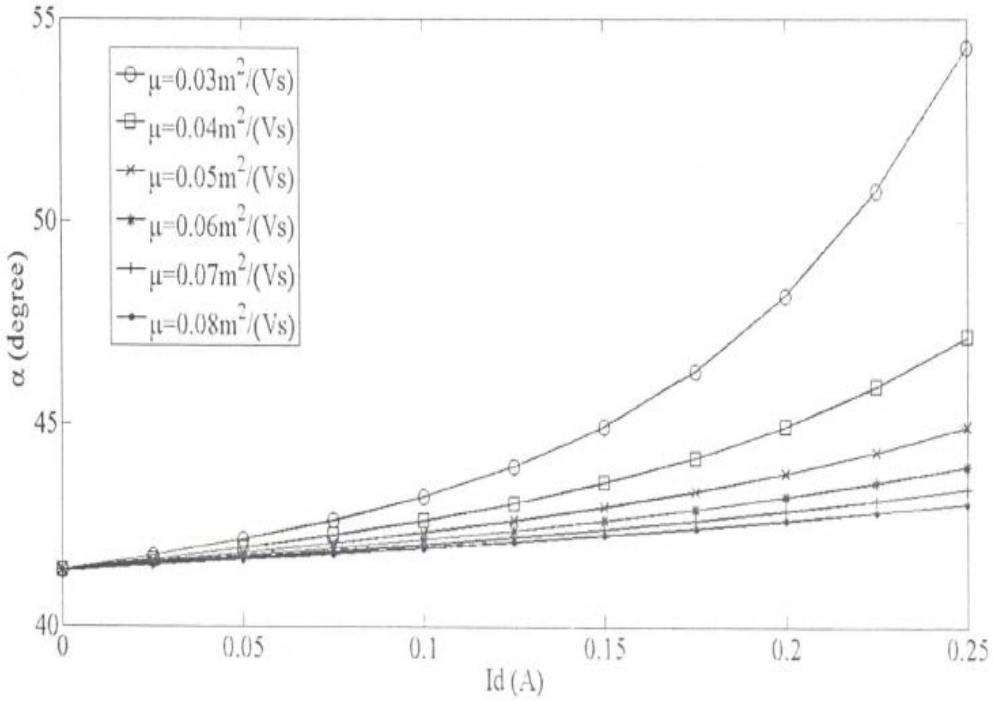


Figure 2.13b. Angle $\propto$ versus I_D, for different values of parameter μ_n

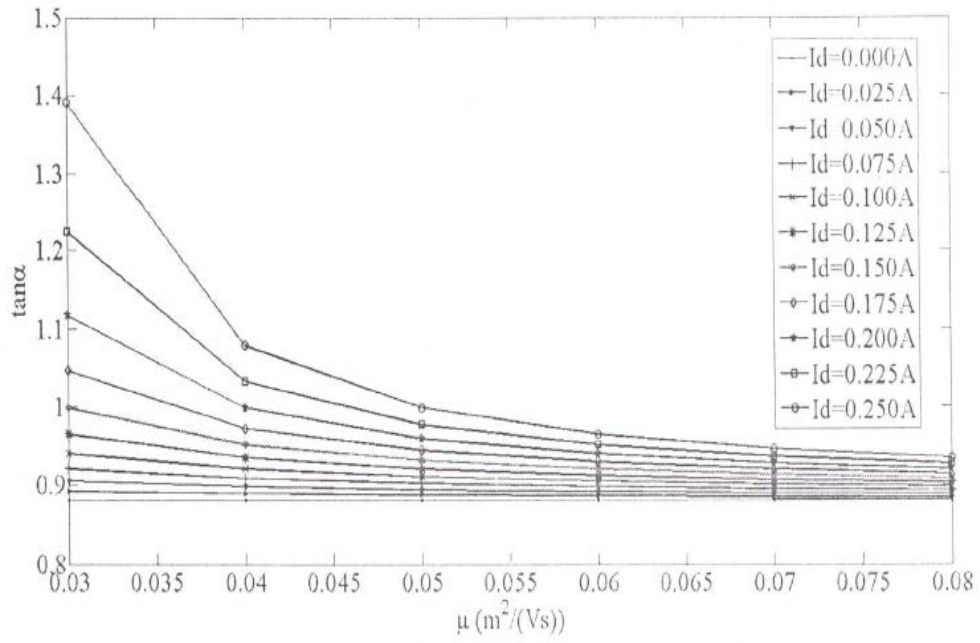


Figure 2.14a. $tg \propto$ versus μ_n, for different values of parameter I_D

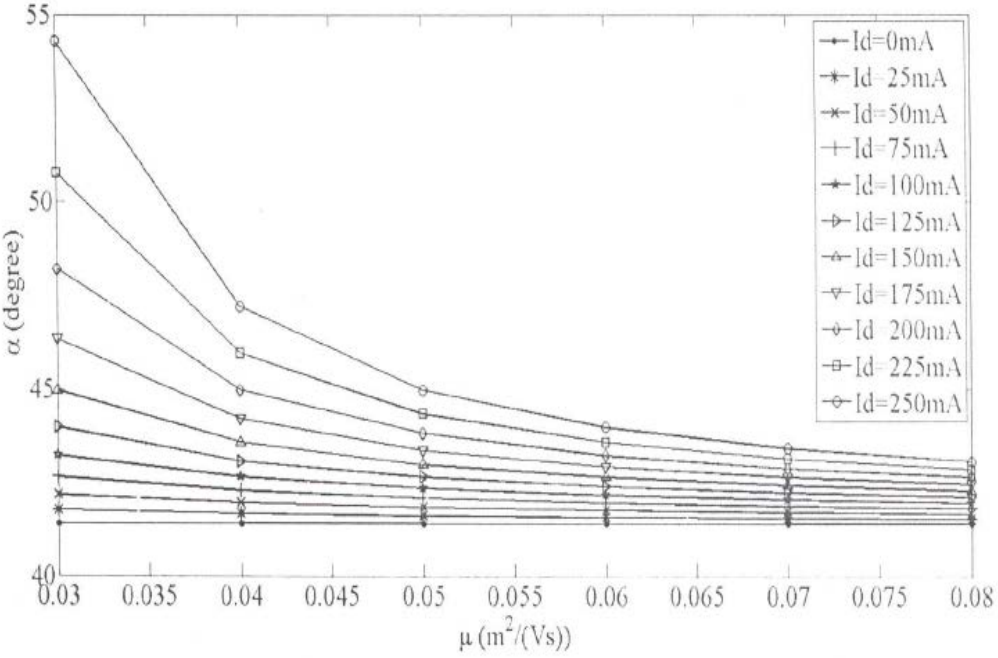


Figure 2.14b. Angle $\propto$ versus μ_n, for different values of parameter I_D

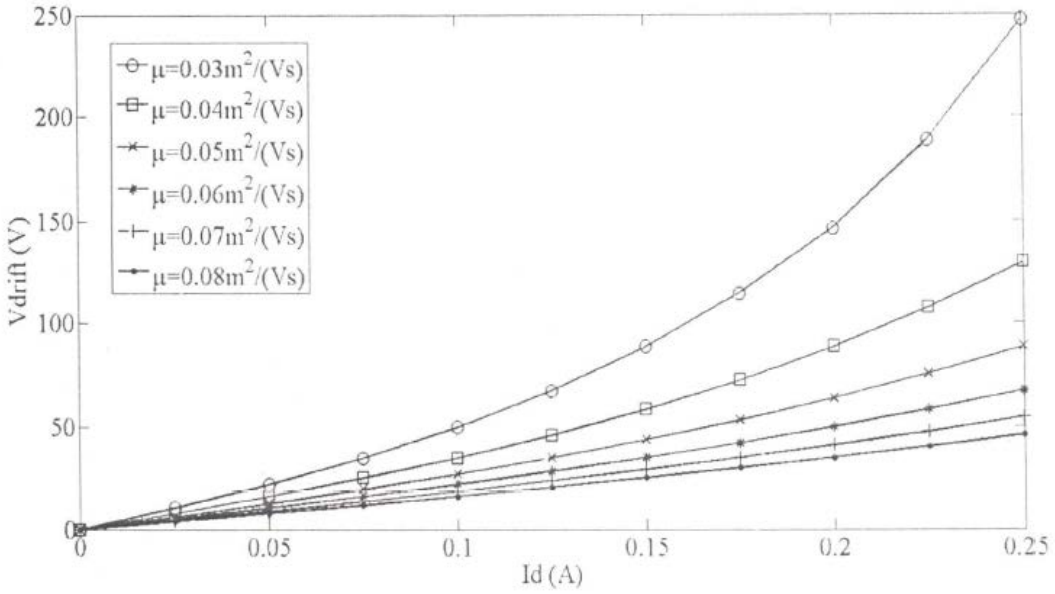


Figure 2.15. Drift region voltage drop V_{drift} versus I_D, for different values of parameter μ_n

2.13.4. S**ummary:**

Exploiting the fundamental principle of physics, the existing analytical model for DlMOS has successfully been improved and the procedure for calculation some missing parameters have been proposed. These parameters turn out to be indispensable for the evaluation of voltage drop over drift region, thus making a great influence on current-voltage characteristic. The values of drift current are mainly governed by the phenomena taking place along the channel.

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Part Three:

3.1- Dual-Material Surrounding-Gate MOSFETs Review:

MOSFETs transistors technology experienced a very fast evolution in order to produce integrated circuits with better performances. This was obtained, up to recent years, by scaling the dimensions of the transistors as well as the voltage applied. Recently the channel length has approached 100nm and bulk MOSFETs have reached their physical shrinkage limits. The innovation has been the development of silicon on insulator (SOI) technology. One of the more promising structures is the vertical Dual-Material Surrounding-Gate (DMSG) MOSFETs [1-2] as shown in Fig. 3.1.(a) in which drain, gate and source, gate oxide are arranged vertically, using sidewalls of silicon pillars as the channel, Fig.3.1.(b) shows the cross section view of Dual-Material Surrounding-Gate (DMSG) MOSFETs. DMSG has the following advantages : (1) high packing density, (2) high-speed cut-off frequency, (3) reduced short channel effects (SCEs), (4) reduced fringe-induced barrier lowering (FIBL), (5) low-power consumption. [3-5] To overcome these limitations and realize high-performance MOS transistors, 3D surrounding-gat (SG) is introduced and successfully applied to the memory circuits, [6-9]. To gain physical insight into the device physics for Dual-Material Surrounding-Gate (DMSG) MOSFETs, there is a need to develop an analytical model for the sub threshold behavior.

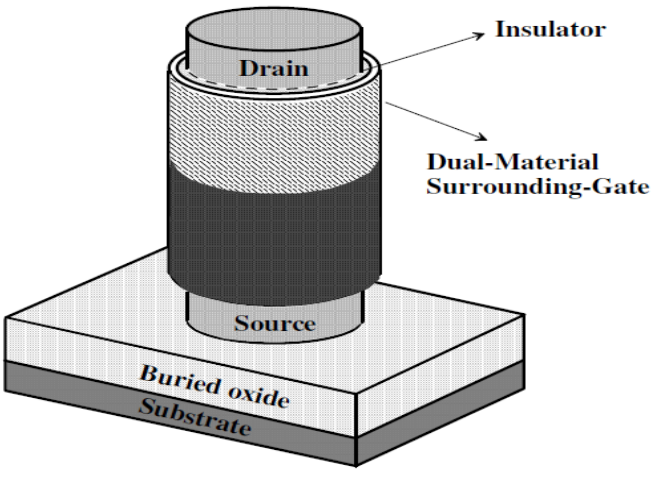


Fig.3.1.(a) vertical Dual-Material Surrounding-Gate (DMSG) MOSFETs

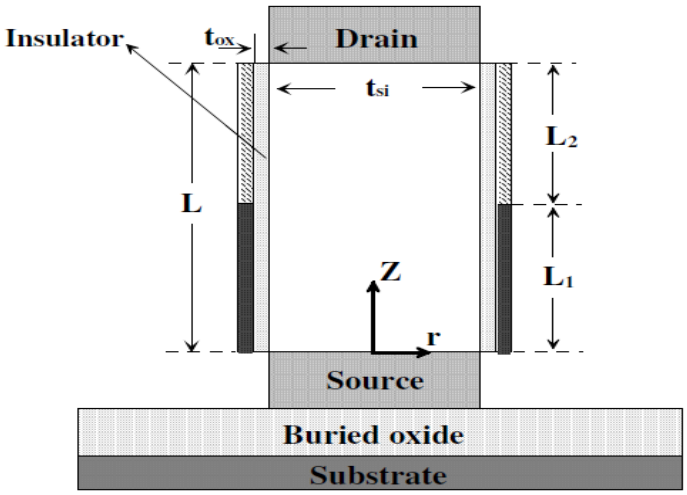


Fig.3.1.(b) cross section view of Dual-Material Surrounding-Gate (DMSG) MOSFETs

3.2- Two Dimensional Model For vertical Dual-Material Surrounding-Gate (DMSG) MOSFETs:

3.2.1.Introduction:

To precisely analyze the vertical Dual-Material Surrounding-Gate (DMSG) MOSFETs, the exact two dimensional expression comprising channel potential and threshold voltage, are needed, especially for the device applied to the integrated circuits. Based on the exact resultant solution of two dimensional Poisson equation, the device physics based models for channel potential, threshold voltage, sub threshold current and sub threshold swing for vertical Dual-Material Surrounding-Gate (DMSG) MOSFETs are developed. In previous papers [10-14], analytical solutions of those models for vertical Dual-Material Surrounding-Gate (DMSG) MOSFETs only included Si-body but exception of insulator region. The simulated results of the analytical model match well with those simulated by device simulator [15]. Besides giving deep insight into the device physics, the analytical results are useful in predictive compact subthreshold modeling of vertical Dual-Material Surrounding-Gate (DMSG) MOSFETs.

3.2.2. Two-Dimensional Potential Solution:

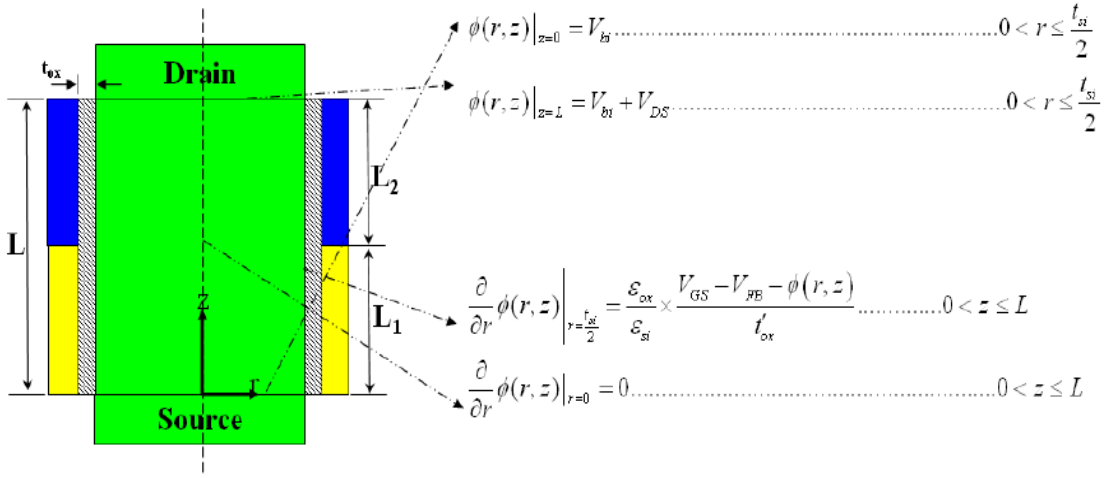
We assume the source and drain junctions are abrupt, boundary conditions are[16-22]

$$\emptyset(r,z)|_{z=0} = V_{bi} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots 0 \le r \le \frac{t_{si}}{2} \quad (3.1)$$

$$\emptyset(r,z)|_{z=L} = V_{bi} + V_{DS} \dots\dots\dots\dots\dots\dots\dots\dots 0 \le r \le \frac{t_{si}}{2} \quad (3.2)$$

$$\frac{\partial}{\partial r}\emptyset(r,z)\Big|_{r=\frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \times \frac{V_{GS}-V_{EB}-\emptyset(r,z)}{t'_{ox}} \dots\dots\dots 0 < Z \le L \quad (3.3)$$

$$\frac{\partial}{\partial r}\emptyset(r,z)\Big|_{r=0} = 0 \dots\dots\dots\dots\dots\dots\dots\dots\dots 0 < Z \le L \quad (3.4)$$



Where V_{bi} is the built-in potential at the interface between source / drain and channel, V_{DS} is the drain bias, V_{GS} is the gate bias, ε_{si} is permittivity of silicon ($\varepsilon_{si} = 11.7 \times 8.85 \times 10^{-14}$ F/m), ε_{ox} is permittivity of gate insulator ($\varepsilon_{ox} = 3.9 \times 8.85 \times 10^{-14}$), $t'_{ox} = \frac{t_{si}}{2} \times \ln\left(1 + \frac{2t_{ox}}{t_{xi}}\right)$ is effective insulator thickness for calculating the capacitance of the vertical, Dual-Material Surrounding-Gate (DMSG) MOSFETs[23].

By assuming that the source and drain junction are abrupt, the Poisson's equation is solved separately under the two gate regions using the following boundary conditions.

(a) Surface ptential at the interface of the two dissimilar metals is continuous:

$$\emptyset_1(r,L_1) = \emptyset_2(r,L_2) \quad (3.5)$$

(b) Electric field at the interface of the two dissimilar metals is continuous:

$$\frac{\partial\emptyset_1(r,Z)}{\partial r}\Big|_{Z=L_1} = \frac{\partial\emptyset_2(r,Z)}{\partial z}\Big|_{z=L_1} \quad (3.6)$$

(c) Electric flux at the interface of gate / oxide is continuous for both of the metal gates:

$$\frac{\partial\emptyset_1(r,Z)}{\partial r}\Big|_{r=\frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \times \frac{V_{GS}-V_{FB_1}-\emptyset_1(r,z)}{t'_{ox}} \dots\dots\dots\dots (for\ M_1) \quad (3.7)$$

$$\left.\frac{\partial \emptyset_2(r,Z)}{\partial r}\right|_{r=\frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \times \frac{V_{GS}-V_{FB_2}-\emptyset_2(r,z)}{t'_{ox}} \text{ .....(for } M_2) \quad (3.8)$$

(d) The potential at the surface end is

$$\emptyset_1(r, z = 0) = V_{bi} \quad (3.9)$$

(e) The potential at the drain end is

$$\emptyset_2(r, L_1 + L_2) = V_{bi} + V_{DS} \quad (3.10)$$

The $V_1(r)$, $U_1(r,z)$ and $V_2(r)$, $U_2(r,z)$ can be from the boundary conditions mentioned-above.

From equations of (3.24), (3.5), (3.6) ,(3.7), and (3.9), the solution $V_1(r)$ can be obtained as

$$V_1(r) = \frac{qN_A}{4\varepsilon_{si}}\mathrm{r}^2 + V_{GS} - V_{FB_1} - \frac{qN_A t_{si}^2}{16\varepsilon_{si}} - \frac{qN_A t_{si}}{4c'_{ox}} \quad (3.11)$$

Similarly, solving the equations of (3.4), (3.5), (3.6) ,(3.8), and (3.10), we get

$$V_2(r) = \frac{qN_A}{4\varepsilon_{si}}\mathrm{r}^2 + V_{GS} - V_{FB_2} - \frac{qN_A t_{si}^2}{16\varepsilon_{si}} - \frac{qN_A t_{si}}{4c'_{ox}} \quad (3.12)$$

By using the separation method together with boundary conditions of (a)-(e), one obtaics the following resultant solution of two-dimensional Laplace equation:

$$U_1(r,z) = \sum_{n=1}^{\infty} J_0(\lambda_n r) \times \left\{A_n e^{\lambda_n z} + B_n e^{-\lambda_n z}\right\} \quad (3.13)$$

And

$$U_2(r,z) = \sum_{n=1}^{\infty} J_0(\lambda_n r) \times \left\{C_n e^{\lambda_n z} + D_n e^{-\lambda_n z}\right\} \quad (3.14)$$

Where the Bessel-Fourier series coefficients of A_n , B_n , C_n , and D_n, are expressed as

$$A_n = \frac{1}{2}[1 - \coth((L_1 + L_2)\lambda_n)]\left\{P_n - e^{(L_1+L_2)\lambda_n}[Q_n + R_n\cosh(L_2\lambda_n)]\right\} \quad (3.15)$$

$$B_n = \frac{1}{2}\left[\coth\left((L_1 + L_2)\lambda_n\right) - 1\right]\left\{P_n e^{2(L_1+L_2)\lambda_n} - e^{(L_1+L_2)\lambda_n}[Q_n + R_n\cosh(L_2\lambda_n)]\right\} \quad (3.16)$$

$$C_n = \frac{1}{4}\left[\coth\left((L_1 + L_2)\lambda_n - 1\right)\right]\left[e^{-L_1\lambda_n}R_n - 2P_n + e^{L_1\lambda_n}(2e^{L_2\lambda_n}Q_n + R_n\right] \quad (3.17)$$

$$D_n = \frac{1}{4}\left[\coth\left((L_1 + L_2)\lambda_n - 1\right)\right]\left\{2e^{2(L_1+L_2)\lambda_n}P_n - e^{(L_1+L_2)\lambda_n}\left[2Q_n + e^{L_2\lambda_n}R_n(1 + e^{2L_1\lambda_n})\right]\right\} \quad (3.18)$$

Where

$$P_n = \frac{qN_A t_{si} c'_{ox} J_2\left(\frac{\lambda_n t_{si}}{2}\right) + J_1\left(\frac{\lambda_n t_{si}}{2}\right)\lambda_n \varepsilon_{si}\left[qN_a t_{si} + 4c'_{ox}(V_{bi} + V_{FB1} - V_{GS})\right]}{t_{si}\left[J_0^2\left(\frac{\lambda_n t_{si}}{2}\right) + J_1^2\left(\frac{\lambda_n t_{si}}{2}\right)\right]\varepsilon_{si}\lambda_n^2 c'_{ox}} \quad (3.19)$$

$$Q_n = \frac{qN_A t_{si} c'_{ox} J_2\left(\frac{\lambda_n t_{si}}{2}\right) + J_1\left(\frac{\lambda_n t_{si}}{2}\right)\lambda_n \varepsilon_{si}\left[qN_A t_{si} + 4c'_{ox}(V_{bi} + V_{FB1} + V_{DS} - V_{GS})\right]}{t_{si}\left[J_1^2\left(\frac{\lambda_n t_{si}}{2}\right) + J_1^2\left(\frac{\lambda_n t_{si}}{2}\right)\right]\varepsilon_{si}\lambda_n^2 c'_{ox}} \quad (3.20)$$

$$R_n = \frac{4J_1\left(\frac{\lambda_n t_{si}}{2}\right)(V_{FB1}-V_{FB2})}{t_{si}\left[J_1^2\left(\frac{\lambda_n t_{si}}{2}\right)+J_1^2\left(\frac{\lambda_n t_{si}}{2}\right)\right]\lambda_n} \quad (3.21)$$

In fig. 3.2, Fig. 3.4 and fig. 3.5, it can be found that the Bessel function series coefficients decay rapidly, and the first term will dominate the Bessel function series, hence, the potential can be expressed by the first term,as shown in the next setion.

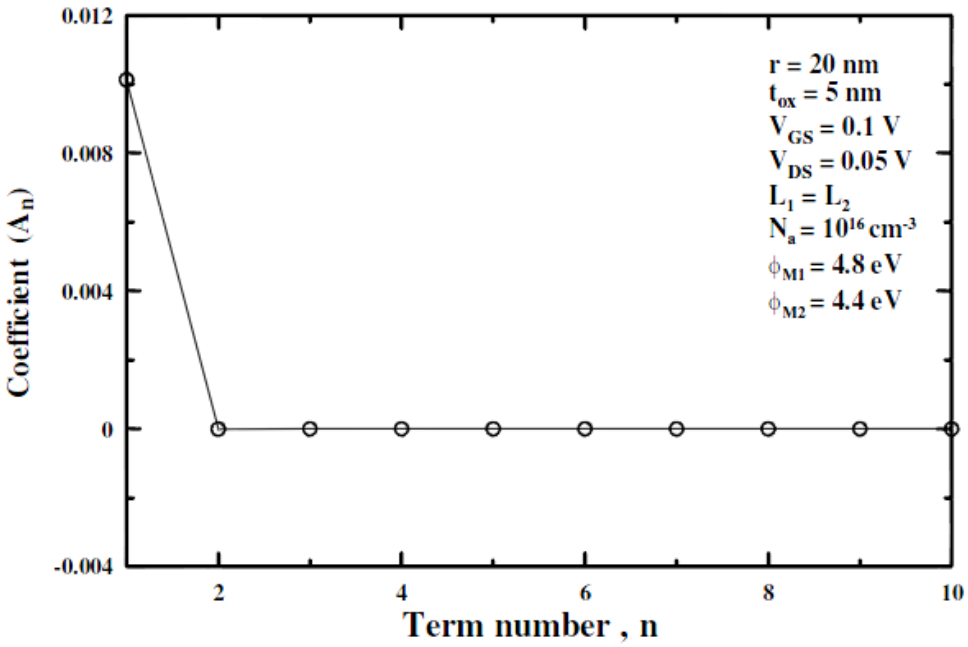


Fig.3.2.The decay of Fourir series A_n coefficients versus the term number.

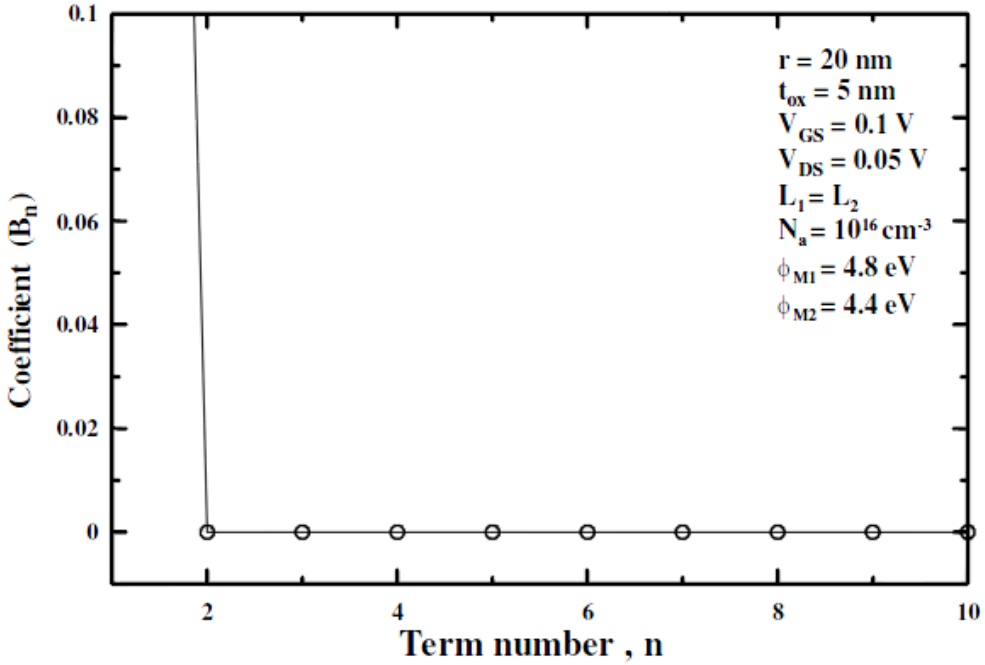


Fig.3.3.The decay of Fourir series B_n coefficients versus the term number.

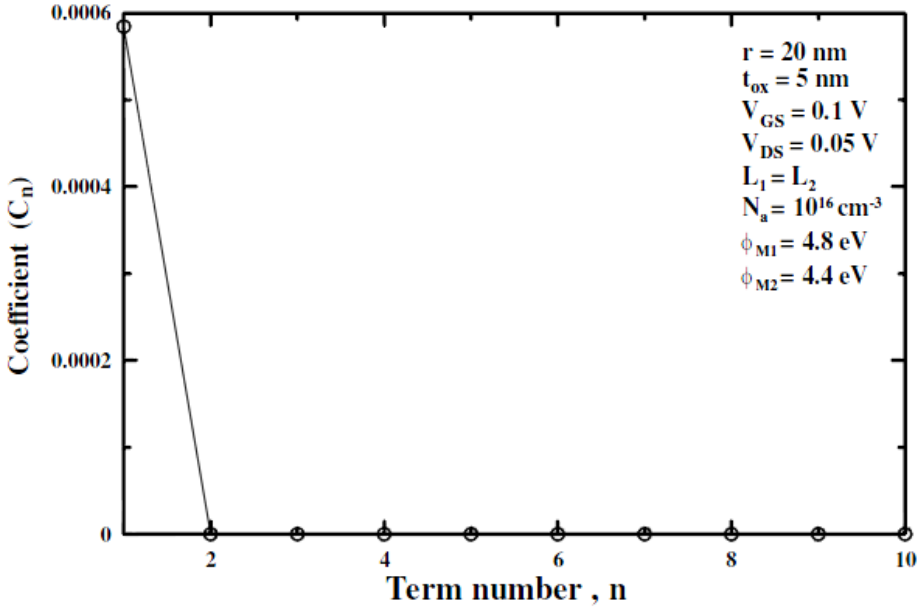


Fig.3.4.The decay of Fourir series C_n coefficients versus the term number.

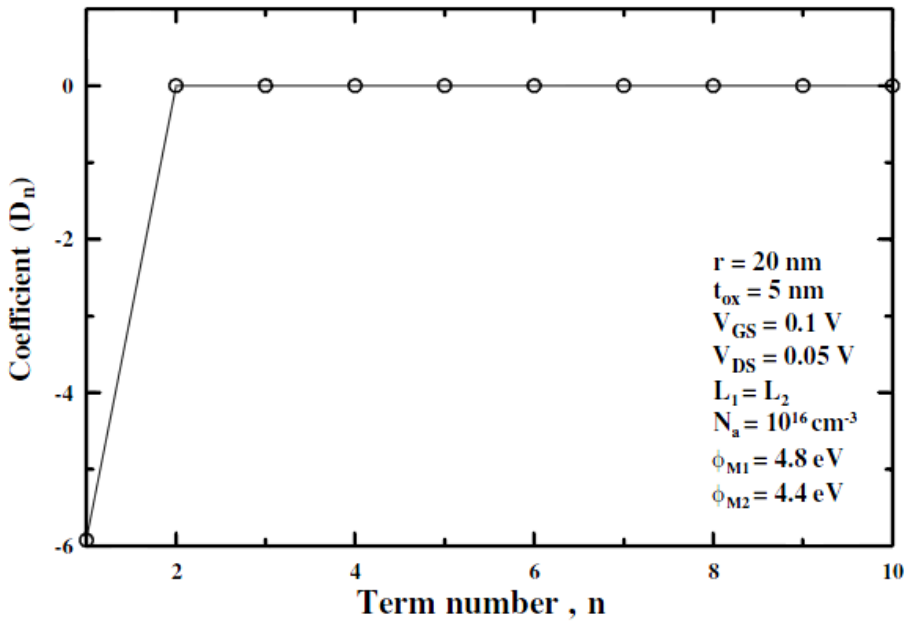


Fig.3.5.The decay of Fourir series D_n coefficients versus the term number.

The λ_n is the electrostatic scale length for 2D effect in the silicon film for the Dual-Material Surrounding-Gate (DMSG) MOSFETs with ultra-thin gate insulator [24-32]

$$\lambda_n = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \times \frac{J_0\left(\lambda_n \frac{t_{si}}{2}\right)}{t'_{ox} J_1\left(\lambda_n \frac{t_{si}}{2}\right)} \qquad (3.22)$$

Where t'_{ox} is effective insulator thick ness for calculating the capacitance of the vertical, cylindrical Dual-Material Surrounding-Gate (DMSG) MOSFETs. $\left(t'_{ox} = \frac{t_{si}}{2} \times \ln\left(1 + \frac{2t_{ox}}{t_{si}}\right)\right)$.

The slope of the contours increases dramatically for shorter scale lengths, indicating a significant departure from the simple theory. This increased slope may be beneficial to highly scaled FETs, since it implies that the penalty for using insufficiently scaled oxide thickness is less then might have been expected, although it also coincides with degraded subthreshold swing. Consequently, it is obviously seen that both thin insulator and thin Si film will

be required for the small scale length which the 2D effects causing DIBL and threshold voltage degradation. Therefore it is protruded that our scaling length model can be applied to larger range of insulator thickness.

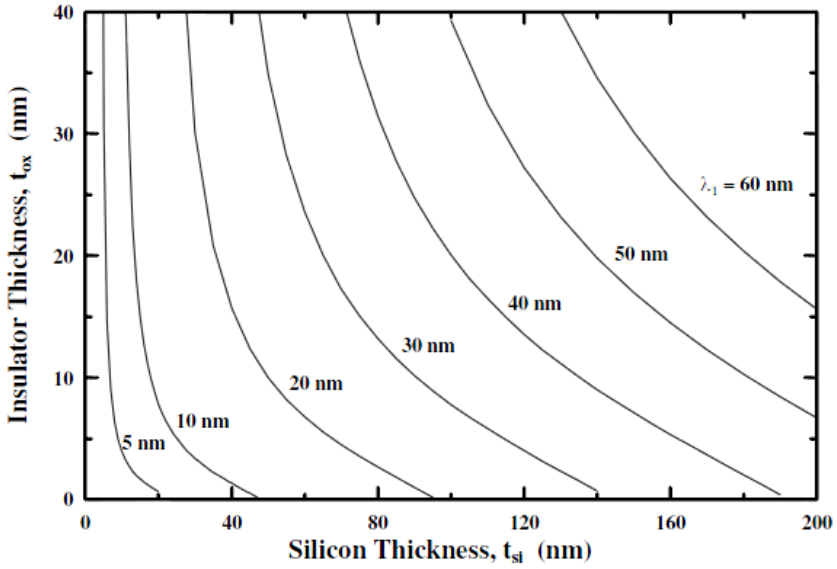


Fig. 3.6. The contour plot of the electrostatic scaling length versus insulator thickness and silicon thickness for the Dual-Material Surrounding-Gate (DMSG) MOSFETs using SiO_2 gate insulation.

Since we are primarily concerned about threshold voltage for purpose of off-current calculation in Dual-Material Surrounding-Gate (DMSG) MOSFETs, we consider only the subthreshold region, in which the mobile carriers in the channel are negligible.

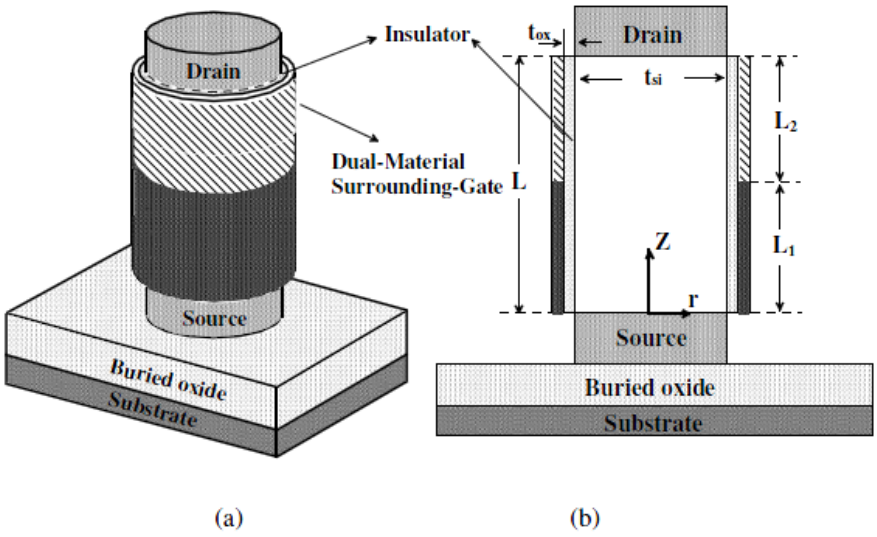


Fig.3.7 (a) Vertical Dual-Material Surrounding-Gate (DMSG) MOSFETs, (b) Cross-sectional view through the channel of Dual-Material Surrounding-Gate (DMSG) MOSFETs.

Fig.3.7 shows the schematic cross section view of Dual-Material Surrounding-Gate (DMSG) MOSFETs. The r-axis is perpendicular to the surface and r=0 refers to the center of the film. The Z-axis is parallel to the channel. Assuming a uniform impurity doping density N_a in the channel region, the two dimensional potential distribution $\emptyset(r,z)$ in the fully depleted silicon film can be obtained by solving the following Poisson's equation:

$$\frac{\partial^2}{\partial r^2}\emptyset(r,z)+\frac{1}{r}\frac{\partial}{\partial r}\frac{\partial^2}{\partial z^2}\emptyset(r,z)=\frac{qN_A}{\varepsilon_{si}} \qquad (3.23)$$

Where q is the electon charge, t_{si} is the permittivity of the silicon film. By using the superposition technique [33], the electrostatic potential $\emptyset(r,z)$ in the Dual-Material Surrounding-Gate (DMSG) MOSFETs can be written as

$$\emptyset_i(r,Z)=V_i(r)+U_i(r,Z), i=1,2 \qquad (3.24)$$

By using the superposition techique and according to the appropiate boundary conditions, we canobtain [34-35]

$$\emptyset_1(r,Z)=V_1(r)+U_1(r,Z)=\frac{qN_A}{4\varepsilon_{si}}r^2+V_{GS}-V_{FB2}-\frac{qN_At_{si}^2}{16\varepsilon_{si}}-\frac{qN_At_{xi}}{4c'_{ox}}+\sum_{n=1}^{\infty}J_0(\lambda_n r)\times \{A_ne^{\lambda_n z}+B_ne^{-\lambda_n z}\}$$

(3.25)

$$\emptyset_2(r,Z) = V_2(r) + U_2(r,Z) = \frac{qN_a}{4\varepsilon_{si}}r^2 + V_{GS} - V_{FB2} - \frac{qN_a t_{si}^2}{16\varepsilon_{si}} - \frac{qN_a t_{xi}}{4c'_{ox}} + \sum_{n=1}^{\infty} J_0(\lambda_n r) \times \left\{C_n e^{\lambda_n z} + D_n e^{-\lambda_n z}\right\} \quad (3.26)$$

Where $c'_{ox} = \frac{\varepsilon_{ox}}{t'_{ox}}$, $t'_{ox} = \frac{t_{si}}{2} \times \ln\left(1 + \frac{2t_{ox}}{t_{si}}\right)$ (3.27)

Since the coefficient of Fourier series decay so fast that the first them can dominate the potential.

$$\emptyset_1(r,Z) = \frac{qN_A}{4\varepsilon_{si}}r^2 + V_{GS} - V_{FB2} - \frac{qN_A t_{si}^2}{16\varepsilon_{si}} - \frac{qN_A t_{xi}}{4c'_{ox}} + \sum_{n=1}^{\infty} J_0(\lambda_n r) \times \left\{A_n e^{\lambda_n z} + B_n e^{-\lambda_n z}\right\}$$
$$\approx \frac{qN_A}{4\varepsilon_{si}}r^2 + V_{GS} - V_{FB2} - \frac{qN_A t_{si}^2}{16\varepsilon_{si}} - \frac{qN_A t_{xi}}{4c'_{ox}} + J_0(\lambda_n r) \times \left\{A_n e^{\lambda_n z} + B_n e^{-\lambda_n z}\right\} \quad (3.28)$$

$$\emptyset_2(r,Z) = \frac{qN_A}{4\varepsilon_{si}}r^2 + V_{GS} - V_{FB2} - \frac{qN_A t_{si}^2}{16\varepsilon_{si}} - \frac{qN_A t_{xi}}{4c'_{ox}} + \sum_{n=1}^{\infty} J_0(\lambda_n r) \times \left\{C_n e^{\lambda_n z} + D_n e^{-\lambda_n z}\right\}$$
$$\approx \frac{qN_A}{4\varepsilon_{si}}r^2 + V_{GS} - V_{FB2} - \frac{qN_A t_{si}^2}{16\varepsilon_{si}} - \frac{qN_A t_{xi}}{4c'_{ox}} + J_0(\lambda_n r) \times \left\{C_n e^{\lambda_n z} + D_n e^{-\lambda_n z}\right\} \quad (3.29)$$

Fig . 3.8. shows the surface potential as a function of normalized position along the channel for different drain voltages. It can be observed that due to the presence of step potential for the Dual-Material Surrounding-Gate (DMSG) MOSFETs, there is no significant change in the potential under M1 as the drain bias is increased. Hence, the channel region under M1is screened from changes in the drain potential. In other words, drain voltage is not absorbed under M1, but is observed under M2. As a consequence, V_{DS} exerts only a very small effect on drain current after saturation and drain conductance is reduced. On the other hand, the figure shows that shift in the point of the minimum potential is almost fixed regardless of the applied drain bias. This clearly indicates that the DIBL effect is considerably reduced for the Dual-Material Surrounding-Gate (DMSG) MOSFETs. Fig.3.9 shows the surface potential profile for a channel length of 90 nm ($L_1 = L_2 = 45\,nm$) with different drain biases. The model results from Ref.[36] are also include for comparison. It is obviously seen that our model is superior to that proposed by Ref.[36] due to better agreement between the calculated results of model and those of simulator. As an opposite to the 2D potential approach, Quasi-2D method will cause a much deviation from simulator results especially near source/drain side. Fig.3.10. shows the variation of surface potential with the normalized channel position

for different combinations of gate lengths L_1 and L_2 of metal 1and 2, respectively, Keeping the sum of total gate length, $(L_1 + L_2)$ unchanged. It is observed that the position of minimum surface potential, unfinished this causes the peak electric field in the channel to shift more toward the source end and thus there is a more uniform electric field profile in the channel, which reduced the hot carrier effects near the drain end. Moreover, the results show that the channel potential minima for the three cases are not the same. It is revealed that as the gate length of metal 1 is reduced, the position of minimum surface potential, lying under metal 1 shifts toward the source and the minimum channel potential is pulled up, which causes intense DIBL. This happens because as L_1 increases, a potential of the channel controlled by the gate metal with larger work function [37] is increased and the SCEs is suppressed substantially. Fig.3.11. shows both the calculated and simulated surface potential profile for a channel length of 90 nm ($L_1 = L_2 = 45\,nm$) with different drain biases. In addition, the simulated potential profile of the SMSG structure is included and compared to the model. In these, the Dual-Material Surrounding-Gate (DMSG) MOSFETs exhibits a peak electric field away from the drain side which therefore causes a uniform field along the entire channel and reduces the hot carrier effects (HCE). On the contrary, The MOSFETs of SMSG demonstrates the peak field almost near the drain and bring about HCE that causes tremendous drain current when the device enters saturation. Fig.3.12 shows the analytical potential contours that are compared to those simulated by two-dimensional anavice simulator –MEDICI and good agreements are observed. The potential contour under the high work function of material 1 has the tendency to bend vertically, which implies that the electric field from the gate of material 1 can easily penetrate into the channel and control the threshold behavior (this gate of material 1 is so-called control gate). On the contrary, the potential contour in the low workfunction of material 2 will bend laterally and can readily absorb the electric field from the variation of the potential of drain side and completely suppress the DIBL(this gate of material 2 is so-called screen gate).

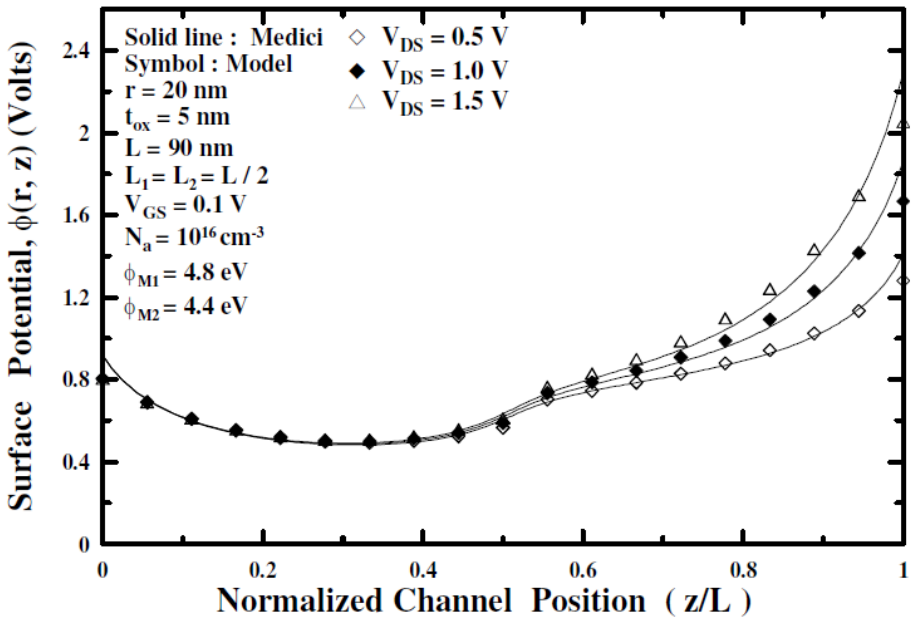


Fig. 3.8. The variation of the sueface potential with the normalized channel position. The comparison between the analytical model data and the simulation results are made.

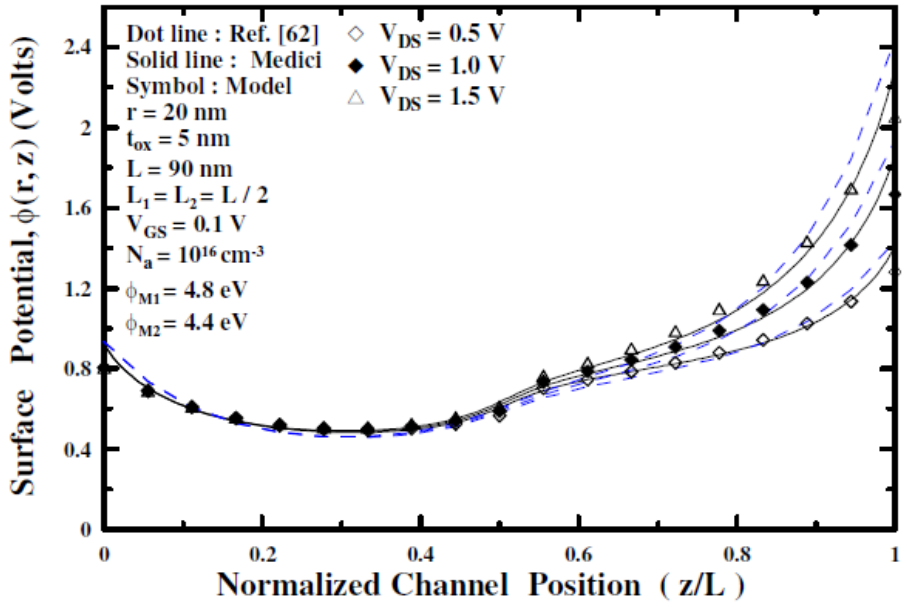


Fig. 3.9. The variation of the sueface potential with the normalized channel position. The comparison the analytical model data , the simulation results and reference made.

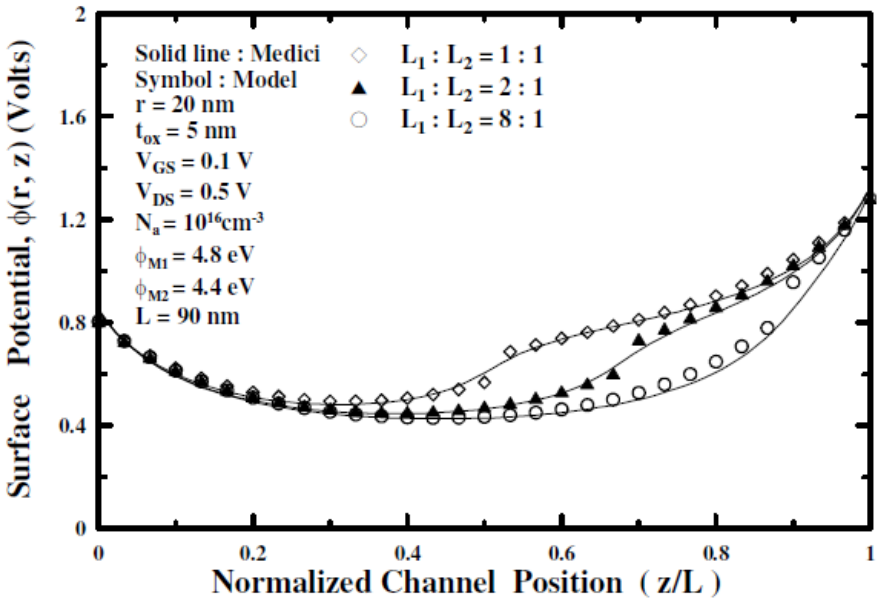


Fig. 3.10. Graph for the surface potential distribution versus the normalized channel distance (z/L) for different combinations of gate lengths L_1 andL_2 of M1 and M2.

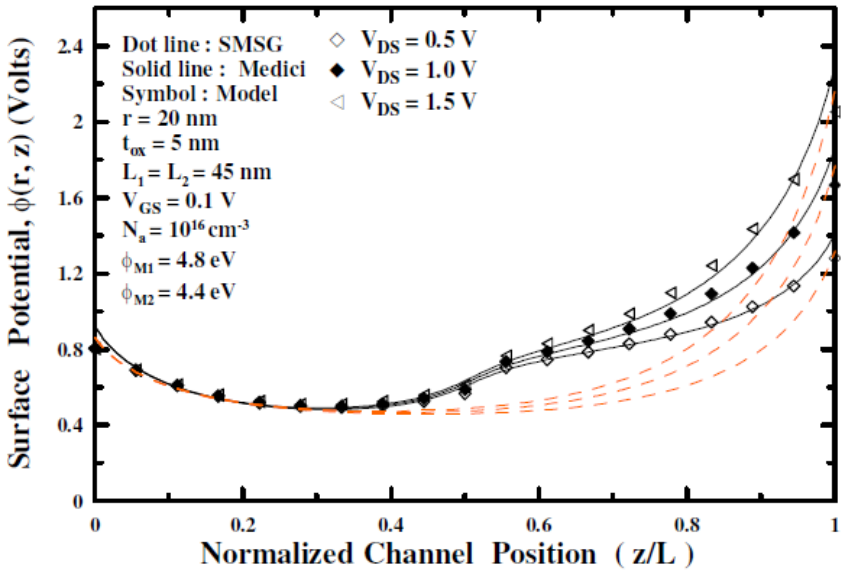


Fig. 3.11. Graph for the surface potential distribution versus the normalized channel distance (z/L) for different drain biases.The simulated potential data for the SMSG are also included for comparison.

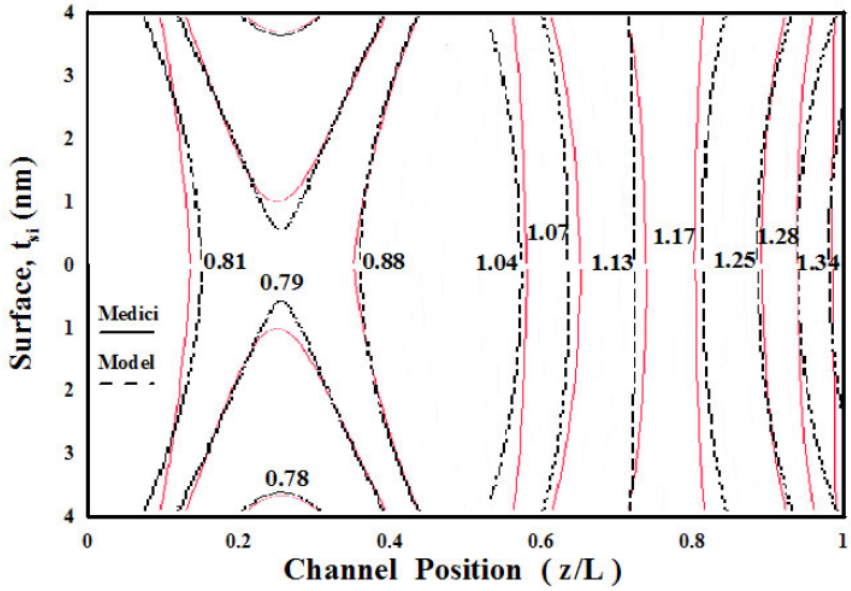


Fig. 3.12. The analytical potental contours are compared to those simulated by two-dimensional device simulator MEDICI for $L_1 : L_2 = 1 : 1$.

3.3. The influence of quantum effects on spatial distribution of carriers in surrounding-gate cylindrical MOSFETs:

3.3.1. Introduction

The evolution of modern device physics has led to the realization of devices with different promising geometries.

Among them, the cylindrical geometry is most frequently used in order to achieve device size reduction and better packaging without the appearance of short-channel effects [38, 39]. Surrounding-gate devices are the best candidate because of their unbroken explicit cylindrical symmetry.

They can appear as Si MOSFETs, as well as thin-film transistors (TFT) produced by means of organic semiconductors [40]. If first ones are considered, the inevitable step is to determine the spatial distribution of carriers over the whole semiconducting structure. So far the usual procedure was to solve the Poisson's equation for an undoped sample assuming that the carriers obeyed

Boltzmann statistics. On the other hand, the sample size is usually even smaller than a thermal de Broglie wavelength λ_D (at room temperature approximately 15nm in silicon) making quantum-mechanical effects become prominent
[38]. It might be possible to try to evaluate concentration of carriers by means of wave function obtained as a solution of 1D (one-dimensional) radial Schrodinger equation, assuming that they are subject to equilibrium Fermi-Dirac distribution. Apart from the shortcomings described in previous papers [41], this procedure would cause more serious problems than in the case of flat geometry (due to the more complex character of wave function) and could
hardly lead to a cylindrical symmetry of concentration of carriers as expected.
Therefore we will directly solve the transport equation described in our previous papers, this time introducing cylindrical symmetry by hand [41, 42]. This equation
contains quantum correction term and is especially convenient near strong barriers, where the curvature of n(r) becomes significant [38].

3.3.2. Device structure:

Let us consider the structure shown in Fig. 1. In the absence of lateral transport (voltage $V_{DS} = 0$) the concentration of carriers can be described by a set of following equations [38]:

$$\Phi_t \mathrm{grad}(n) - \mathrm{grad}(V + q) - 0 \qquad (3.30a)$$

$$q(\vec{r}) = \frac{h^2}{2me}\frac{1}{\sqrt{n}}\Delta_r\left(\sqrt{n}\right) \qquad (3.30b)$$

Where $\Phi_t = KT/e$, V is the electrostatic potential, q is the quantum correction term, n is the concentration. First of them is the transport equation in equilibrium and leads to a straight-forward Boltzmann-like solution:

$$n(r) - n_0 . \exp\left(\frac{V+q}{\Phi_t}\right) \qquad (3.31)$$

With quantum-correction term defined by means of relation (3.30b) and n_0 being an arbitrary parameter imposed by boundary conditions.

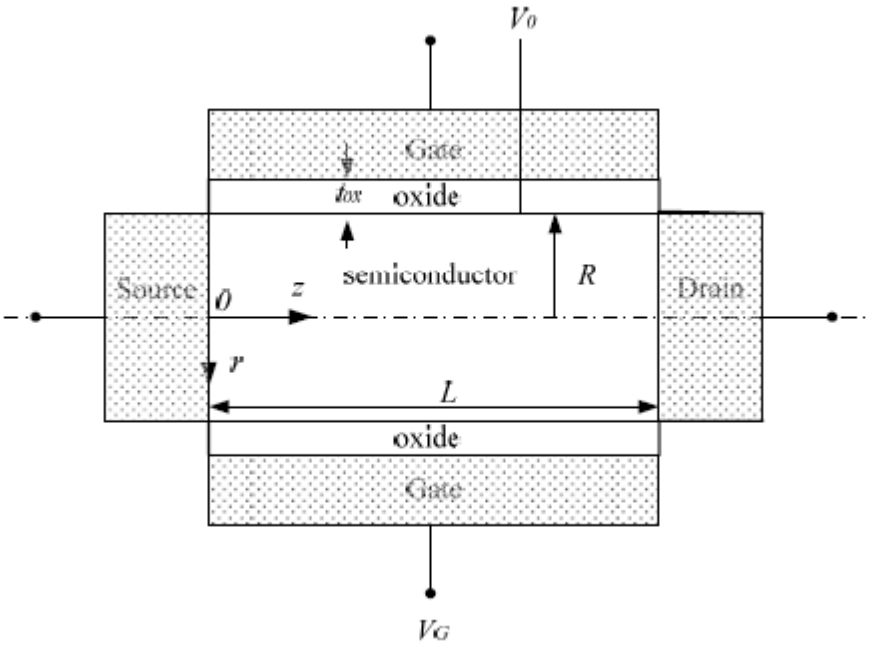


Fig. 3.13.Cross-sectional view of the cylindrical SG MOSFET.

If the channel length L is much greater than the radius of the sample, all the equations become 1D, depending only on radial coordinate r:

$$n(r) - n_0 . \exp\left(\frac{V+q}{\Phi_t}\right) \qquad (3.32a)$$

$$q(\vec{r}) = \frac{h^2}{2me} . \frac{1}{\sqrt{n}} . \left(\frac{d^2}{dr^2} + \frac{1}{r} . \frac{d}{dr}\right) . \left(\sqrt{n}\right) \qquad (3.32b)$$

Eliminating q(r) from the above set of relations, one derives a new equation that describes the variation of carriers' concentration in the presence of the applied external voltage V(r):

$$\frac{d^2 n}{dr^2} - \frac{1}{2n} . \left(\frac{dn}{dr}\right)^2 + \frac{1}{r} . \frac{dn}{dr} + \frac{4me}{h^2} . \left(V(r) - \Phi_t . \ln\frac{n}{n_0}\right) . n = 0 \qquad (3.33)$$

This voltage is certainly subject to Poisson's equation, but at the moment our goal is rather to investigate the consequences of equation (3.33) than to construct a closed self-consistent procedure. At first it must be observed that the equation (3.33) can be rewritten in a dimensionless form:

$$\frac{d^2\breve{n}}{dr^2} - \frac{1}{2n}.\left(\frac{d\breve{n}}{dr}\right)^2 + \frac{1}{r}.\frac{d\breve{n}}{dr} + \frac{4me\Phi_t}{h^2}.\left(\frac{V(r)}{\Phi_t} - \ln\breve{n}\right).\breve{n} = 0 \qquad (3.34)$$

Where:$n(r) = n_0.\breve{n}$ is valid.

Equation (3.34) turns out to be very important due to its universal character and therefore deserves to be investigated in details, while the influence of particular sample features is accounted for by taking different values

Of n_0. The choice $n_0 = N_A.\exp\left(\frac{-2\Phi_F}{\Phi_t}\right)$ describes p-doped sample , while

$n_0 = n_i.\exp\left(\frac{-\Phi_F}{\Phi_t}\right)$is valid for an undoped semiconductor, etc. Both cases assume that near the axis of the sample bulk is formed, in spite of the fact that small size of the sample (a~ 5nm-10nm) implies this statement to be contemplated much more carefully [41].

The universal character of equation (3.34) provides the possibility of imposing universal boundary conditions:

$$\breve{n}(a) = 0 \qquad (3.35a)$$

$$\breve{n}(0) = 1 \qquad (3.35b)$$

First of them is a consequence of quantum-mechanical requirement that the carriers are not able to leave semiconductor substrate and penetrate into oxide, while the second one is enabled by the arbitrarily of parameter n_0 [41].

Although equation (3.34) does not seem difficult for numerical solving at first sight, its nonlinear term can cause some problems. Fortunately, there exists a straightforward procedure to linearize it. If a new quantity z(r) according to:

$$\sqrt{\breve{n}(r)} = Z(r) \qquad (3.36)$$

is introduced, equation (3.34) appears in a much more convenient form:

$$\frac{d^2Z}{dr^2} - \frac{1}{Z}.\frac{dZ}{dr} + \frac{1}{r}.\frac{dZ}{dr} + \frac{4me\Phi_t}{h^2}.\left(\frac{V(r)}{2\Phi_t} - \ln z\right).z = 0 \qquad (3.37a)$$

together with derived boundary conditions:

$Z(a)=0$ (3.37b)

$Z(0)=1$ (3.37c)

Similar to the flat geometry case, it is very useful to introduce a new parameter with the dimension of length [41]

$$\lambda^2 = \frac{h^2}{8me\Phi_t}, \text{ i.e. } \quad \lambda = \frac{h}{\sqrt{8me\Phi_t}} \qquad (3.38)$$

With the effective mass considered, at the room temperatures the estimated value for silicon becomes $\lambda \approx 1.4$nm. This length plays a significant role in investigating how deep quantum effects penetrate into the sample. Being comparable with the radius of the sample in the order of magnitude, it gives a reliable hint that quantum effects become really prominent in the sense they can affect the device operation. Finally, the equation to be treated numerically becomes:

$$\frac{d^2Z}{dr^2} - \frac{1}{Z}.\frac{dZ}{dr} + \frac{1}{r}.\frac{dZ}{dr} + \frac{1}{2\lambda^2}.\left(\frac{V(r)}{2\Phi_t} - \ln z\right).z = 0 \qquad (3.39)$$

With boundary conditions mentioned above (3.37b, 3.37c). This equation is going to be solved in two different cases of special importance. The first one will investigate carriers' spatial distribution in the absence of external field ($V(r) = 0, \forall\ r \in D_r$), while the second one will exploit the following form of the applied voltage (Fig. 3.14):

$$V(r) = V_0\left(\frac{r}{a}\right)^{\propto} \qquad (3.40)$$

This step is supposed to be sufficient due to the limited range with respect to radial coordinate r and the dimensionless parameter α being greater than one in order to achieve the expected convexity.

3.3. 3. Numerical procedure:

The first problem one had to face with was the existence of boundary conditions specified at two different points (3.35, 3.37b, 3.37c). This fact has prevented the straightforward use of previously developed Runge-Kutta method and made one to search for alternative ones [43]. As the best candidate a "shooting" method has emerged. The essence of this procedure is to start with the presumed boundary conditions at one side of the sample [43]:

$Z(a)=0$ (3.41a)

$\frac{dZ}{dr}(a) = \theta$ (3.42b)

Where θ is the free parameter finding itself in the range $(0; +\infty)$.
The suggested procedure was to solve equation (3.39) together with boundary conditions (3.41a, 3.41b) varying the parameter θ over the whole range until the solution
satisfying both boundary conditions (3.37b, 3.37c) emerged. Only then we were able to go throw Runge-Kutta steps suggested in the literature [43]. To achieve this goal, it is convenient to renormalize the radial coordinate r in the following manner:

$y = \ln\frac{a}{r}\ ,\ 0 \leq r \leq a\ , 0 \leq y < +\infty$ (3.42)

giving equation (3.39) even simpler form:

$\frac{d^2Z}{dy^2} + \frac{a^2}{2\lambda^2}.\exp(-2y).\left(\frac{V(y)}{2\Phi_t} - \ln z\right).z = 0$ (3.43)

$V(y) = V_0.\exp(-\propto.y)\ , z(0) = 0\ ,\ \ \lim_{n\to+\infty} z(y) = 1$ (3.44)

The solution z(y) of equation (3.43) is shown in Figs. 3.14 and 3.15 and deserves some general remarks:
a) due to the exponential term exp(-2y) the solution
z(y) strongly tends to its asymptotic (constant) value even for moderate values of the unknown y;

b) if V(y)=0 the solution z(y) is convex upwards over the entire domain D_y: (0; +∞) as expected (Fig. 3.14), but introducing V(y) according to (3.44) will change this conclusion (Fig. 3.15). The concentration of carriers has a sharp peak near the oxide/semiconductor interface surpassing the asymptotic value, as also expected. It is usually said that the carriers are attracted by the potential V(y) and thus removed from the core of the sample to its border. At the very end, it is interesting to go back to initial quantities, i.e. to go through all transformations in the reverse direction; the result n (r) is shown in Fig. 3.16.
with the mostly expected behavior.

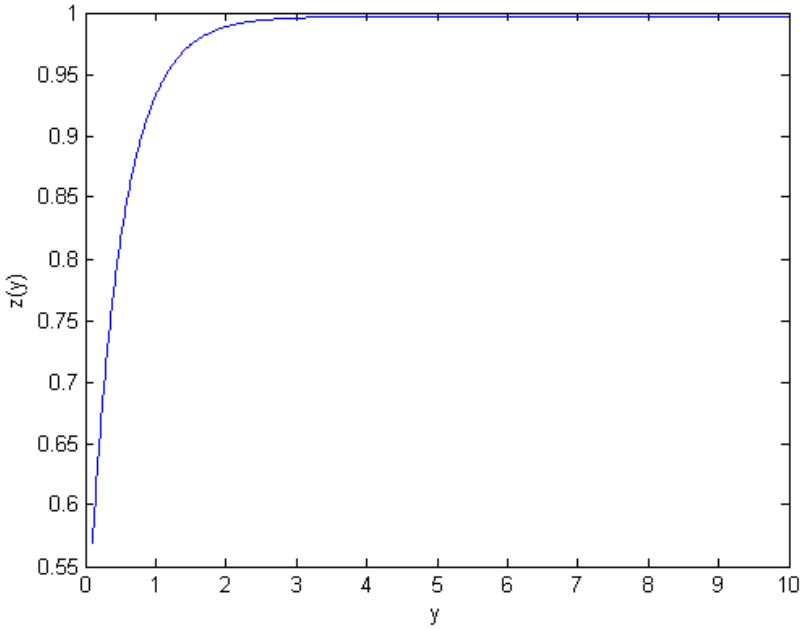


Fig. 3.14a. The results of calculation according to equation (3.43) z(y), V_0=0, a=5nm

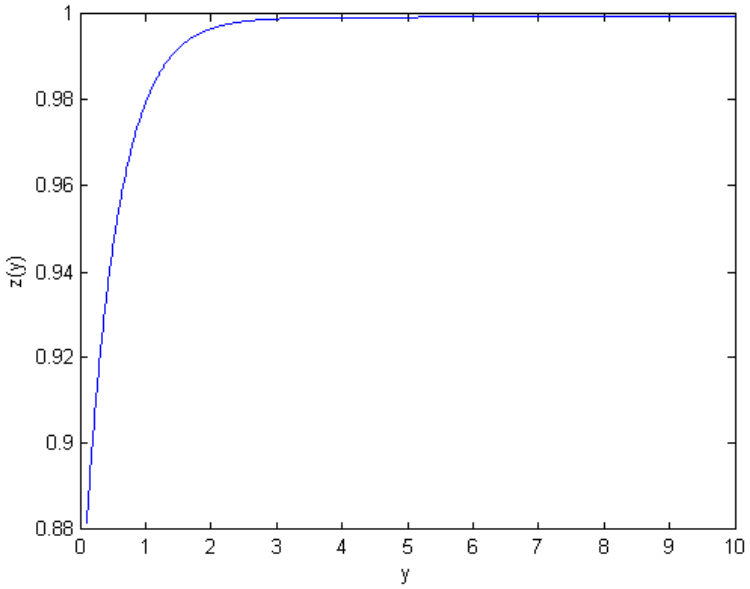


Fig. 3.14b. The results of calculation according to equation (3.43) z(y), V_0=0, a=2.5nm

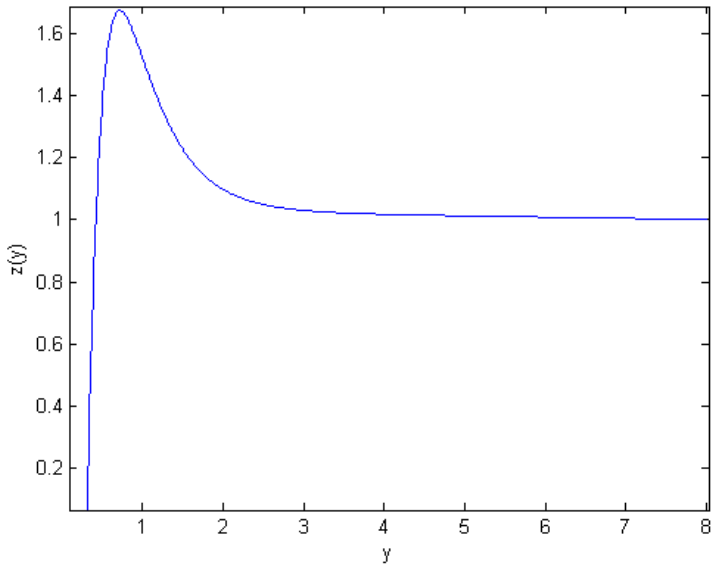


Fig. 3.15. The results of calculation according to equation (3.43) z(y), V_0=1.2V, a=3, a=5nm

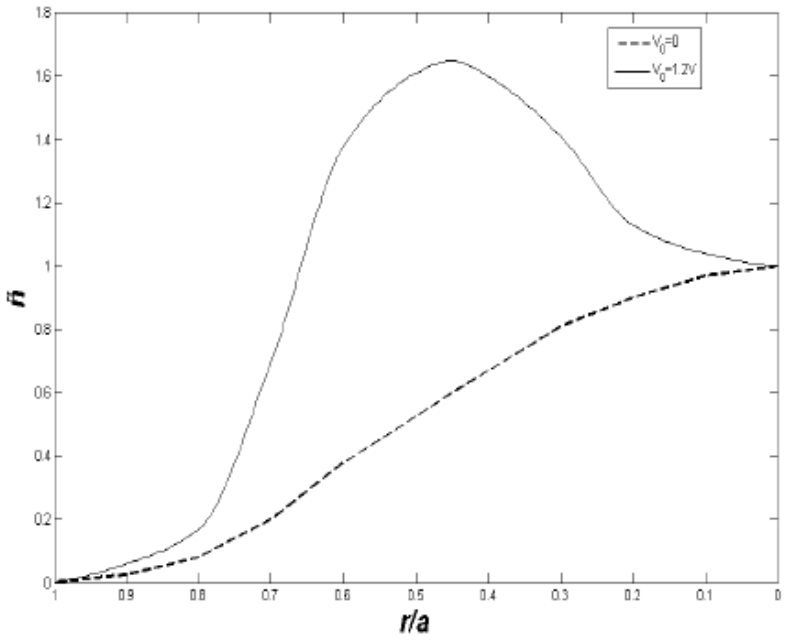


Fig. 3.16. The calculated profile of carriers' spatial distribution in SG MOSFET.

In addition to equation (3.43), it is useful to assume that the potential V(y) is subject to Poisson's equation. This set of conjugated equations must be solved exploiting self consistent procedure, but its foundation in this case is far beyond the goal of this part.

3.4. **An Improvement of Analytical *I-V* Model for Surrounding-Gate MOSFETs**

3.4.1. Introduction:

During the last decade different types of multiple gate MOSFETs (double-gate, triple-gate, quadruple-gate and surrounding-gate MOSFETs) emerge as interesting structures and candidates to relieve single-gate MOSFETs in most applications, the role of later ones becoming exhausted because they are approaching their limit imposed by gate oxide tunneling. Among them double-gate MOSFETs and surrounding-gate MOSFETs are the most promising [44].

Starting from the exact analytical solution of Poisson's equation with respect to the potential distribution across the structure, the analytical expression for carriers' density is derived [45]. Imposing it into the drift-diffusion model and taking the carriers' mobility μ as constant (not varying across the strusture), an entirely analytical model of current-voltage relation $I_D(V_{DS})$ is obtained [46,48]. But one must be aware of the fact that the effective mobility strongly depends on electric field, i.e. on the position of the carriers in the structure [45]. Therefore it was considered that this dependence should be included in the drift-diffusion model. The price to be paid was the loss of the analytic character of the current-voltage relation. In spite of this fact, the model derived in this paper causes no additional difficulties and needs only one numerical integration to be performed as a final step, what seems to be reasonable if the result is more realistic and physically based model.

Although drain-current model is not enough for circuit simulation, its as most as possible accurate shape is of great importance [45].

3.4.2.Electric Potential Analysis for SG MOSFETs

Consider an undoped cylindrical surrounding-gate MOSFET shown in figure 3.17.

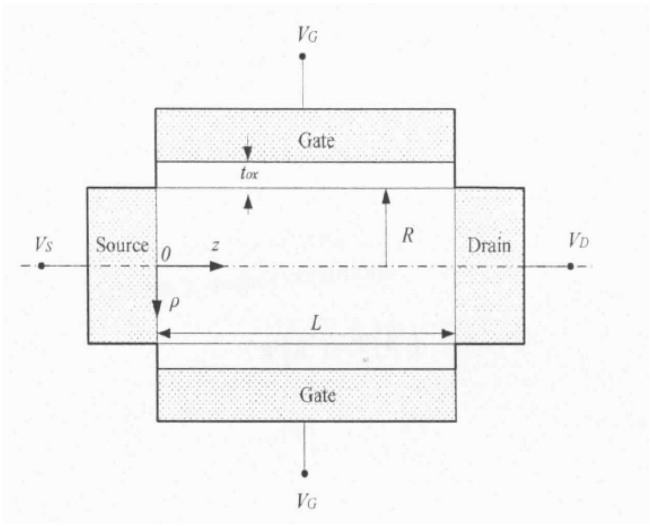


Figure3.17. Cross-sectional view of considered SG MOSFET

Due to the small normal (radial) dimension of the structure, i.e. the radius R, light doping level, usually called unintentional doping, will cause no significant departure from calculated

values. The gradual channel approximation reduces the general two-dimensional (2D) Poisson's equation to the following one-dimensional (1D) from, where all quantities are assumed to be dependent only radial coordinate ρ [47].

$$\frac{d^2\psi}{d\rho^2} + \frac{1}{\rho}\frac{d\psi}{d\rho} = \frac{q_e}{\varepsilon_{si}}.n_i.e^{\frac{q_e(\psi-V)}{nT}} = \frac{q_e}{\varepsilon_{si}}.n(\rho,z) \tag{3.45}$$

Here q_e is the electronic charge, ε_{si} is the permittivity of silicon and $\psi(\rho)$ is the electrostatic potential in the structure. The concentration of holes is considered negligible compared to the concentration of electrons, having on mind that $e^{\psi/kT} \gg 1$ if $V_G > 0$. V denotes electron quasi-Fermi potential; it is assumed to be constant with respect to radial coordinate ρ, but also slowly varies between V_s and V_D along z-axis, usually taken as $V_s = 0$, $V_D = V_{DS}$. In equation (3.45) n_i denotes the intrinsic carrier density; such form of its right side is overtaken from previous investigations, although nobody can provide a proof that in such a narrow structure bulk is going to be formed [47,48].

Fortunately, the solution of equation (3.45) can be written in a closed form which is convenient for further use [47, 48]:

$$\psi(\rho) = V(z) - \frac{2KT}{q_e}.\ln\left\{\frac{R}{2}.\sqrt{\frac{q_e^2 n_i}{2\varepsilon_{si}KT(1-\propto)}}.\left[1-(1-\propto).\frac{\rho^2}{R^2}\right]\right\} \tag{3.46}$$

where $\propto$ denotes a real number belonging to the range (0, l). It can be considered as a parameter dependent on *z* which somehow compensates the slight dependence *V(z)* and provides that the electrostatic potential depends only on radial coordinate *ρ*. In the oxide layer the Poisson's equation in the absence of any charge has a straightforward solution:

$$\psi(\rho) = C_1 \ln\rho + C_2 \tag{3.47}$$

The Poisson's equation over the entire structure (the silicon core as well as the oxide layer) is subject to following boundary conditions:

$$\psi(R^-) = \psi(R^+) \tag{3.48a}$$

$$\varepsilon_{si}.\left.\frac{d\psi}{d\rho}\right|_{R^+} = \varepsilon_{ox}.\left.\frac{d\psi}{d\rho}\right|_{R^+} \tag{3.48b}$$

$$\psi(R + t_{ox}) = V_g \tag{3.48c}$$

Eliminating parameters C_1, C_2 by means of the set of equations (3.48), one derives a crucial relation of the entire model:

$$\frac{\varepsilon_{si}}{\varepsilon_{ox}}.4\phi_t.\frac{1-\alpha}{\alpha}.\ln\left(1+\frac{t_{ox}}{R}\right)=V_g-V(z)+2\phi_t.\ln\left\{\frac{R}{2}.\sqrt{\frac{q_e.n_t}{2\varepsilon_{si}.\phi_t}}.\frac{\alpha}{\sqrt{1-\alpha}}\right\} \tag{3.49}$$

which can be rewritten in a more convenient form:

$$\frac{1}{2}\ln(1-\alpha)-\ln\alpha+S.\frac{1-\alpha}{\alpha}=\frac{V_g-V(z)}{2\phi_t}+\ln\left\{\frac{R}{2}.\sqrt{\frac{q_e.n_t}{2\varepsilon_{si}.\phi_t}}\right\} \tag{3.50}$$

$$S=2\frac{\varepsilon_{si}}{\varepsilon_{ox}}.\ln\left(1+\frac{t_{ox}}{R}\right) \tag{3.51b}$$

$$\phi_t=\frac{KT}{q_e} \tag{3.51c}$$

In previous equations t_{ox} denoyes the oxide thickness.

Although equation (3.51) is implicit of α, the approach to solve it causes no difficulties (Newton-Ralphson numerical method, graphic method ...). The importance of its solution is caused by the fact that imposing $V(0)=V_S(=0)$ and $V(L)=V_D(=V_{DS})$ where L is the channel length, gives the parameters α_s, α_1 respectively, which turn out to be inevitable in the development of models proposed in the literature [47, 48]

3.4.3.Current-Voltage Characteristic for SG MOSFETs:

Electrostatic potential derived in the previous section makes possible to determine the carriers' concentration anywhere in silicon:

$$n(z,p)=n_i.e^{q_e[\psi-V(z)]/K.T}=n_i.e^{[\psi(\rho)-V(z)]/\phi t} \tag{3.52}$$

Which enters the drift-diffusion expression of current for SG MOSFETs:

$$dI_D=q_e.\mu.n(\rho,z).\frac{dV}{dZ}.2\pi\rho.d\rho=\mu.\frac{dV}{dZ}.\frac{8\varepsilon_{si}.\emptyset_t}{R^2}.\frac{(1-\alpha).2\pi\rho.d\rho}{\left[1-(1-\alpha).\frac{\rho^2}{R^2}\right]^2} \tag{3.53}$$

The straightforward integration of equation (3.53) with respect to ρ $(0\le\rho\le R)$ and z $(0\le z\le R)$ would lead to the result known in the literature [47]:

$$I_D = \mu.\frac{8\pi\varepsilon_{si}}{L}.\emptyset_t.\int_{\propto_s}^{\propto_d}\frac{dV}{d\propto}.\frac{1-\propto}{\propto}.d\propto = \mu.\frac{8\pi\varepsilon_{si}}{L}.\phi_t^2.[f(\propto_d)-f(\propto_s)] \quad (3.54a)$$

Where:

$$\frac{dV}{d\propto} = \emptyset_t.\left(\frac{2}{\alpha}+\frac{1}{1-\alpha}+\frac{2s}{\alpha^2}\right) \quad (3.54b)$$

$$f(\alpha) = -\frac{2}{\alpha}-\ln\alpha+s\left(\frac{2}{\alpha}-\frac{1}{\alpha^2}\right) \quad (3.54c)$$

Integrating equation (3.53) into (3.54) one totally ignores the fact that the carriers' mobility depends on their position in the silicon layer. The aim of this investigation is to modify the model from the literature [47] by taking into consideration the empirical, but widely adopted formula for silicon [45]:

$$\mu(E_\rho) = \frac{\mu_0}{1+\lambda.\left|\frac{d\psi}{d\rho}\right|} \quad (3.55)$$

where μ_0, α depend on temperature and can be considered fitting parameters. As channel length L decreases, the mobility μ_0 is affected by the effects of velocity saturation and channel length modulation as well. Their contributions are of the opposite sign and mostly compensate each other in the observed range of channel lengths. Therefore μ_0 is considered roughly half of the bulk mobility (evaluated for lightly doped structures) and depends only on the magnitude of normal (radial) electric field strength (3.55) [45].

If one inserts the relation (3.55) into equation (3.53), the following expression arises:

$$dI_D = \frac{dV}{dZ}.\frac{8\varepsilon_{si}.\emptyset_t}{R^2}.\frac{\mu}{1+\lambda.4\emptyset_t.\frac{(1-\alpha).\frac{\rho}{R^2}}{1-(1-\alpha).\frac{\rho}{R^2}}}.\frac{(1-\alpha).2\pi\rho.d\rho}{\left[1-(1-\alpha).\frac{\rho}{R^2}\right]^2} \quad (3.56)$$

Integration with respect to ρ $(0 \le \rho \le R)$ can be analytically performed; the integrating procedure is described in calculus textbooks (the integration of rational functions by means of Ostrogradsky method):

$$I_D = \frac{8\varepsilon_{si}.\phi_t.2\pi(1-\alpha)}{R^2}.\frac{dV}{dz}.\mu.I(\alpha,\lambda) \quad (3.57a)$$

With:

$$I(\alpha,\lambda)=\int_0^R \frac{\rho.d\rho}{\left[1-(1-\alpha).\frac{\rho}{R^2}\right].\left\{\left[1-(1-\alpha).\frac{\rho}{R^2}\right]+\lambda.4\emptyset_t.\frac{(1-\alpha).\rho}{R^2}\right\}} \quad (3.57b)$$

i.e.:

$$I(\alpha,\lambda)=\frac{1}{b\sqrt{a}}.\left\{\frac{1}{2}\ln\frac{1+\sqrt{1-\alpha}}{1-\sqrt{1-\alpha}}-\frac{1}{2\sqrt{1+\left(\frac{b}{2\sqrt{a}}\right)^2}}.\left[\ln\left|\frac{\sqrt{1+\left(\frac{b}{2\sqrt{a}}\right)^2}+\left(\sqrt{1-\alpha}-\frac{b}{2\sqrt{a}}\right)}{\sqrt{1+\left(\frac{b}{2\sqrt{a}}\right)^2}-\left(\sqrt{1-\alpha}-\frac{b}{2\sqrt{a}}\right)}\right|-\ln\frac{\sqrt{1+\left(\frac{b}{2\sqrt{a}}\right)^2}-\frac{b}{2\sqrt{a}}}{\sqrt{1+\left(\frac{b}{2\sqrt{a}}\right)^2}+\frac{b}{2\sqrt{a}}}\right]\right\} \quad (3.57c)$$

With the abbreviations:

$$\alpha=\frac{1-\alpha}{R^2} \quad (3.57d)$$

$$b=\lambda.\frac{4\phi_t.(1-\alpha)}{R^2} \quad (3.57e)$$

Next step in the standard procedure is the integration over z which leads to a final result:

$$I_D=\frac{8\varepsilon_{si}.\phi_t.2\pi}{R^2.L}.\mu.\int_{\alpha_s}^{\alpha_d}\frac{dV}{d\alpha}.(1-\alpha).I(\alpha,\lambda).d\alpha \quad (3.58a)$$

$$I_D=\frac{8\varepsilon_{si}.\phi_t.2\pi}{R^2.L}.\mu.\int_{\alpha_s}^{\alpha_d}\left(\frac{2}{\alpha}+\frac{1}{1-\alpha}+\frac{2s}{\alpha^2}\right).(1-\alpha).I(\alpha,\lambda).d\alpha \quad (3.58b)$$

Unfortunately, this integration can't be performed analytically. Although the numerical procedure is necessary, it turns out to be very simple by means of any of methods described in the literature. At the end just to be mentioned that the suggested improvement of the previous model will not break its most important features (triode regime, the onset of saturation, etc.).

3.4.4.Numerical Results and Discussion :

In order to bring the results nearer to the spectator, the dimensionless ("normalized") part of the drain current according to relations (3.57) is calculated:

$$I_D^*=\frac{I_D}{\mu.\frac{8\pi\varepsilon_{si}}{L}.\emptyset_t^2}=\frac{2}{R^2}.\int_{\alpha_s}^{\alpha_d}\left(\frac{2}{\alpha}+\frac{1}{1-\alpha}+\frac{2s}{\alpha^2}\right).(1-\alpha).I(\alpha,\lambda).d\alpha \quad (3.59)$$

The results of the calculation for two different sets of geometric parameters *(R=5nm, t_{ox}=1.5nm, $L=1.5nm$* and *R=2.5nm, t_{ox}=1.5nm, $L=1\,\mu m$* with a varied gate-source voltage V_{GS} are shown in figures 3.18 and 3.19 respectively. In each of these figures the parameter *A*

(responsible for the mobility degradation - the effect to be examined in this part is also varied in a reasonable range around the value adopted for silicon: $\lambda_0 = 0.025\ \mu m/V$

$$\lambda = \eta.\lambda_0 \tag{3.60}$$

In order to expose the results in a more transparent manner, the dimensionless parameter η is introduced($\eta = 1$ corresponds to degradation due to λ_0, while $\eta = 1$ denotes the absence of degradation).

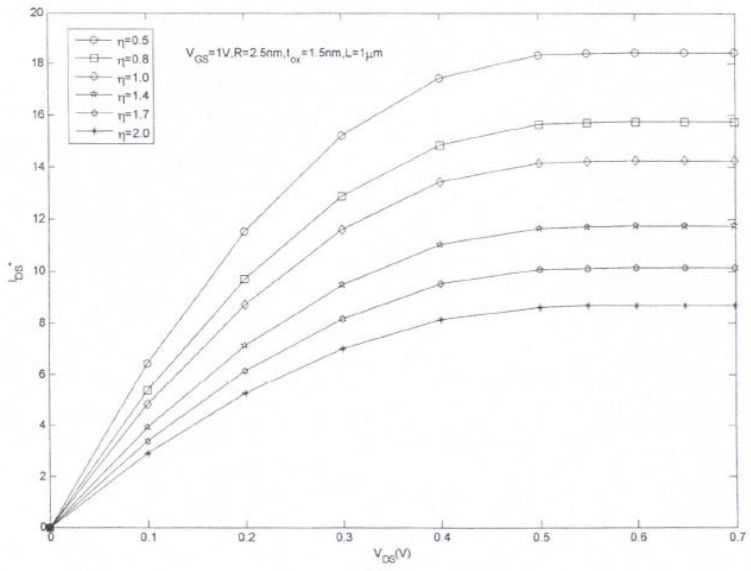


Figure 3.18a The "normalized" drain current I_{Ds}^{*} versus drain-to-source voltage V_{DS} for a specific set of geometric and technological parameters in the presence of mobility degradation

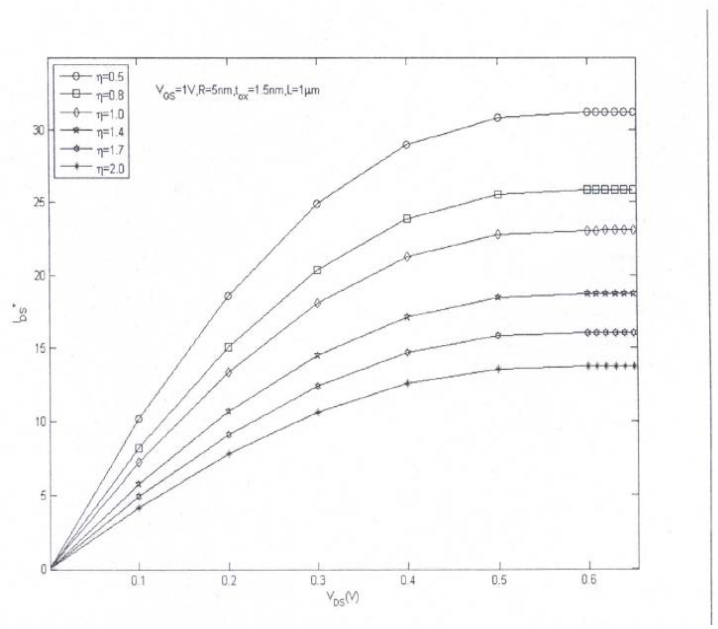


Figure 3.18b The "normalized" drain current I_{Ds}^{*} versus drain-to-source voltage V_{DS} for a specific set of geometric and technological parameters in the presence of mobility degradation

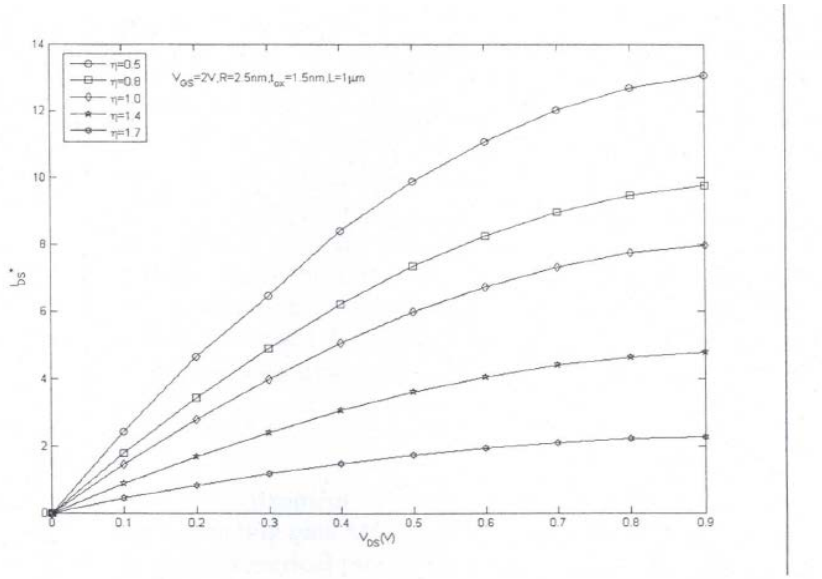


Figure 3.19a The "normalized" drain current I_{Ds}^{*} versus drain-to-source voltage V_{DS} for a specific set of geometric and technological parameters in the presence of mobility degradation

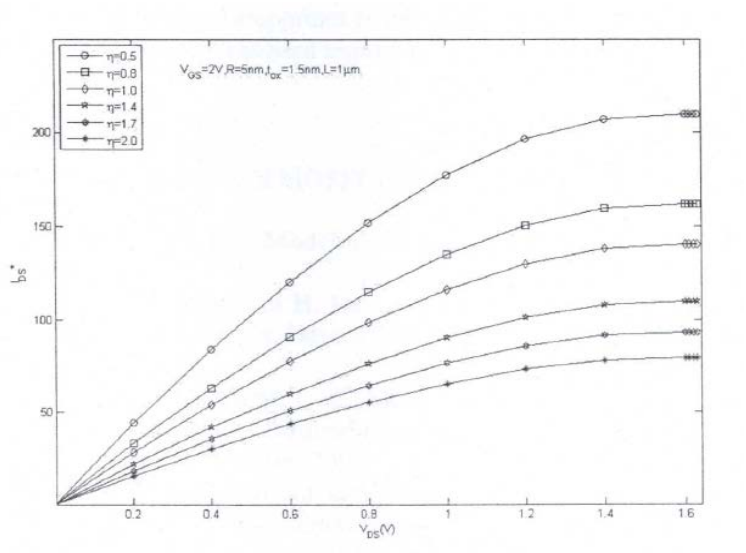


Figure 3.19b The "normalized" drain current I_{Ds}^{*} versus drain-to-source voltage V_{DS} for a specific set of geometric and technological parameters in the presence of mobility degradation

Obviously, the increase of $\lambda(\eta)$ decreases the magnitude of drain current for all values of V_{DS}, while the shape of the characteristic and the onset of saturation remain unaffected (as expected). If the goal is to estimate the influence of described improvement on the existing model, then it is necessary to compare the values of drain current for $\eta = 0$ with the values for some chosen $\eta \neq 0$ ($\eta = 0$ for example - the bolded curves in corresponding figures). The interesting conclusion is that the ratio $I_D^*(\eta = 0)/I_D^*(\eta = 1)$ will have similar values lying between 0.5 and 0.55 over the whole range of drain-source voltages V_{DS}.

While $\eta = 1$ ($\lambda = \lambda_0$) corresponds to the values usually adopted for silicon, the influence of mobility degradation on current-voltage characteristic turns out to be considerable. Unfortunately, the lack of experimental data for the chosen set of geometric parameters makes the further search for more exact value of parameters μ, λ impossible.

3.5.Conclusion

In The influence of quantum effects on spatial distribution of carriers in surrounding-gate cylindrical MOSFETs a method for introducing quantum effects on the carriers' concentration profile and their transport properties, previously developed bringing together the achievements of quantum mechanics and statistical physics, has been applied to devices with recently designed and promising cylindrical geometry. The 1D equation describing this concentration profile for rather long-channel devices has been derived, transformed and numerically solved in two cases of the greatest interest ($V(y)=0$ and $V(y)\neq 0$ as postulated). The invariance of the obtained equation under multiplication of n(r) by an arbitrary quantity n_0 provides it some kind of universal character. That means it can be solved for any constant value n_0 (for example $n_0=1$) and only then the actual boundary conditions for r=0 are implemented. The role of quantum effects is unquestionable. The lateral dimension of the sample implies that quantum effects (here appearing as edge effects) penetrate deep into semiconductor sample and spread over the prevailing part of it. Therefore, it can be reasonably assumed that these quantum effects have a great influence on a device operation.

And in An Improvement of Analytical *I-V* Model for Surrounding-Gate MOSFETs considerable improvement of the existing analytical model of current-voltage characteristic for surrounding gate MOSFETs was presented. The price to be paid was the appearance of a simple numerical procedure in our model. On the other hand, the model proposed in this part is more realistic and makes the more detailled investigation of carriers' mobility in similar silicon structures possible. The as much as possible exact knowledge of current-voltage characteristic is found to be of great importance because the drain current expression strongly affects conductance, transconductance and terminal capacitance coefficients, thus having a great influence on dynamic behavior of such devices. Therefore, it is believed important to try to incorporate an improved model into circuit simulation for dc, ac and transient regime as well.

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7- Figure 1.7 Equivalent circuit of the MOS capacitor. Reproduced from Shur M. (1990) Physics of Semiconductor Devices, Prentice Hall, Englewood Cliffs, NJ

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61. **Figure 3.19b** The "normalized" drain current I_{Ds}^{*} versus drain-to-source voltage V_{DS} for a specific set of geometric and technological parameters in the presence of mobility degradation.

KRATKA BIOGRAFIJA

ABEDALHKEM SALEMAN ALKOASH JE ROĐEN 12..1969. U SABRATI(LIBIJA) . OPŠTU GIMNAZIJU ZAVRŠIO JE U SABRATI(LIBIJA) 1988. SA VRLO DOBRIM USPEHOM .DIPLOMIRAO JE 1992. GODINE NA TEHNOLOŠKOM FAKULTETU – ODSEK FIZIČKIH NAUKA – UNIVERZITETA ″ SEDMI APRIL ″ U ZAVIJI (LIBIJA). ZAVRŠIO JE KOMPJUTERSKU OBUKU 2000.GODINE NA INSTITUTU U SABRATI (LIBIJA).ZAVRŠIO JE TAKODE KURS (SREDNJI NIVO)SLI NA INSTITUTU ZA ENGLESKI JEZIK U BRNU ČEČKA . MASTER-STUDIJE JE ZAVRŠIO NA UNIVERZITETU VUT (BRNO,ČEŠ-KA)2006.GODINE IZ OBLASTI MIKROELEKTRONIKE.RADIO JE KAO PROFESOR GIMNAZIJE U SABRATI (1992- 2000), A ZATIM KAO POMOČNIK U ODSEKU ZA FIZIKU NA UNIVERZITETU ″ SEDMI APRIL ″ U AL- ZAVIJI (LIBIJA,2002-2003). NA KRAJU JE RADIO KAO ČLAN ODBORA ZA OBRAZOVANJE (2006 -2008) NA ODSEKU ZA ELEKTRONSKU FIZIKU UNIVERZITETA ″ SEDMI APRIL ″

IZJAVA

SA PUNOM ODGOVORNOŠĆU IZJAVLJUJEM DA PREDLOŽENU TEMU POD OVIM NAZIVOM NISAM PRIJAVIO NA BILO KOJOJ USTANOVI U ZEMLJI ILI INOSTRANSTVU

ABEDALHKEM ALKOASH

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Потписани-а Abedalhkem Sleman Ahmed Alkoash

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The investigation of electro physical properties of sic and its application in **Nanoelectronic** devices

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Име и презиме аутора Abedalhkem Sleman Ahmed Alkoash

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Студијски програм: The investigation of electro physical properties of sic and its application in **Nanoelectronic** devices.

Наслов рада _ Ментор**: Dr.Rajko Sašič**

Потписани : Abedalhkem Sleman Ahmed Alkoash

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The investigation of electro physical properties of sic and its application in **Nanoelectronic** devices

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