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Investigation of Silicon Carbide Based High Voltage And High Power Electronics Components

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(Allah have mercy on them and bring them into the paradise)

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Abstract:

Silicon has been the number one choice of materials for over 40 years. It has reached an almost perfected stage through extensive research for so many years; now it is cheap to be manufactured and performs very reliably at room temperature. However, as modem electronics move to a more advanced level with increasing complexity, materials other than silicon are under consideration. Several areas where Silicon shows shortcomings in high temperature environments and high voltage conditions. The Silicon devices need to be shielded – cooled, are limited to operation at low temperature and low blocking voltage by virtue physical and electric properties. So silicon devices are restricted and have focused on low power electronics applications only, these various limitations in the use of Si devices has led to development of wide band gap semiconductors such as Silicon carbide . And because there is an urgent need for high voltage electronics for advanced technology represented in (transportation - space - communications - power systems) in which silicon has failed to be used. Due to various properties of Silicon carbide like lower intrinsic carrier concentration (10–35 orders of magnitude), higher electric breakdown field (4–20 times), higher thermal conductivity (3–13 times), larger saturated electron drift velocity (2–2.5 times),wide band gap (2.2 eV) and higher, more isotropic bulk electron mobility comparable to that of Si. These properties make it a potential material to overcome the limitations of Si.

The fact that wide band gap semiconductors are capable of electronic functionality, particularly in the case of SiC. 4H-SiC is a potentially useful material for high temperature devices because of its refractory nature. So Silicon Carbide (SiC) will bring solid-state power electronics to a new horizon by expanding to applications in the high voltage power electronics sectors. It is the better choice for use in high temperature environment and high voltage conditions. Silicon carbide is about to replace Si material very quickly and scientifically will force Si to get retired. The superior characteristics of silicon carbide, have suggested considering as the next generation of power semiconductor devices. And because our study will concentrate on the use of semiconductors on high voltage unipolar power electronics devices. DIMOSFET will be

our candidate to support the study of potential utilization of the emerging silicon carbide (SiC) unipolar devices.

The present work aims at the design of high breakdown voltage of (DIMOSFET) double implanted metal- oxide semiconductor field effect transistor by extending the drift region to three sections, with uniformly and linearly graded doping profile which is responsible for the specific on resistance (internal dynamical resistance) which will be minimized. Confirming our investigation by mathematical modeling and calculating the voltage drop across these sections and simulation in drift region to show its characteristics and various properties.

UDC Number: 546.281'261:539.183.3

Sažetak :

Takom paslednjich Četrdeset godina gilicijum je bio najzastupljeniji poluprovodnički materijal.takom godina istražen je do savršenstva,sada se jeftino proizvadi i panzdana funkcio-niše na sobnim temperturama .Ali maderna elekronika biva sve kompleksnija i drugi materijali osim silicijnma se razmatrajn.Neke od primena gde silicijum pakazuje nedostathe su one sa povišenom temperaturom ili povišenim naponom. Silicijumske komponente magn se koristiti pri niŽim temperaturama i nižim blokirajućim naponima,što implicira primenu u kolima ni že snage . Ovi nedostaci silicijuma doveli su do taga da u nekim situacijama silicijum –karbide sve češće zauzi-ma njegovo mesto.meatu glavnim prednostima silicijum-karbida su niža sapstvena koncentracija nosilaca,veća vrednost probejnog električnog polja ,veća toplotna provo dnost,veća brzina nasilaca u zasićenju,širok energetski procep kao i manje izražens anizotropija pokret ljivosti nega kad silicijuma.

Sobziromiram da je širok energetski procep poželjna osbina sa stan ovišta funkcionisanja silicijum karbid je na najbaljem putu da istisue silicijum u karbide je na najbaljem putu da istisne silicijum u nekim priormenama,posebna visoka temperaturskim iu kolina pavećance snage.

Naše istraživanje biće posvećeno primeni ovog mate rijala u gere navedence srrhe,a sve to biće učinjeno na primeru VDIMOSFET – a (Vertikalnog dvostruko implantiranog metal – oxside – poluprovodnik tranzistara sa elektom polja). Na bazi matematičkih proračuna od govarajućih modela biće predložen izvesna poboljšanja kejhće se koristit pri dizanu.

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LIST OF USED ACRONYM

CVD: Chemical Vapor Deposition

eV: Electron Volt

HTCVD: High Temperature Chemical Vapor Deposition

LPE: Liquid Phase Epitaxy

MESFET: Metal-Semiconductor Field Effect Transistor

MOSFET: Metal-Oxide Semiconductor Field Effect Transistor

SBD: Schottky Barrier Diode

SBH: Schottky Barrier Height

SiC: Silicon Carbide

SiO_2 **:** Silicon dioxide

JFET: junction field effect transistors

DRAM: dynamic random access memory

V_{TH}: threshold voltage

BVDSS: breakdown drain source voltage

V_{BR}: breakdown voltage

VGS: gate source voltage

V_{DS} : drain source voltage

LED: light Emitting diode

HVDC: high voltage direct current

VPE: Vapor Phase Epitaxy

Eg **:** Energy bandgap

E_C **:** Energy Conduction Band

E_{fm} **:** Metal Fermi Level

f_m **:** Metal Work Function

f_S **:** Semiconductor Work Function

E_{fs} **:** Semiconductor Fermi Level

E_0 **:** Vacuum Level

f_{Bn} : Barrier height of n-type semiconductor

f_{Bp} : Barrier height of p-type semiconductor

f_{B} : Barrier height

V_{bi} : Built in voltage

ε_{S} : Permittivity of semiconductor

ε_{0}: Permittivity of free space

V : Applied voltage to Schottky Contact

N_{D} : Doping concentration of semiconductor

J : Current Density

k : Boltzmn constant

T : Temperature

q : Electronics Charge

n_{i}: Intrinsic Carrier Concentration

ε_{cr} : Critical electric field

$R_{on\,sp}$: Specific on-resistance

μ_{n} : Electron mobility

J_{L} : Leakage Current Density

V_{R} : Reverse Bias Voltage

BJT: Bipolar Junction Transistor

CV: Capacitance vs. Voltage

EC: Critical Electric Field

EB :The breakdown electric field

EF: Fermi Energy

F-D: Fermi-Dirac

GTO: Gate Turn-off Thyristors

HVDC: High-Voltage Direct-Current

IGBT: Insulated Gate Bipolar Transistor

Lp: Hole Diffusion Length

MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor

N: Nitrogen

1. Introduction

The first solid state devices were fabricated using germanium (Ge) which was considered as the semiconductor material of the future. But later on, silicon (Si) turned out to be more suitable for several reasons [1, 2, 3, and 4]. Silica, the source of Si is widely available, and it is easier to get high purity Si from it. Si can easily be doped to Produce n- type-type and semi-insulating material [5].Another very important reason is that a native oxide SiO_2 can be grown on Si using thermal oxidation at the relatively low temperature of around $900^{\circ}C$ [6, 7 ,8]. These characteristics make Si semiconductor industry favorite.

At present, our national semiconductor industry as total is more than $290 billion [9]. Around 10% of this worth is in smart integrated circuits and electronic power devices [10, 11]. More than 50% of our electricity is conditioned by electronic power devices [12, 13]. These devices are important because they determine the cost and efficiency of electronic systems. Hence they have a greater impact on the economy of a country. The arrival in the 1950s of solid state devices like the bipolar transistor led to the replacement of vacuum tubes [13,14], and these improvements made possible the Second Electronic Revolution with silicon as the material of choice. Silicon – based power devices have dominated the power systems applications in along period of time. Devices such as bipolar ,unipolar, controlled ,uncontrolled, MOS-gated made by Si are widely used by power electronics and power systems designers .The breakthroughs in the areas of Si power semiconductor device physics, electric and process technology in the middle of last century have accelerated the development of Si power electronic devices. Si power electronic devices started with the invention of the bipolar junction transistor (BJT) in 1950s, and have experienced three stages as shown as in Fig .1.1 In the 1960s, the appearance of the thyristor started the first period in the history of power semiconductor devices and opened up many possibilities for the growth of power electronics as general. In the second half of the 1970s the two controllable non-latching type devices, the bipolar transistor module and the gate turn-off thyristor (GTO), were introduced to match the growing demand for inverter-controlled power conversion equipment, which quickly became the focus of power electronics growth.

This started the second period in the chronological evolution of power semiconductor devices. The introduction of power MOSFETs in the 1970s enabled compact and efficient system designs, particularly which was based on low voltage (less than 200V)

applications. To improve performance and reliability, the DMOS process and trench gate technologies were adopted subsequently, and these became the predominant options for device manufacturers. The third period in the late 1980s through early 1990s focused on MOS-gated device physics blended with the bipolar transistor.

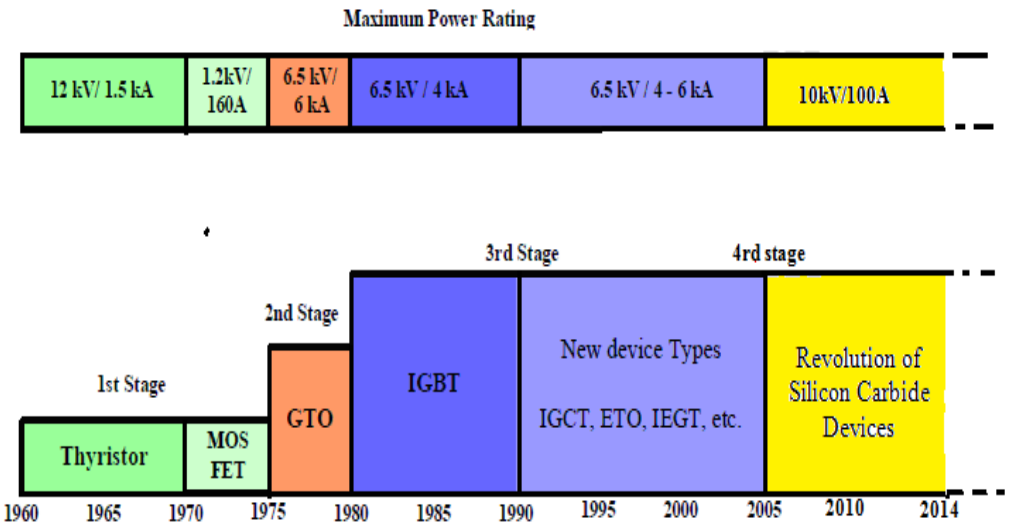


Figure 1-1.time line of semiconductors power electronic devices

As a result, the evolutionary power device, the insulated gate bipolar transistor (IGBT) was put into practical use and has been a key component for the acceleration of power electronics. The IGBT, by virtue of its MOSFET-like insulated gate controllability and bipolar-like conductivity modulated on-state operation, has successfully shown its ability to perform adequately in high power and high frequency fields [15, 16]. However, in the recent decade, no new concepts of power electronic devices were introduced to the market though some new types of improved power electronic devices has been developed by optimal integration of the existing technologies, such as the integrated gate-commutated turn-off (IGCT) thyristor; the MOS-Controlled thyristor (MCT), the emitter turn-off (ETO) thyristor, the injection enhanced (insulated) gate transistor (IEGT). Some typical applications are shown in Fig. 1.2. The development of Si power electronic devices has slowed. After more than one half century's efforts, Si semiconductor technology has been highly developed. Today, the main goal of researchers and manufacturers has been integrating and perfecting the features and characteristics of the existing devices. It is hard to achieve any breakthrough. The power handling of IGBTs and GTOs increased initially at a rate of roughly and the same for other devices the rate of growth diminished. So some changes have taken place that

have drawn more attention to silicon (Si) devices for it is powerless to operate for high voltage devices.

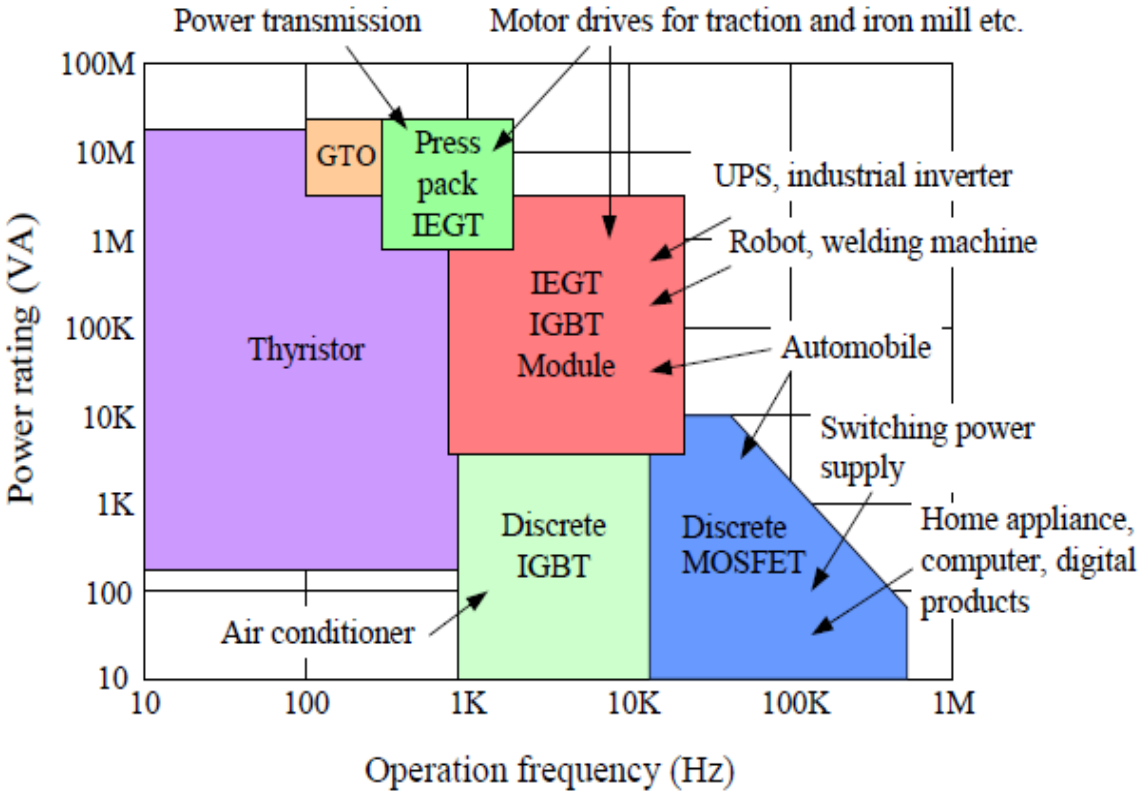


Figure. 1.2. *Comparisons of devices application fields [17]*

The present silicon (Si) technology is reaching the material's theoretical limits and can not meet all the requirements. It is already proven that even the first SiC based power devices surpass Si's theoretical limits. SiC power devices can work in harsh environments where Si power devices cannot operate. Therefore there are good reasons to believe that the improvements will begin to saturate in the future. A substantial reason behind this is that Si power electronic devices are reaching the fundamental limits imposed by the material of Si. And the requirements of present and the future high-performance power electronic systems are exceeding the power density, efficiency, and reliability of silicon-based devices. The first generation semiconductors devices require heavy and bulky heat sinks to reach their operational temperature limits at approximately 350°C, are highly susceptible to harsh environments such as intense radiations, and have a switching limit in the range of a few gigahertz (GHz). On the other hand, SiC devices could operate at temperatures up to 600°C, at switching

frequencies in the 10-100 GHz range and at increased power densities. These lighter, more compact high density power devices operating in harsh environments or at high temperatures would meet the requirements spanning many areas of both the military and civilian sectors. Although very few SiC devices are currently commercially available.

1.1. (SiC) As the Promising Semiconductor for High Power Devices

The electronic revolution during the 20th century is mainly based on silicon and it can be regarded as the first generation semiconductors. On the late of twentieth the advanced and matured Si semiconductor technology has been pushing Si-based power electronic devices to their material limits. Alternative materials has been starting imposing it self and are being developed for future power electronic devices. Around the turn to the 21st century gallium arsenide and indium phosphide have evolved as second generation semiconductors constituting the base for wireless and information revolution. Now at the start of the 21st century, the wide band semiconductors silicon carbide and gallium nitride are on the rise and may be regarded as the third generation semiconductors used in the electronic and optoelectronic industries.

Silicon carbide (SiC) has been recently given renewed attention as a potential material for the high power and high frequency applications requiring high temperature operation. And application requiring large radiation damage resistance. Properties such as large breakdown electric field strength and large constant, reasonably high electron mobility, and high thermal conductivity make SiC attractive for fabrication of power devices with reduced power losses and die sizes .high thermal conductivity and breakdown electric field also suggest that integration of devices, with close to ideal characteristics, offer great performance improvement. Some of the advantages compared with Si based power device are as follows:

- SiC has low resistance because it has reduced drift region widths due to high band gap and less on state on resistance. Hence, silicon carbide devices have lower conduction losses compared to silicon.
- High switching frequency – the high velocity saturation and thinner drift region associated with high band gap make the device switch faster.
- The blocking voltage of a SiC component can be ten times higher, compared to an equal large Si component, which makes it more suitable automotive industry .in addition, the resistance is lower at voltage over 200V compared to Si.

- Smaller heat sinks – thermal conductivity of SiC is three times greater than silicon. This results in reduced thermal management system.
- SiC unipolar devices are thinner, and they have lower on resistance. At low breakdown voltages (50V), these devices have specific on resistance of 1.12μΩ around 100 times less than their Si counterpart's .At higher breakdown voltages (5000V), this goes up to 29.5mΩ, 300 times less than comparable si devices. With lower R_{on} , SiC power devices have lower conduction losses; therefore, higher overall converter efficiency is attainable .
- Silicon carbide devices are highly reliable because, the static and dynamic characteristics do not vary much with the variation in temperature compared to it is counterparts.
- SiC based power devices have higher breakdown voltages because of their higher electric breakdown field ;Si Schottky diodes are commercially available typically at voltages lower than 300V,but the first commercial SiC schottky diodes are already rated at1450V.
- SiC has a higher thermal conductivity (4.9 W/ cm K for SiC and 1.5 W/cm-K for Si) ; therefore ,SiC power devices have a lower junction to case thermal resistance ,$R_{th\text{-}jc}$ (0.02K/W for SiC and 0.06 K/W for Si) ; device temperature increase is slower .
- SiC device operate at up to 600°C is mentioned in the literature. Si devices, on the other hand, can operate at maximum junction temperature of only 150°C.
- SiC is extremely radiation hard ; irradiation does not degrade the electronic properties of SiC ;therefore ,a SiC converter can be used in aerospace applications decreasing the weight of the vehicles due to reduced radiation shielding .
- Forward and reverse characteristics of SiC power devices change only slightly with temperature and exploitation time; therefore, they are more reliable.
- SiC based bipolar devices have excellent reverse recovery characteristics. With less reverse recovery current, the switching losses and EMI are reduced, and there is less or no need for snubbers. As a result, there is no need to use soft switching losses.
- Because of low switching losses, SiC based devices can operate at higher frequencies (>20 kHz) not possible with Si based devices in power levels of

more than a few tens of kilowatts. High switching frequency in power converters is highly desirable because it permits use of a smaller size capacitors, inductors, and transformers, which in turn can reduce over all size and weight.

- Silicon carbide is a very hard and strong material and is not attacked by any acids or alkalis or molten salts up to 800˚C. In air, SiC forms a protective silicon oxide coating at 1200˚C and able to be used up to 1600˚C the high thermal conductivity coupled with low thermal expansion and high strength give this material exceptional thermal shock resistant qualities .
- Forward resistance of SiC power devices is approximately 200 times lower than that of conventional silicon devices.
- Silicon carbide devices are highly reliable because the static and dynamic characteristic do not change much with the variation temperature compared to it is counter parts.

Silicon carbide disadvantages:

- Low prosing yield because of micro pipe defects. The wafers available have < 1/ cm^2 , but they are more expensive than the typical wafer with < 10/cm^2 .
- Higher device cost due to unavailability of large wafers.
- Limited availability only Schottky diodes at relatively low power are commercially available.
- Need for high temperature packaging techniques that have not yet been developed.

These disadvantages are expected considering that SiC technology has not matured ,yet .the same disadvantages existed for Si when it was intended that to replace germanium (Ge). Today few remember the initial processing problem of Si . The advantages already outweigh the disadvantages .As far as the power electronics is concerned, the future will be SiC.

1.2.References

[1] W. G. Pfann and J.H. Scaff, *Proceedings of the I.R.E.* **38**, 1151 (1950).

[2] L. B. Valdes, *Proceedings of the I.R.E.* **40**, 445 (1952).

[3] J. A., *Proceedings of the I.R.E*. **40**, 1314 (1952).

[4] Chrisrophe Lecuyer, *Making Silicon Valley: Innovation and the Growth of High Tech, 1930-1970* (The MIT Press, 2007).

[5] William C. ÓMara, Robert B. Herring, and Lee P. Hunt, *Handnook of Semiconductor and Silicon Technology* (Willam Andrew, 1990).

[6] B.E. Deal and A.S. Grove, J. Appl. Phys. **36**, 3770 (1965).

[7] N. F. Mott, S. Rigo, F. Rochet, A. M. Stoneham,*PHIL. Mag. B.* **60**, 189 (1989).

[8] K. Dah-Bin, M. P. James, N. D. William, C.S. Krishna, *IEEE Trans. Elec. Dev.* 35, 25 (1998).

[9] http://www.sia-online.org/news/2012/02/06/global-sales-report-2012

[10] http://www.icinsights.com

[11] http://www.electroiq.com/articles/sst/print/volume-54/issue-7.html

[12] http://www.power-mag.com/news.detail.php?NID=38

[13] B. J. Baliga, *Fundamentals of Power Semiconductor Devices,* (Springer, 2008).

[14] R. M. Warner, IEEE Trans. Elec. Dev. **48**, 2457 (2001).

[15] E.I.Carroll, power electronics for very high power applications,Power Engineering Journal,vol.13,issue 2,April 1999 ,pp.81-87.

[16] G.Majumdar,Future of power semiconductors,Proceeding of the 35th Annual IEEE PowerElectronics specialists Conference ,vol.1,20-25 June 2004,pp.10-15.

[17] http://www.semicon.toshiba.co.jp/eng/prd/pdf_presen/tr_IEGT_200502_e.p

2. Brief History of Silicon Carbide

Silicon carbide is one of the oldest compounds in the universe. Scientists believe that SiC was a celestial compound, which was formed around 4.6 billion years ago and migrated to the earth through meteorites. It is older than our solar system, and it has been floating around the Milky Way for billions of years as stardust that was generated in the atmospheres of carbon-rich red giant stars and grains have reached the earth on meteorites. And on the other side Silicon carbide (SiC) is naturally synthesized in the atmospheres of carbon rich red giant stars and by supernova remnants. No natural crystals can be found on Earth. It is almost nonexistent in the nature very seldom and it is one of the oldest compound semiconductors in the universe. Therefore SiC never attracted man's interest as other crystals like diamond did.J¨ons Jacob Berzelius, also known for his discovery of silicon, was most probably the first to synthesize SiC. The presence of SiC in other natural formations such as diamond pipes [1], or volcanic breccia [2], or in rock-forming material found as a beach pebble [3], has been described. Although it is scarce on Earth, SiC compound can be found in stardust grains predating the solar system. Molecular condensation of SiC particles is thought to be possible in the atmospheres of the carbon red giants [4]. And material ejected from supernova. Isotope analysis of the Murray. And the Murchison. Meteorites containing such SiC grains suggest their origin is closer to the center of the galaxy than the solar system. Silicon carbide is the only binary compound of silicon and carbon existing in the solid phase under normal condition. And it crystallizes in three Bravais lattices [5]:

- Close packed cubic (zinc blende structure)
- Hexagonal (wurtzite structure)
- Rhombohedral

However. In 1824, it was suggested for the first time that a chemical bonding could exist between silicon and carbon [6]. The first SiC crystals were grown already in 1891 by Acheson [7]. He melted a mass of carbon and aluminum silicate and found some small blue crystals, which he named Carborundum derived from the Corundum Al2O3, because he believed they consist of Al and C. Despite the fact that soon later [8] the crystals were identied to consist of silicon and carbon the name Carborundum has become

A synonym to SiC. In 1905, Moissan found natural SiC in meteorites. Because of this discovery, SiC is known to mineralogists as″moissanite ″ [9] .Fig. 2.1 shows the three

moissanite crystals. Also a small amount of SiC minerals from volcanic processes were found 50 years later [10].Historical interest in SiC has been centered on traditional ceramic-based applications. However, already in 1892 Nikola Tesla realized the first technical application of SiC [11]. Tesla developed a lamp containing carborundum, however, without knowledge of the chemical consistence of the material used.

Figure 2.1: *shows three moissanite crystals in nearly colorless till light yellowish*

In 1907, H. J. Round produced the first Light Emitting Diode (LED) based on SiC. He reported that "on applying a potential of 10 volts between two points on a crystal of carborundum, the crystal gave out a yellowish light" [12]**.** The evolution of SiC as an electronic material then took several decades. Already in 1929, See man concluded from the negative temperature coefficient of the electrical resistance that SiC is a semiconductor [13]. A more detailed study of the "electrical" luminescence of silicon carbide was made by Losev [14] in 1923–1940. He found that one of the types of emission was associated with the presence of a special "active layer" on the crystal surface. He showed later that this layer had electron conductivity and the bulk of the sample had hole conductivity. He also established the existence of a coupling between recitation and electrical luminescence. Thus, the two most important phenomena for semiconductor electronics, electro-luminescence and the rectifying properties of p–n structures were first observed in SiC crystals. SiC history is illustrated on a time line in Fig 2.2. In 1912, the occurrence of SiC in different crystal structures has been discovered [15]. And H. Baumhauer used the word "polytype" to describe the ability of SiC to crystallize into different forms varying only in their stacking order in one direction. This behavior of SiC was later called Polytypic (polytypism), i.e. polymorphism in one direction [16, 17]; it is one of the most interesting properties of SiC. Polytypism means the occurrence of different crystal structures in one material. The SiC polytypes can be described by different stacking of the Si–C double layers

perpendicular to the direction of the closed-packed plane, i.e., the cubic (1 1 1) or the hexagonal (0 0 0 1).

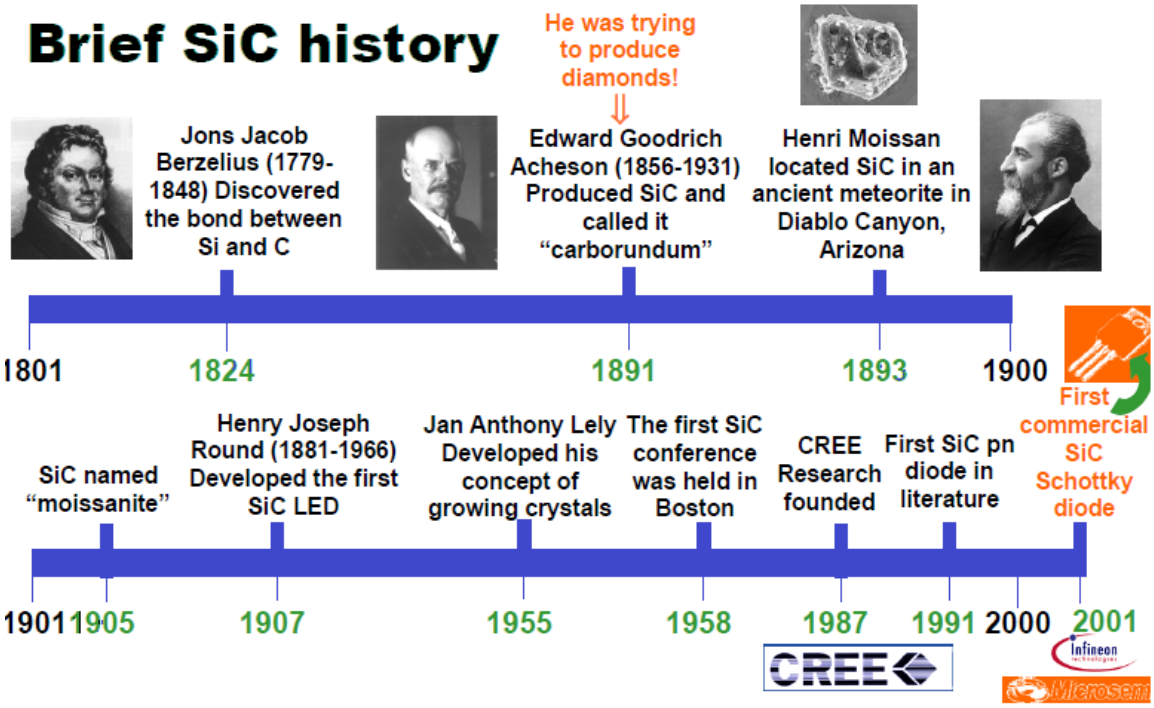


Figure 2.2: *SiC history timeline.*

More than 200 different SiC polytypes are mentioned, among them are only one cubic (C) and several hexagonal (H) and rhombohedral (R) structures. The cubic polytype 3C–SiC is called β-SiC, whereas the family of non-cubic polytypes refers to α -SiC. The ideal face-centered cubic or 3C-structure follows an ABCABC... stacking sequence, whereas the stacking sequence in the [0 0 0 1] direction for example of the hexagonal polytype 6H is ABCACB...., where A, B, and C represent the three possible positions of the Si–C double layers as shown in (Fig. 2.3). At this point it should be noted, that the term "polytype" was also used by Esaki. However with a different meaning. He used this term to characterize a new type of super lattices in which in addition to two host-semiconductors a third constituent is introduced, such as AlSb in the InAs–GaSb system. He pointed out that such triple-constituent system (type III electronic hetero structure) leads to a new concept of "man-made polytype" super lattices.

In this sense polytype means a combination of different types of electronic hetero structure, and should be therefore better named "heterotypic" structure. Such structures are also possible based on the combination of three different SiC polytypes, such as 3C/4H/6H–SiC (type III super lattice). But although the researches ceased at 1970. It

was maintained in the Soviet Union. The breakthrough was made in 1978.

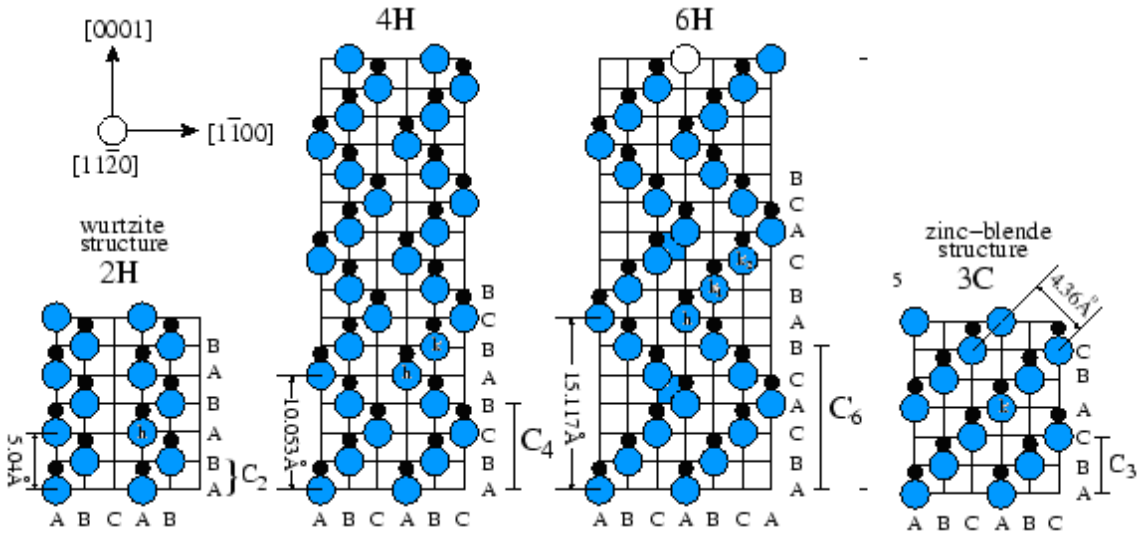


Figure.2.3: *Schematic models of the three most common, also commercially available, SiC polytypes. H and k denote the hexagonal and cubic sites in the lattice, respectively. Open and full circles stand for the silicon and carbon atoms, respectively.*

The modified Lely method was reported by Tairov and Tsvetkov. And also there is anther method which uses a seeded sublimation process and reduces the problems with yield and polytype control, the seeding sublimation technique is used to grow SiC boucles from which wafers are commercially produced today. In 1987 Cree Research Inc. was founded and it was the - structural quality and excellent doping control, however it suffers from low growth rates of about 3-5 μm/hour, thus growth of very thick layers is time consuming and creates a need for long-term process control. Due to the increased interest that SiC received, series of conferences was introduced, such as the International Conferences on Silicon Carbide and Related Material (ICSCRM) and the European Conferences on Silicon Carbide and Related Materials (ECSCRM). The rapid growth in SiC research is reflected in the number of contributions, which increased from 28 at the first ICSCRM conference held in Washington, D.C. in 1987 (by that time called as First International Conference on Amorphous and Crystalline Silicon Carbide and Related Materials) to 430 at the latest one in Lyon, France 2003, making this conference the largest meeting of its kind worldwide.

2.1. Silicon Carbide Technology

The second generation semiconductor, which has been used so far for high power applications, is Si. It is, however, is limited to low and medium voltage due to resulting high losses and heating. Also, the theoretical limits of the physical, electrical properties of Si have been reached it is limitations for temperature and power densities. And For a long time silicon-based power devices have dominated the power electronics and power system applications. As the needs and requirements for electric energy continuously grow nowadays, silicon (Si) devices are coming to face some fundamental limits in performance due to the inherent limitations of Si material properties, which make them uncompetitive for future demands, especially in high-voltage, high-efficiency, and high-power-density applications. This, together with the higher demand from the industry, has led to a more rapid development of SiC [Chinthavali, M.S, et al, 2005].

The properties of wide bandgap semiconductors silicon carbide make this material an ideal choice for device fabrication for applications in many different areas, e.g. light emitters, high temperature and high power electronics, high power microwave devices, micro-electromechanical system (MEMS) technology, and substrate. This semiconductor has been recognized for several decades as being suitable for these applications, but until recently the low material quality has not allowed the fabrication of high quality devices. Silicon carbide based electronic is at different stages of their development. An overview of the status of silicon carbide's application for high temperature electronics is presented. Silicon carbide electronics is advancing from the research stage to commercial production.

Silicon carbide (SiC)-based semiconductor electronic devices and circuits are presently being developed for use in high power operation, high-temperature, harsh environments, and high-radiation conditions under which conventional semiconductors cannot adequately perform.The silicon semiconductors switching devices are limitted only to medium and low voltages operations and for high voltage industrial operation systems we use electromechanical switches, magnetic contactor switches which are unpereferable because of it is shrortcomings represented in maintenance ,size,power losses ; thus silicon carbide semiconductors switching devices (MOSFET) will overcome these electrical and mechanical shrortcomings . And for the previous mentioned exceptional physical and electric properties that entitle it as potential material

which will overcome the limitation of silicon. And because of that SiC will receive special attention in the recent years for it is capability, suitability in electronics and offering the radical solution for the limitations of the previous Si devices drawbacks which was obstructing the technical evolutions so the recent development of power semiconductor devices has always been a driving force for power electronics systems. A wide variety of SiC power devices have been proposed ,including diodes ,BJT, GTO, MCT, MOSFET ,and IGBT, generally, these devices belong to categories – unipolar and bipolar or two – and three – terminal devices as shown as Fig.2.4 .

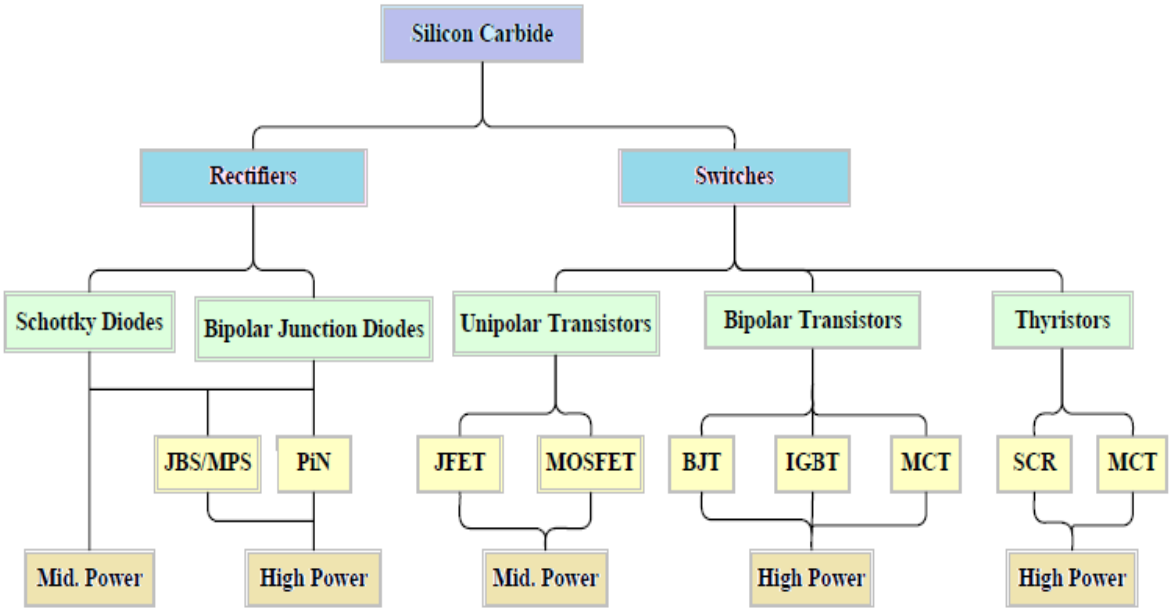


Figure. 2.4: *SiC power electronic components*

SiC technology has the potential to improve the current limitations of today's power electronics. Its ability to withstand days or weeks in a harsh environment, instead of a few hours as for Si, is something that can be useful, because it provides the ability to integrate power electronics directly.

It is expected to enable significant improvements to a far ranging variety of Power electronics applications in the field of power distribution, transmission systems. So at the consumer end, much of the electrical power under goes some form of electronic conversion, it is estimated to be 15 % of the electric power produced.

Table. 2.1: *Main advantages of SiC and related application fields.*

	SiC vs Si advantage	**Application**
Electrical properties	High electric field Wide band gap High carrier Saturation velocity	Power devices HT electronics ,sensors UV radiation detectors High frequency (RF devices)
Mechanical properties	Young modulus Hardness	Mechanical sensors Surface coating
Chemical properties	Intertness Biocompatibility	Chemical sensors(gas,HT) Bio-sensors
Thermal properties	High thermal conductivity	Power devices
Low power losses	High efficiency	Future:domestic automobiles ,motor drives

SiC material has been gaining a wide attention because of their anticipated large scale application in the near future. For the past few decades power electronics devices have enabled HVDC transmission, which mostly line commutated electronics. How ever improvisation has taken place recently. So it is predicted that with the future developments in silicon carbide semiconductors and their packaging technology, power electronic application will be extended into distribution application as device efficiency and reliability increases, Table. 2.1 show the main advantages of SiC and related application fields. The Performance gains from SiC electronics could enable the public power grid to provide increased consumer electricity demand without building additional generation plants and it has a potential to save a lot of money for the user when the efficiency is raised and switching losses are decreased. Increased switching speed, power density and reliability [Hornberger J. et al, 2004].

For example, high-power converters and motor drives able to operate in harsh environments are key components in the U.S. military project of developing hybrid-electric armed robotic vehicles. NASA is also interested in SiC power converters for spacecraft and satellite applications to increase the payload capability in lightweight solar arrays. These SiC power converters would increase the operational temperature

range while reducing the required but heavy and bulky heat exchangers. Energy companies and geological exploration instrumentation would also benefit from SiC improved motor drives and sensors' capabilities in deep earth drilling where hostile environments and extreme temperatures make the use of silicon electronics impossible. Another area where SiC superior properties are desirable is advanced turbine engines, propulsion systems, automotive and aerospace electronics, and applications requiring large radiation damage resistance. More efficient electric motor drives which will benefit industrial production systems as well as transportation systems such as diesel-electric railroad locomotives, electric mass-transit systems, nuclear-powered ships, and electric automobiles, SiC High-frequency power devices are being used in high-frequency power supplies, powerful microwave electronics for radar communications, Commercial communications industries such as air traffic control, weather radar stations and cell phone base stations, would also benefit from higher performance radio-frequency SiC devices. Fig.2.5 shows the step by step emergence of the SiC devices in different application: switch mode power supplies → industrial drives and motor control → traction →utility and megawatt application.

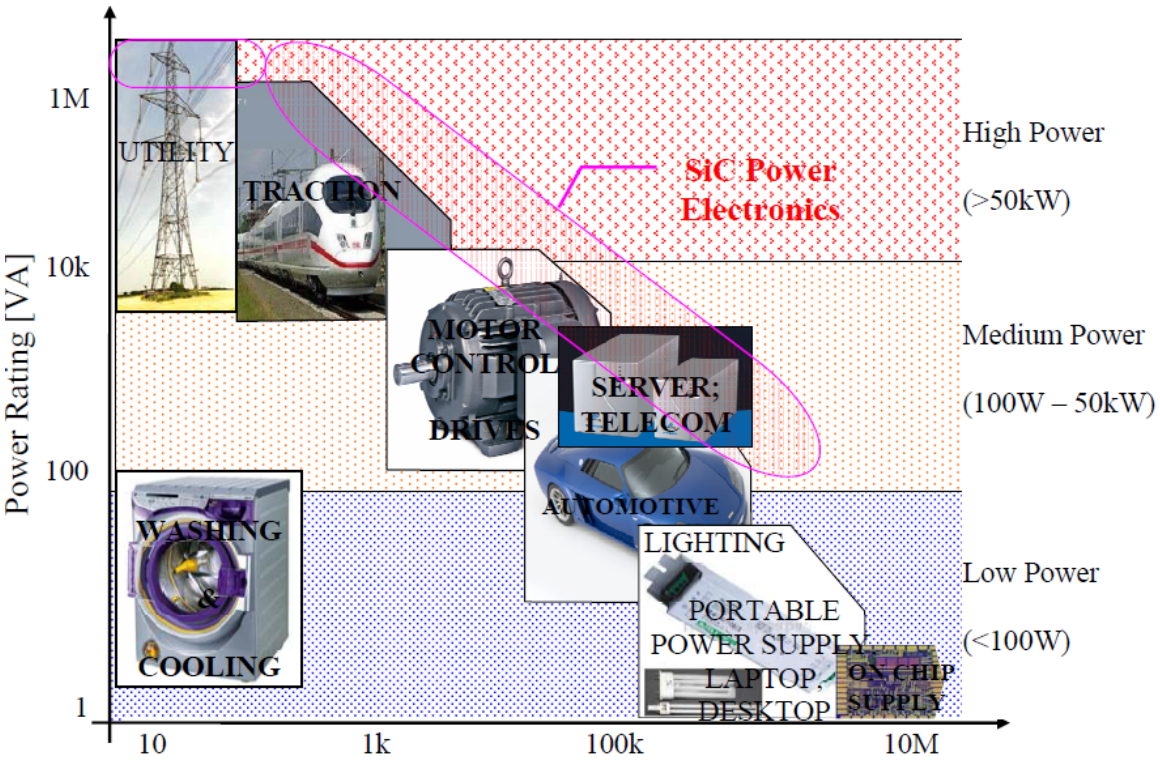


Figure. 2.5: *related voltage, current and frequency ranges for different power devices and their application range extension by means of SiC semiconductor.*

However, fast-switching capability coupled with high power density and high operating temperature make SiC high-frequency devices ideal for military aircraft requiring lightweight high-performance electronic radar systems. Integrated circuits are yet another field where SiC is expected to play a major role. Nowadays, for example, sensor and control electronics used in conjunction with jet or rocket engines must be removed from the target area, carefully shielded, protected and cooled. SiC devices would offer for instance the possibility to mount electronic controls directly on or into a jet engine, therefore increasing reliability and performance while reducing complexity, costs, and weight. Landing long-term, fully operational probes in hostile high-temperature environments is another attractive aspect for space exploration.

Apart from these cutting-edge niche markets, domestic applications would also benefit from SiC devices' ability to work in harsh, high-temperature environments. In the computer industry, thermal issues are the main by concerned when transferring technology from the desktop system to the laptop. With transistor junctions operating at 600 °C instead of 80 °C in the case of current commercial electronics, these issues would be greatly reduced. All the achievements in developing SiC technology in the case of military hybrid-electric combat vehicles could be directly applicable to domestic vehicles. And SiC devices would also allow sensor and control electronics to be mounted onboard directly on the engine block of automobiles without being shielded or kept away from the engine compartment because of thermal issues. All these possible applications rely on the superior physical properties of SiC.

2.2. Silicon Carbide Important Properties

2.2.1. SiC Material Properties (Crystal Structures, Polytypes)

SiC consists of both the Si and C atoms, which are group IV element materials. Each Si atom shares electrons with four C atoms, which means that each atom is bonded covalently to four neighbors, and vice versa. The basic structural unit is already shown in Fig.2.6 .The approximate bond length between Si and C atoms is 1.89 Å and the length between Si-Si and C-C atoms is 3.08 Å. SiC has a properties known as a polytypism. It means that the material can possess more than one crystal structure. Each crystal structure is called a polytype. There are also other polytypes, but the ones presented here are the two most interesting and the only structures that are used in semi conducting devices. The most common polytypes in commercially prepared crystals are

3C, 4H, 6H The two most widely used SiC polytypes have similar properties, but 4H-SiC has become more preferred since it does not exhibit the anisotropy of 6H-SiC. Therefore, 4H-SiC motilities are identical along two crystallographic planes of the semiconductor.

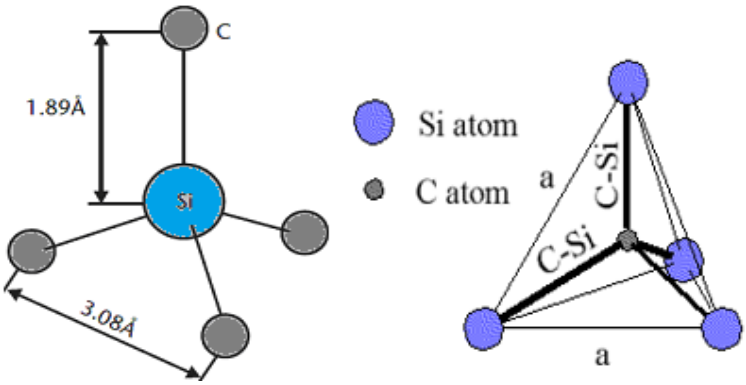


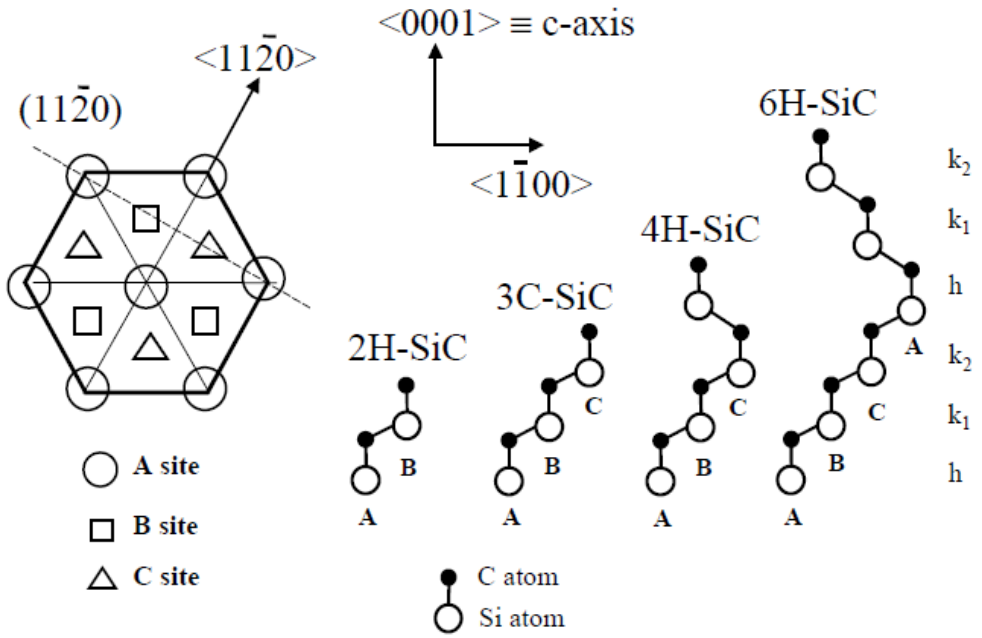
Figure.2.6:*the characteristic tetrahedron building block of all SiC crystals .four carbon atoms are covalently bonded with silicon atom in the center. Two types exist .one is rotated 180 around the c- axis with respect to the other, as shown.*

4H-SiC is preferred over 6H-SiC in most electronic applications, because it has more isotropic properties and a higher mobility. Even though the electrical properties are different, the mechanical and thermal properties are almost the same, independently of which polytype is being used [Ayalew T., 2004]. Silicon carbide occurs in many different crystal structures termed as “polytypes” and the phenomena is polytypism. The term polytypism is the special case of polymorphism. While polymorphism is the ability of an element or compound to crystallize in more than one crystal structure, one dimensional polymorphism is called polytypism. In case of silicon carbide, Si-C bilayer, as basic elements, arrange in different stacking sequences (Fig.2.7), (*Table.2.2)* giving rise to various polytypes without changing stoichiometry.

And the different polytypes are defined by the stacking sequence. For instance, 4H, and 6H is hexagonal structure and has an, ABAC, ABCACB stacking sequence, respectively. Similarly, 3C - SiC is cubic with ABC stacking sequence. And initially work was focused to on 3C- SiC material due to the superior transport properties.

How ever, the unavailable technology for growing 3C SiC bulk crystals and the poor material quality of the 3C SiC heteroepitaxially grown on Si hinders the advancement in 3C SiC devices. The availability and quality of reproducible single crystal wafers in 4H

and 6H SiC make these polytypes the most promising materials for electronic devices. 4H SiC's substantially higher carrier mobility compared to 6H SiC [18]. should make it the polytype of choice for the most SiC electronic devices.



(a) (b)

Figure.2.7: *the crystalline of SiC: (a) the three possible hexagonal positions (A, B, and C) for Si and C atoms and (b) the stacking sequences of four common SiC polytypes. The different cubic and hexagonal lattice sites are marked.*

Table.2.2: *notation and hexagonality of SiC polytypes with the corresponding numbers of in equivalent lattice sites*

Ramsdell notation	ABC notation	Jagodzinski notation	Hexagonality (%)	Number of inequivalent lattice sites
3C	ABC	k	0	1
2H	AB	h	100	1
4H	ABCB	hk	50	2
6H	ABCACB	hkk	33	3

Further more, the inherent mobility anisotropy that degrades conduction parallel to the crystallographic c-axis in 6H SiC [18, 19] will particularly favor 4H SiC for vertical power devices. The emergence of higher mobility 4H SiC has largely overshadowed significant progress made in obtaining greatly improved 3C SiC through hetroepitaxy on low –tilt- angle 6 H SiC substrate [20,21]. The higher mobility and more isotropic nature of 4H SiC properties compared to 6H SiC has made 4H SiC the poly type of choice

and much of the current device research activity.If the first double layer is called the A position, the next layer that can be placed according to a closed packed structure will be placed on the B position or on the C position. The different polytypes will be constructed by permutations of these three positions. … The number thus denotes the periodicity and the letter resulting structure which in this case is hexagonal. The 3C- SiC polytype is the only cubic polytype and it has a stacking sequence ABCABC …or ACBACB …A common crystalline defect is the so called Double Positioning Boundary(DPB), which is commonly seen in 3C-SiC grown on –axis 6H- SiC substrates. The defect arises when islands of the two possible stacking sequences ABCABC and ACBACB meet. When the stacking sequence is drawn in this manner a zig zag pattern is revealed. The surrounding lattice does not, however, look the same for each position. The A position has a different surrounding lattice than B and C positions. We call this position the hexagonal site, h. It is simply characterized as the turning point of the zig zag pattern. The other two positions (B and C) are called cubic, k1 and K2. An impurity replacing a host atom at one of the three sites will obtain a different binding energy depending on the site it replaces. A very illustrative example is the nitrogen donor in 6H-SiC. The hexagonal site gives rise to the P-level of the nitrogen donor with a binding energy of approximately 85 meV. The two cubic sites will give the R- and S-levels with binding energies around 138 meV and 142 meV, respectively. In the 4H-SiC polytype there are only two in-equivalent sites, one hexagonal and one cubic .The two levels of the nitrogen donor are in this case called P and Q. In 3C there is of course only one cubic site and in 2H there is only one hexagonal site. The 6H-SiC polytype can thus be characterized as being 33% hexagonal, whereas the 4H- and 2H-SiC polytypes are 50% and 100% hexagonal, respectively. So since the release of commercial 6H-SiC bulk substrates in 1991 and 4H-SiC substrates in 1994 The successive development of any material for semiconductor applications depends to a large degree on the capability of producing high quality single crystals of that material with controlled electronic properties. The development of SiC had for long been hindered by a lack of suitable crystal growth technology. Two significant factors in SiC’s crystal growth problems are its ability to grow in many different crystal structures, called polytypes and its inability to be melted at a reasonable pressure.

2.2.2 .Physical And Electrical Properties of SiC

SiC is wide band gap semiconductor with high thermal conductivity, high breakdown electric field strength, high saturated drift velocity, and high thermal stability. It exists in what are called polytypes. These polytypes are formed by stacking SiC molecules on the top of each other in certain order. More than 170 SiC polytypes are reported and each of them has different physical properties. The most commonly known polytypes are 3C-SiC, 6H-SiC, and 4H-SiC, but only the last two are commercially available. Since 1994, 4H-SiC has replaced 6H-SiC as the most commonly used SiC polytypes. The electrical properties of polytypes, such as band gap energy, electron mobility and critical field are modified by adding impurities and the impurities affect the electrical properties which give the priorities to SiC compared to Si Fig. 2.8: shows the difference between Si and SiC . Some important electrical properties are anisotropic, so they are a strong function of crystallographic direction of current flow and applied electric field.

The notation convention of the polytypes comes from their repeated stacking order and the shapes they form , 3C corresponds to three SiC molecules stacked in layers in three different position A,B, and C and the formed crystals has a cubic (C) shape . The same way 4 H as a stacking order of ABAC and the resulting shape is hexagonal (H). Finally, the stacking order of 6H-SIC is ABCACB repeating this also has a hexagonal shape. Some physical and electric characteristics of the SiC polytypes and some other competing semiconductors are given in Table: 2.3.

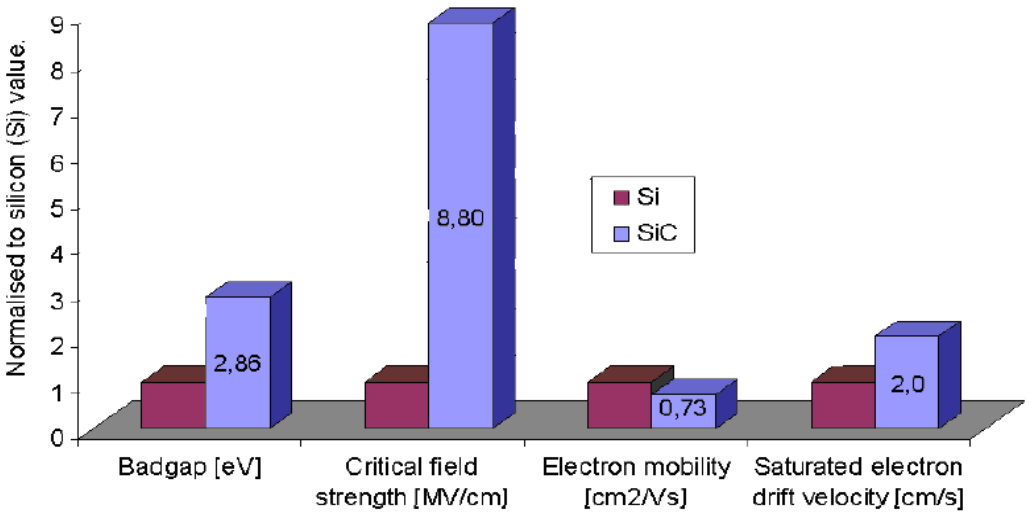


Figure.2.8: *Electrical properties of the SiC compared to the Si: value are normalized*

Table2.3: *physical and electrical properties of wide bandgap Semiconductors*

Property	Si	GaAs	4H-SiC	6H-SiC	2H-GaN	2H-AlN	Diamond
Bandgap at 300 K (eV)	1.11	1.43	3.26	3.02	3.39	6.2	5.45
Lattice parameters (Å)	5.43	5.65	a = 3.08 c = 10.08	a = 3.08 c = 15.12	a = 3.19 c = 5.18	a = 3.11 c = 4.98	3.56
Max. operating temp. (°C)	350	460	1200	1200			1100
Melting point (°C)	1410	1240	Sublimes > 2800	Sublimes > 2800		2275	Graphitization > 1500
Electron mobility (10^{-4} m^2/Vs)	1400	8500	900	600	900	1100	2200
Hole mobility (10^{-4} m^2/Vs)	600	400	40	40	150		1600
Breakdown electric filed (10^8 V/m)	0.3	0.4	2.2	2.5	3.3	11.8	10
Thermal cond. (W/m K)	150	54	490	490	130	200	2000
Saturation drift velocity (10^5 m/s)	1.0	2.0	2.7	2.0	2.9	1.8	2.7
Dielectric constant	11.8	12.8	10	9.7	8.9	8.5	5.5
Mohs hardness	7	4-5	9.2-9.3				10

2.2.2.1. Wide Band Gap

Table: 2.4: *widebande gap property of (4H-SiC, 6H-SiC, Si And Ga As)*

property	4H-SIC	6H-SIC	Si	GaAs
Bandgap (eV)	3.26	3.03	1.12	1.43

Some semiconductors are classified as a wide bandgap semiconductor because of their bandgap .Si has a bandgap of 1.12 eV and is not considered a wide bandgap semiconductor. The bandgap of SiC polytypes range from 2.39 eV for 3C-SiC to 3.33 eV for 2H-SiC; therefore, all SiC polytypes are classified as wide bandgap semiconductors. According to this fact, SiC offers a critical electric field of 2.0 × 106 V/cm – an order of magnitude higher than Si Fig.2.9 shows that. This increases the

blocking capability of SiC power devices and also allows them to be fabricated with much thinner and higher doped drift layers, significantly reducing the on-state resistance.

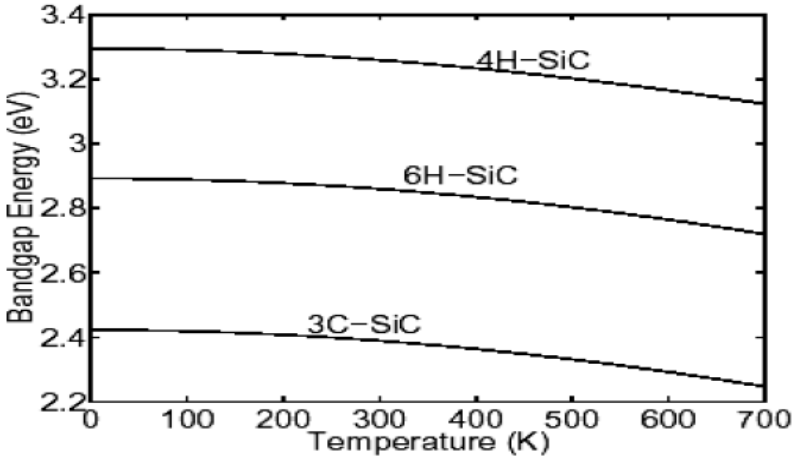


Figure.2.9 *bandgap variation with temperature ([22])*

Wide bandgap semiconductors have the advantage of high temperature operation and more radiation hardening. As the temperature increases, the thermal energy of the electrons in the valence band increases, so at certain temperature they have sufficient energy to leave the conduction band. This uncontrolled conduction needs to be avoided. The temperature at which this happens is around 150°C for Si. For SiC, the band gap energy is higher therefore, electrons in the valence band need more thermal energy to move to the conduction band this intrinsic temperature for SiC is around 900°C all previous reasons also true for radiation hardening, radiation energy can also excite an electron like the thermal energy and make it move to the conduction band. So we can summarize that wide bandgap, devices built from SiC can withstand more heat and radiation without losing their electric characteristics.

2.2.2.2. High Break down Electrical Field

SiC has a higher breakdown field than silicon because of the wide band-gap. The electron-hole pair generation due to ionization impact is difficult because of the wide band gap, and hence SiC can withstand higher electric fields compared to silicon. It's 8 times higher than Si .with this high electric breakdown field E_C (V/cm) ($1.5\text{-}4\times10^6$) much higher doping (N_D) (cm^{-3}) levels can be achieved ; thus ,the device layers can be made thinner than Si at the same break down voltage levels [23]. Fig.2.10.shows the

critical electric field as a function of drift region doping for Si and 4H-SiC material.

The blocking voltage V_{BR} of a (non- punch through) power MOSFET using ID analysis is then given as:

$$V_{BR} = \frac{\varepsilon_{sic} E_c^2}{2qN_D} \quad \textbf{(2.1)}$$

Where ε_{sic} is the dielectric constant of SiC (F/cm) ,and q is the charge (C) . V_{BR} varies as square of the E_C and is thus ($\varepsilon_{sic}E^2_{sic}/\ \varepsilon_{si}E^2_{si}$) 60 times higher than in similar Si power devices of the same doping N_D . For a given blocking voltage, SiC device can use a higher drift layer doping and thinner drift regions than that required for silicon devices. The specific on – resistance $R_{on,sp}$ consisting only the of drift layer resistance for (non- punch through) therefore less drift region resistance reducing the on-state losses ,design is given as :

$$R_{on,sp} = RA = \rho W_D = \frac{4V_{BR}^2}{\mu_{bulk}\varepsilon_{sic}E_c^3} \quad \textbf{(2.2)}$$

$R_{on,sp}$ varies as the square of the V_{BR} voltage and inversely proportional to the cube of E_C . Fig.2.11. shows a plot of $R_{on,\ sp}$ vs. V_{BR} for Si ,and just switching from Si to 4H-SiC material , $R_{on,sp}$ gets 200 times smaller than comparable Si devices .

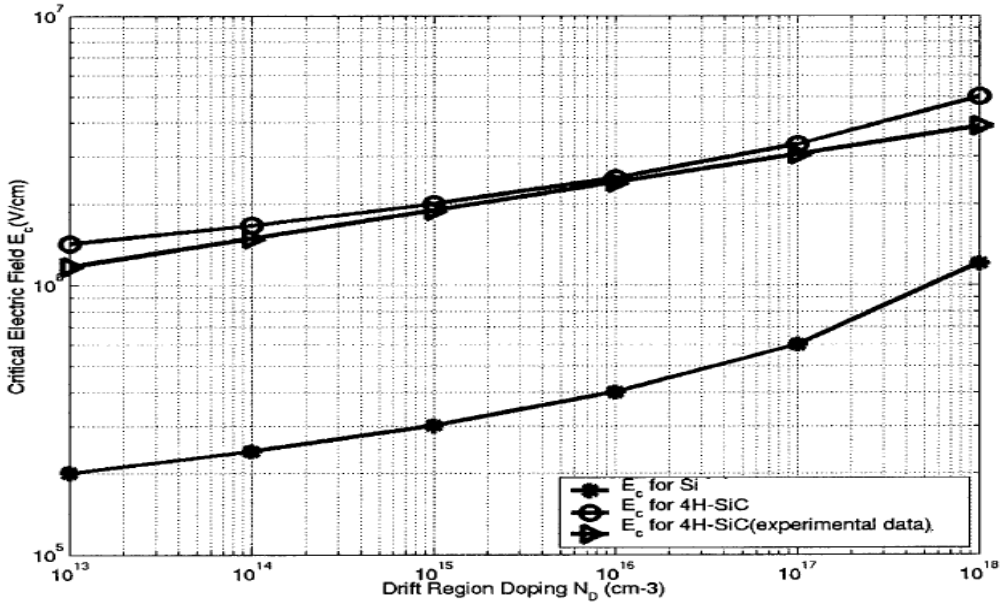


Figure. 2.10: *Variation of critical electric field as a function of drift region doping for Si and 4H-SiC material [24] & [25].*

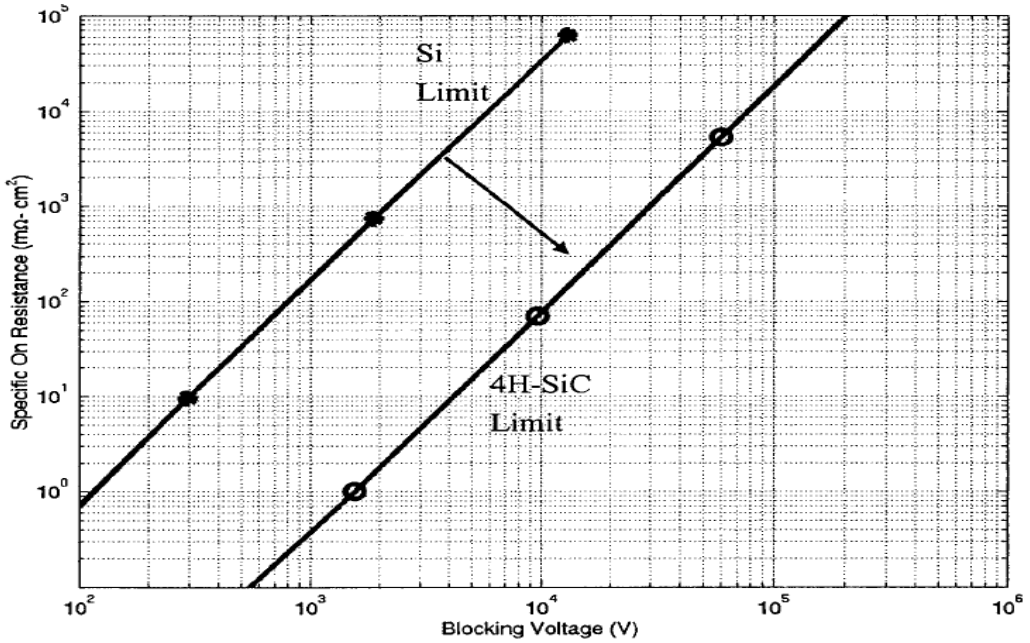


Figure. 2.11: *Specific on-resistance and blocking voltage of silicon and 4H-SiC power MOSFET structures with a "non-punch-through" design.*

Another useful performance measure for power MOSFETs isV^2_{BR} / $R_{on,sp}$ only depends on bulk mobility (μ_{bulk}) ,semiconductor dielectric constant (ε_{sic}) , and critical electric field (E_C) Thus, SiC power devices show higher breakdown voltage and lower power loss than Si devices.

2.2.2.3. High Saturated Drift Velocity

Table: 2.5: *high saturated drift velocity property of (4H-SiC, 6H-SiC, And Si)*

Property	**4H-SiC**	**6H-SiC**	**Si**
Saturated drift velocity (cm/sec) Vsat @ E= $2*10^5$ V/cm	$2*10^7$	$2*10^7$	$1*10^7$

Silicon carbide material has two times higher saturated drift velocity for electrons flowing in the direction perpendicular to the c – axis [26] compared to silicon at high fields. Thus SiC is a material used in high power microwave devices operating in the GHz range.

For high-frequency devices, the breakdown electric field strength is not as important as

the saturated drift velocity. A high-saturated drift velocity is advantageous in order to obtain as high channel currents as possible for microwave devices, and clearly SiC is an ideal material for high-gain solid-state devices. High frequency capability of semiconductor material is directly proportional to its drift velocity. The drift velocity of SiC polytypes (2×10^7) is twice the drift velocity of Si(1×10^7) ; therefore ,it is expected that SiC based power devices could be switched at higher frequencies than their silicon counterparts and there is decreasing in power losses during circuit switching .moreover , higher drift velocity allows charge in the depletion region of a diode to be removed faster ; therefore ,the recovery current of SiC diodes is smaller and the reverse recovery time is shorter .

2.2.2.4. High Thermal Conductivity

Silicon carbide based semiconductor devices can operate at high temperatures. 4H-SiC has a thermal conductivity , which is 2.5-3.3 times higher than Si,the thermal conductivity is (4.9W/cm-K) compared to silicon (1.5W/cm-K) , This feature enables easy transfer of heat generated in the device through the case and heat sink.

Table: 2.6: *high thermal conductivity property of (4H-SiC, 6H-SiC, And Si)*

Property	**4H-SIC**	**6H-SIC**	**Si**	**cu**
Thermal conductivity (W/cm°K)	3.3	3.3	1.5	3.97

The equation (2.3), junction – to – case thermal resistance, $R_{th\text{-}jc}$ of a 4H-SiC device is more three times lower.

$$R_{th\text{-}jc} = (d/\lambda A) \qquad \textbf{(2.3)}$$

Where λ: is the thermal conductivity,

A: is the cross sectional area.

d: is the length

Lower $R_{th\text{-}jc}$ means that heat generated in the SiC based device can more easily be transmitted to the case , heat sink ,and then to the ambient . The high thermal conductivity of SiC (4.9W/cm-K) enhances heat dissipation and, coupled **(1.3)** wide bandgap energy (3.3eV), allows high-temperature operation (above 300°C).

2.2.2.5. Carrier Mobility

The carrier mobilities μ_n and μ_p account for the scattering mechanisms in carrier transport. Carrier mobility depends on various factors like temperature, doping concentration, applied electric field, and the lattice structure. At low electric fields lattice scattering is the dominant factor. If the electron mobilities are compared, see table: 2.7.

Table 2.7: *carrier mobility property of (4H-SiC, 6H-SiC, And Si)*

Property	4H-SiC	6H-SiC	Si
Mobility $cm^2/Vsec$) μ_n bulk $\perp$	800	400	1400
μ_n bulk $\parallel$	900	100	1400

It is clear that the SiC has a disadvantage compared to Si. The lower mobility for SiC will Actually lower the switching frequency for SiC devices, but this is true only at low voltage .At higher voltage, the mobility is not dominating the property [Hornberger J.et al, 2004]. Owe field mobility models degradation of mobility due to ionized impurity scattering, phonon scattering, and carrier – carrier scattering .the field dependent mobility model further includes the degradation of mobility due to applied fields. To model mobility for electric field in the direction of current flow .

The lattice scattering (acoustic phonons) and ionized impurity scattering, together with piezoelectric scattering are the most relevant mechanisms which limit the mean free path of carriers at low electric fields in SiC. At low electric fields the electron velocity increases almost linearly with the field. A widely used empirical expression for the doping dependence of the low-field mobility is Caughey-Thomas low field mobility model [27].

$$\mu_o = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left(\frac{N_D + N_A}{N_{ref}}\right)^{\alpha}} \qquad \textbf{(2.4)}$$

Where (N_A+N_D) is the total doping concentration,(μ_{max}) and(μ_{min}) are the minimum and maximum mobilities of electrons and holes,(N_{ref}) is the doping concentration for p- type and n-type material calculated empirically and α is the curve fitting parameter, a measure of how quickly the mobility changes from µmin to µmax.

2.2.2.6. SiC Oxidation

SiC surface oxidation is one of the key issues for successful device applications. SiC has a great advantage that an oxide layer can be thermally grown by heating in an O_2 ambient exactly like for Si. This oxide layer is used as gate isolation material for MOSFETs, which is a most widely used semiconductor device in modern electronic industry. Moreover SiC MOSFETs would be applicable in extreme conditions where the conventional silicon devices can not work efficiently.

Similar to the Si technology, the oxide layer on SiC can be obtained in different ways such as thermal oxidation [28, 29, and 30] and CVD [31, 32]. SiC surfaces can be thermally oxidized using dry and wet oxygen at around 1000˚C in the same way as for Si. The oxidation of SiC has been studied by many anthers [29, 33, and 34]. It has been found that the oxidation rate of all SiC polytypes is much lower than that of Si. It normally takes a much longer time to get the same thickness on SiC than on Si under the same oxidation conditions. Another unique characteristic in the oxidation process of SiC is that the oxidation rates are different between the silicon face and the carbon face i.e. the oxidation rates depend on the crystal orientation of SiC, thus SiC shows an anisotropic oxidation [35].

Fabrication of efficient and reliable SiC-MOSFETs requires abrupt homogeneous SiO_2/SiC interface with low interface states density comparable to that of SiO_2/silicon interface. Several groups have reported the fabrication of MOSFETs in three main polytypes 4H, 6H and 3C-SiC [36, 37]. However, the channel mobility is extremely small compared to its bulk value which hinders the realization of power MOSFETs in SiC. The low channel mobility is largely related to the presence of greatly enhanced density of imperfections at the SiO_2/SiC interface [38, 39] which not only degrade the device performance but also cause reliability problems related to the anticipated extreme operating conditions [40].

SiC is the only compound semiconductor which can be thermally oxidized to grow high quality $Si0_2$ much like the Si/SiO_2 interface. To build high performance MOS devices

in SiC, the SiO_2/Si interface needs to be improved. For years, the progress has been hampered by problems with the gate oxide, reflecting in very poor channel-carrier mobility and oxide reliability. A lot of research efforts have been poured into the improvement of quality SiO_2/Si interface in SiC.

2.3. Silicon Carbide Advantages for Power Electronic Devices

There are many devices ,4H-SiC and 6H-SIC PiN diodes ,Schottky diodes ,IGBTs ,thyristors ,BJTs, various MOSFETs, GTOs, MCTs, MTOs, in kV range [41] with reduced on resistances . There are basically two families of two and three terminal power semiconductor switching devices the schottky rectifier and the power FET representing the unipolar family and BJT and thyristor belonging to the bipolar family. The majority carrier devices (or unipolar devices) such as MOSFETs, MESFETs, JFETs, and Schottky diodes are faster than minority carrier devices (or bipolar) such as PiN diodes, BJTs, IGBTs and SCRs. The controlled unipolar devices have negligible switching losses and some of the power devices can be discussed in the following subsection.

Table: 2.8. *Advantage and application scope of SiC devices*

Device Characteristics	**System Benefits**	**Application Scope**
High breakdown voltage	Large power capacity	Military :combat vehicles , Weapons, electric ships
High current density	High reliability, compactness	Aerospace: spacecraft and Satellite application
High operational temperature	Less cooling requirements	Energy: power transmission and distribution
High switching frequency	Reduced passive components	Industry: deep earth drilling for energy exploring
Low power losses	High efficiency	Future: domestic automobiles ,motor drives

2.3.1. High Voltage Operation

Using Si bipolar devices at the voltage higher than a certain value (300V) it's more cost effective because of their higher current densities than unipolar devices. This voltage value is ten times [42] higher in SiC devices (3kV) than Si devices. Thus SiC unipolar devices are expected to replace Si bipolar devices in the 300- 3000V range power applications; however, over 3kV, bipolar devices regain the control. In this voltage range, SiC bipolar devices still have an edge over their Si counterparts.

There are several different bipolar, unipolar, controlled, uncontrolled are used for power electronics and power system designers but; metal- oxide- semiconductor (MOS) – gate devices are widely used than others. IGBTs offer low switching losses, high switching frequency operation and a simplified gate circuit. GTOs and thyristors, on the other hand, are still used for high power applications, such as power systems conditioning equipment and large direct current (dc) rectifiers. Low switching losses of power MOSFETs make them perfect for high frequency application. The need for faster devices with high voltage and high switching frequency capability is growing, especially for advanced power conversion.

Silicon based power devices have long dominated the power electronics and power system applications. The primary limitation of the silicon is the small energy band gap, which leads to low intrinsic breakdown voltage. In order to overcome this limitation, the active layers were made thick to have greater voltage drop across the device and stacking packaged devices in series was adopted. However, series stacking is expensive from a packaging standpoint and requires complicated control. Hence, there is strong intention to develop high voltage blocking capability semiconductor device particularly from wide band gap semiconductor like SiC. Owing to the wide band gap, silicon carbide can block high voltage with increased doping and thinner drift region. Silicon devices are limited to 5000V [43], and silicon carbide devices can block the voltages up to 19.2 kV.

Higher breakdown voltage is another consequence of wide band-gap material and leads directly to much higher-voltage devices. The prospect of single devices that can withstand 5,000 to 40,000 V is very appealing in high power systems. Currently, achieving medium voltage in silicon IGBTs requires multilevel converters, or the stacking or cascading of multiple inverter modules. A simple 6-device inverter that operates with high switching frequency at 4,160 VAC (requires a 10,000 V device)

would make a serious impact on size, cost, and reliability. Theoretically, the resistance of the blocking layer in a power semiconductor increases as the voltage blocking capability is increased. In fact, for most devices, the resistance increases with the square of the voltage. However, this is quite misleading in predicting the practical result. The conduction loss is proportional to the square of current, which decreases inversely with the increase in voltage. The conduction loss determined by this simple analysis would thus remain the same. However, the device has regions other than the blocking layer where the resistance does not increase commensurately with the voltage. The practical outcome of increasing voltage is usually quite favorable. One of the major negative implications of targeting SiC at higher voltages is longer development time.

2.3.2. High Temperature Operation

Silicon carbide has the inherent ability to operate at higher temperatures compared to other material devices and exhibits similar electric characteristics as at room temperature. Silicon carbide has higher thermal conductivity and low intrinsic carrier concentration ,which enables them to operate at high junction temperatures , The maximum junction temperature that silicon operates is 150°C whereas; Silicon carbide can operate at 650°C [44] .However ,packaging and high temperature contacts are a problem for SiC devices . Two important facts about higher operating temperature are (1) the higher temperature will result in smaller heat – sink area of the same packaging technology, (2) high operating temperature allows a complete change in the thermal management approach for a given packaging area. So SiC power devices can operate at higher temperature. SiC MOSFETs have been operated to function at as high as 650°C [45]. Moreover, SiC MOSFETs were reported to work at 450°C and thyristor (700V, 6A) at 350°C [46]. This is quite an improvement compared with 150°C operation temperature for Si power devices .The high temperature SiC power devices are still in experimental stage for higher temperatures. SiC Schottky diode has a rated operating temperature of 175°C [47]. High temperature electronics are increasing markedly in importance. The demands for high power electronics is increasing day by day. Where high temperature operation is necessary, SiC devices might be the only acceptable option for high power levels because they (not SiC MOSFETs) can operate at over 400°C. This capability is a direct result of being a wide band-gap material. As

temperature is increased, a number of physical processes increase in intensity to interfere with the operation of a device, as intended by the designer. Fig 2.12.shows high power and high temperature device.

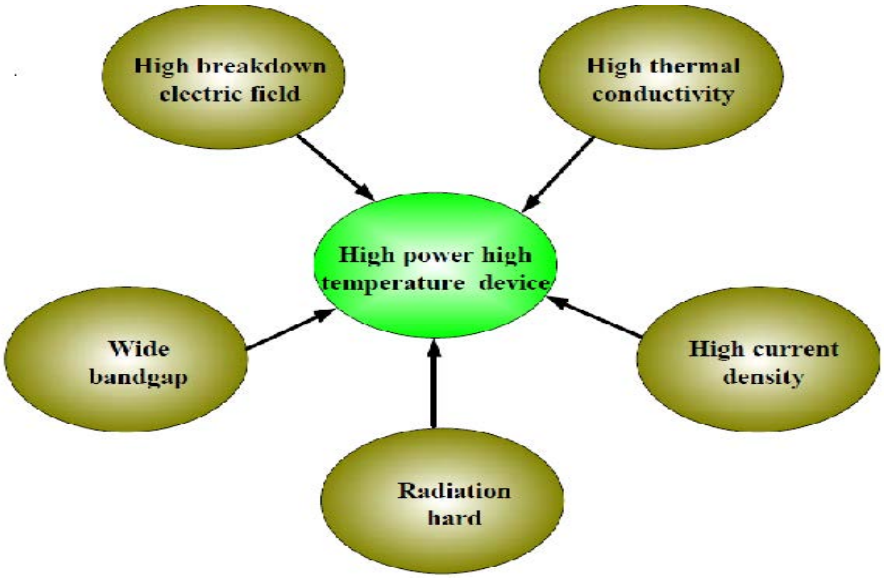


Fig 2.12.*high power and high temperature device*

These include an increase in intrinsic carriers, increase in thermionic leakage of devices, and decrease in carrier mobility. A wide band-gap causes these processes to be less intense at any given temperature, so higher temperatures will be necessary for unacceptable levels of intensity to be reached. Currently, the primary applications driving high temperature electronics development include vehicles, space and aviation, and deep well drilling.

2.3.3. High Frequency Operation

Because silicon carbide devices have higher saturation velocity and reduced drift region widths SiC has low switching losses compared to Si and hence is suitable for high frequency operation .Increase in the device speed results in many system benefits , one of which is a reduction in volume and weight associated with passive components , which can be simply achieved by increasing the frequency , the turn- of time in SiC devices is less than in Si devices because of the fact that SiC devices can block faster which is reduced the turn – of time which leads to increase the frequency operation.

as a result of the previous properties , SiC power devices can operate at high frequencies . the switching frequency of Si power devices is usually limited to less than

20 kHz for power levels of more than a few tens of kilowatts , The switching frequencies of over 100kHz are possible for SiC power devices. Higher switching speeds are achieved with SiC for two reasons: (1) the higher speed, lower loss, switching properties of SiC devices, and (2) the ability to use faster switching types of devices at higher voltages. Silicon MOSFETs have excellent switching characteristics but are limited to lower voltages and currents. With SiC, the MOSFET might be designed for operation up to 10,000 V, making its superior switching characteristics available at industrial voltages for the first time. Whether the improved switching speed is financially beneficial, depends on the application. For example, in a typical two-quadrant drive, which comprises well over 90% of the drive market, there is no supplemental filter whose size would be reduced by higher switching frequency.

The only filtering is provided by the inductance of the motor. The inductance is determined entirely by the motor requirements and that inductance generally is adequate for current smoothing with the switching speeds now found in drives. Without the need for higher speed switching, the designer would have to look elsewhere for a reason to use SiC devices rather than the standard silicon IGBTs.

2.3.4. Optoelectronic Device Operation

The wide bandgap of SiC is useful for realizing short wavelength blue and ultraviolet (UV) optoelectronics. SiC-based blue pn-junction light emitting diodes LEDs were the first Silicon carbide based devices to reach high volume commercial sales .These epitaxially – grown dry-etch mesa isolated pn- junction diodes were the first mass – produced LEDs to cover the blue ($\sim$250 to 280 nm peak wavelength) portion of the visible full – color LED-based displays [48].

While both blue and green SiC LEDs have been developed to the point of commercial viability with the blue being a relatively successful product, the brightness and efficiency of these devices is far below that of the III- nitride based blue green LEDs developed in the past few years. As a result, the future of emitters which use SiC as the active structure appears to be quite limited however SiC is an excellent substrate for heteroeptaxial growth of III- nitrides structures grown on SiC. As such, SiC will continue to play a major role in future super – bright visible emitters and UV detectors.

2.3.5. High Reliability

Some papers reported that the static and dynamic characteristic of SiC devices do not change much with the temperature. Some reliability studies of SiC PiN diodes are done in [49,50].they show that in the long – term ,SiC PiN show excellent reverse voltage characteristics. The forward voltage drop , increase in time.

No comparison with Si PiN diodes is given. The reverse recovery waveform of a 1500V 0.5A rated silicon diode is shown at different temperatures. the peak reverse current of the SiC diode stays at 0.4A while that of the 1000V 1A rated Si PiN diodes increase from 1.5Ato 2.7A as the temperature changes from 25°C to 225°C . Furthermore, the reverse recovery time of the SiC diode stays at 20ns while that of the Si diode increases from 50 ns to 100 ns. Similar results given in [51].

2.4 - Defects in Silicon Carbide

Silicon carbide often contains several crystal defects, where as the most harming is the "micropipe" defect. Caused by several screw dislocations bunching together to form a giant screw dislocation and making it energetically favorable to open up a hollow core in the center [52]. It prevents the increase of defect – free wafer diameter, which directly affects the SiC electronics capability.

1- Micropipes : are basically a hollow core penetrating the entire wafer along the *c*-axis direction (a cave diameter at the order of micrometers) in the SiC wafer that extends roughly parallel to the crystallographic c-axis [53]. as shown in Fig. 2.13.

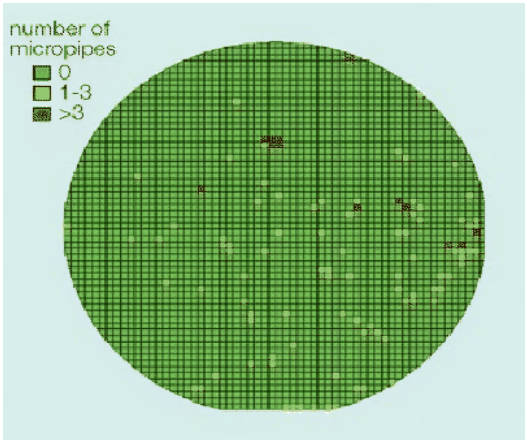


Figure:2.13. *A map of micropipe defect count on a 3 inch semi-insulating 4H-SiC substrate . showing an average micropipe density of only 3/cm* ^{2} *and 96% of the area to be micropipe-free.*

SiC wafer also contain high density of closed core defects ,which like miccropipes cause a localized strain and SiC lattice deformation [53],[54]. These defects are particularly disturbing for large-area devices such as high-power devices. In addition to micropipe defects, there are also non-hollow core (elementary) screw dislocation defects in the SiC wafers and epilayers. A different way of forming micropipes may be simply by system contamination, where particles are trapped in the growing crystal, thus forming a micropipe, as described by Augustine et al. [58]. These defects are not considered to be fatal as micropipes ,recent experiments have shown that they degrade and leakage and breakdown characteristics of P-N junctions:[55],[56] and [57].considering permanent and consequent increase of device chip area .

2 - Stacking Faults

The second defect that needs to be discussed does not have as grand a history as micropipes because it only recently became popular. This defect is the stacking fault, which creates degradation of bipolar devices. Reports by Lendenmann [59] and Bergman [60] reveal that a PiN diode operating under normal conditions begins to degrade. While the diode is operating, defects, which the authors interpret as stacking faults, evolve with an accompanying reduction in carrier lifetime. The defects thus act as recombination centers for the carriers.

Furthermore, the stacking order has been identified as that of the 3C-SiC polytype and, according to the study by Saltbush, an explanation to the recombinative behavior of the stacking fault is that the 3C-SiC, having a lower bandgap than 4HSiC, acts as a quantum well, thereby enhancing the recombination [61]. It is a very serious materials issue that must be solved prior to the realization of commercial bipolar devices. Work is ongoing to reduce defects in SiC material. One of the more interesting concepts is the reduction of defects through epitaxial growth on porous SiC substrates [62]. This approach has clearly demonstrated a reduction in intrinsic defects, as evidenced by photoluminescence measurements. It is too early to tell whether this technique can provide a path forward for the bipolar devices but it will clearly find its applicability in several areas where SiC will have a market.

2.5. References

[1] A. P. Bobrievich, V. A. Kalyzhnyi, and G. I. Smirnov, Proc. Acad. Sci. USSR, Sect.Geol. Sci **115** 757-760 (1957).

[2] J. Bauer, J. Fiala, and R. Hrichova, *Natural α-SiC,* Am. Mineralogist **48** 620-634(1963).

[3] S. Di Pierro, E. Gnos, B. H. Grobety, T. Armbruster, S. M. Bernasconi, and P.Ulmer, American Mineralogist, Vol. 88, Nos. 11–12, 2003, pp. 1817–1821.

[4] Friedemann Chr. *Physica* **41**, 139-143 (1969)

[5] E.Arnold and D.Alok, Effect of interface states on electron transport in 4H-SiC inversion layers "IEEE Trans.Elect.Dev.48.1870,(2001).

[6] J.J. Berzelius, Zersetzung der Eussspatsauren Kieselerde durch Kalium, Ann. Phys. Chem. 1 (1824) 169, 208.

[7] E.G. Acheson, On carborundum, Chem. News 68 (1893) 179.

[8] E.G. Acheson, Production of arti cial crystalline carbonaceous materials, US Patent No. 492,767 (28.2.1893).

[9] http:// www.ifm.liu.se/matephys/AAnew/research/sicpart/sicindex.html

[10] A.J. Regis, L.B. Sand, Natural cubic silicon carbide, Geol. Soc. Am. Bull. 69 (1958) 1633.

[11] T.C. Martin, Nikola Tesla's Untersuchungen Xuber MehrphasenstrXome hXoherer Spannung und Frequenz [German translation of collected lectures by H. Maser], (Halle/Saale, 1895), pp. 136, 255.

[12] H. J. Round, Electr. World 19, 309 (1907).

[13] H.J. Seemann, Phys. Z. 30 (1929) 1929.

[14] O.V. Losev, Detailed study of radiation recombination in silicon carbide (SiC), (in Russian) Telegra a i Telefonia 18 (1923) p.61; (see also H. Gernsback, A sensational radio invention, Radio News (1924) p.291, p. 294, p. 431); Luminous Carborundum detector and detection e1ect and oscillations with crystals, Philos. Mag. 6 (1928) p.1024; About the photoelectric e1ect in the active layer of carborundum crystals, (in Russian) Zh. Tekh. Fiz. 1 (1931) 718.

[15] H. Baumhauer, UX ber die krystalle des Carborundums, Z. Kristallogr. 50 (1912) 33.

[16] H. Baumhauer, UX ber die verschiedenen Modi kationen des Carborundums und die Erscheinung der Polytypie, Z. Kristallogr. 55 (1915/20) 249.

[17] C.J. Schneer, Polymorphism in one dimension, Acta Cryst. 8 (1955) 279.

[18] W. J. Schaffer, G. H. Negley, K. G. Irvine, and J. W. Palmour, conductivity anisotrophy in epitaxial 6H and 4H SiC・, Mat. Res. Soc. Symp. Proc., vol. 339, Diamond, SiC, and Nitride Wide-Bandgap Semiconductors, C. H. Carter, Jr., G. Gildenblatt, and S. Nakamura, Eds. Pittsburgh, PA: Materials Research Society, p. 595, 1994.

[19] G. A. Lomakina, electrical properties of various polytypes of silicon carbide・, in Silicon *Carbide-1973, R. C. Marshall, J. W. Faust, Jr., and C. E. Ryan, Eds. Columbia, SC: University of South Carolina Press, p. 520, 1973.*

[20] P. G. Neudeck, D. J. Larkin, J. E. Starr, J. A. Powell, C. S. Salupo, and L. G. Matus, electrical properties of epitaxial 3C- and 6H-SiC p-n junction diodes produced side-by-side on 6H-SiC wafers・, IEEE Trans. Elect. Dev., vol. 41, p. 826, 1994.

[21] P. G. Neudeck, D. J. Larkin, J. E. Starr, J. A. Powell, C. S. Salupo, and L. G. Matus, greatly improved 3C-SiC p-n junction diodes grown by chemical vapor deposition・*IEEE Elect. Dev. Lett., vol 14, p. 136, 1993.*

[22] J.B. Fedison,"High Voltage Silicon Carbide Junction Rectifiers and GTO Thyristors, "Thesis Submitted to RPI New York,May 2001

[23] T. Funaki, T. Kimoto, and T. Hikihara, "Evaluation of capacitance-voltage characteristics for high voltage SiC-JFET," in *IEICE Electron. Express*, vol. 4, no. 16, 2007, pp. 517-523.

[24] A. O. Konstantinov, Q. Wahab, N. Nordell and U. Lindefelt, "lonization rates and critical fields in 4H silicon carbide," Applied Phys. Lett., Vol. 71, No.l, pp.90-92,July, 1997.

[25] J. W. Palmour, S. T. Allen, R. Singh, L. A. Lipkin and D. G. Waltz, "4H-silicon carbide power switching devices," Silicon Carbide and Related Materials 1995,Proceedings of the sixth Int'l Conf lOP Publishing, pp.813-816, Bristol, UK.

[26] I. A. Khan and J. A. Cooper, Jr., "High Field Electron Transport in Silicon Carbide,"
Materials Science Forum, Vol.264-268, pp509-512, 1998.

[27] M.Roschke,Frank Schwierz,"Electron Mobility Models For 4H,6H,3C SiC" IEEE Transactions on Devices letters,vol.48,No.7,pp.1442-1447,july 2001.

[28] W. V. Muench and I. Pfaffeneder, thermal oxidation and electrolytic etching of silicon carbide・, J. Electrochem. Soc., vol. 122, p. 642, 1975.

[29] A Suzuki, H. Matsunami, and T. Tanaka, auger electron spectroscopy analysis of thermal oxide layers of silicon carbide・, J. Electrochem. Soc., vol. 125, p. 1896, 1978.

[30] A. Suzuki, H. Ashida, N. Furui, K. Mameno, and H. Matsunami, thermal oxidation of SiC and electrical properties of Al-SiO2-SiC MOS structure・, Jpn. J. Appl. Phys., vol. 21, p. 579, 1982.

[31] A. Golz, R. Janssen, E. Stein von Kamienski, and H. Kurz, ・ Characterization of oxides on silicon carbide deposited by remote plasma enhanced chemical vapor deposition・*The Physics and Chemistry of SiO2 and the Si-SiO2 Interface – 3, H. Z. Massoud, E. H. Poindexter, and C. R. Helms, Eds. Pennington, NJ, USA: The Electrochem. Society, p. 753, (1996).*

[32] S. Sridevan, V. Misra, P. K. McLarty, B. J. Baliga, and J. J. Wortman, rapid thermal chemical vapor deposited oxides on N-type 6H-silicon carbide・, IEEE Elect. Dev. Lett., vol. 16, p. 524, 1995.

[33] L. Muehlhoff, M. J. Bozack, W. J. Choke, and J. T. Yates, Jr., comparative oxidation studies of SiC (0001) and SiC (0001) surfaces・, J. Appl. Phys., vol. 60, p. 2558, 1986.

[34] C. D. Fung and J. J. Kopanski, thermal oxidation of 3C silicon carbide single crystal layers on silicon・, Appl. Phys. Lett., vol. 45, p. 757, 1984.

[35] K. Christian and R. Helbig, anisotropic oxidation of 6H-SiC・, J. Appl. Phys., vol. 79, p. 3276, 1996.

[36]. Spitz J, M. R. Melloch, J. A. Cooper Jr., M. A. Capano, “2.6kV 4H-SiC lateral DMOSFETs”,*IEEE Electron Device Letters 19(4) (1998) 100*

[37]. Materials Research Society Symposium Proceedings 54 (1986) p561, 97 (1987) p2597, 116(1988) p357

[38]. Afanas’ev V.V., M. Bassler, G. Pensl, M. Schulz “Intrinsic SiC/SiO2 Interface States”,*Physica Status Solidi A 162 (2001) 321-337*

[39]. Afanas’ev V.V., “Electronic properties of SiO2/SiC interfaces”, *Microelectronics Engineering48 (1999) p241*

[40]. Mathur, M.M., J.A. Cooper Jr., “Time-dependent-dielectric-breakdown measurements of thermal oxides on n-type 6H-SiC”, *IEEE Transactions on Electron Devices ED 46 (2000)p520*

[41] http:// www.ecn.purdue.edu/WBG/Data_ Bank/Best_Performance.html

[42] J.W.Palmour,R.singh,R.C.Glass,O.Kordina,and C.H.Carter ,Jr., “Silicon Carbide Power Devices,” Proceeding of the IEEE International symposium on Power Semiconductor Devices ICs,pp.25-32,1997.

[43] http://www.ecn.purd.edu/WBG/Data_Bank/Best_Performance.html

[44] M.Shanbag T.P.Chow, M.S.Adler, “Reliability testing of SiC high voltage power devices ,”Proceedings of Center for Power ElectronicSystems (CPES) Annual Seminar,pp,487-490,2001.

[45] N.S.Rebello and F.S.Shoucair ,”6H silicon carbide MOSFET modeling for high temperature analogue integrated circuits (25-500˚C),”IEE Proceeding – Circuits Devices systems ,vol.143,no.2,pp.155,April 1996.

[46] WWondrak,R,Held,E. Niemann,and U.Schmid,”SiC devices for advanced power and high temperature application ,”IEEE Transaction on Industrial Electronics,vol.48,no.2,pp.307-308,April2001.

[47] http://www.infineon.com

[48]J. Edmond, H. Kong, A. Suvorov, D. Waltz, and C. H. Carter, Jr., "6H-Silicon Carbide Light Emitting Diodes and UV Photodiodes," *Phys. stat. sol. (a)*, vol. 162, no. 1, pp. 481-491, 1997.

[49] H.Lendenmann, F.Dahlquist, N.Johansson,P.Bergman,H.Bleichner, and C.Overn,”Performance and reliability of high power SiC diodes ,” Future Electron Device,vol.11,no.2,pp.113-118.

[50] M.Shanbhag,T.P.Chow,and M.S.Adler,”Reliability testing of high power SiC high voltage power devices , “Proceedings of center for Power Electronic Systems (CPES) Annual seminar,pp.487-490,2001.

[51] A.R.Hefner,R .Singh,J.S.Lai,D.W.Berning,S.Bouche,and C.Chapuy,”SiC Power diodes provide breakthrough performance for a wide range of application , IEEE,vol.16,no.2,pp.273-280,March 2001.

[52] Chen M,Xu D.,Matsui M.,”study on Magnetizing Inductance of High frequency Transformer in the Two Transistor Forward Converter”,Power Conversion Conference ,2002,pages:597-602.

[53] Heindl J.,Strunk Heydemann P and Pensl G., “Micropipes:Hollow Tubes in silicon carbide “,Physica Status solidi,1997,pages :162- 251.

[54] Si W., and Dudley M., “study of hollow-core screw dislocation in 6H-SiC and 4H-SiC single crystals”, silicon carbide , III-Nitrides, and Related Materials,science forum 1998,pages :264-268,Switzerland.

[55] Neudeck P.,Huang W.,Dudley M., and Fazi C ., “Non-Micropipe Dislocations in 4H- SiC Devices : Electrical Properties and Device Technology Implication “,wide-Bande –gap semiconductors for high power, high frequency and high temperature ,materials research society ,1998,warrandale,USA

[56] Sugawara Y., “recent progress in SiC power device developments and application “ power semiconductor devices and ICs ISPSD ,2003,pages:10-18

[57] Ohashi H., “Possibility of Power Electronics Paradigm shift with wide band gap semiconductors “, Tokyo institute of technology,material science forum,2004 vols. 457-460,pages :21-26

[58] Ohashi H,”the progress in SiC technology in japan “, AIST Power electronics research centre “, EPEO5 SiC workshop,2005,Dresden

[59] Lendenmann, H., et al., *Proceedings of the Ultra-Low-Loss Power Device Technology Workshop*, 2000, pp. 125–130.

[60] Bergman, J. P., et al., *Mat. Sci. Forum*, Vols. 353–356, 2001, pp. 299–302.

[61] Stahlbush, R. E., et al., *Mat. Sci. Forum*, Vols. 389–393, 2002, pp. 427–430.

[62] Saddow, S. E., et al., *Sci. Forum*, Vols. 353–356, 2001, pp. 115–118.

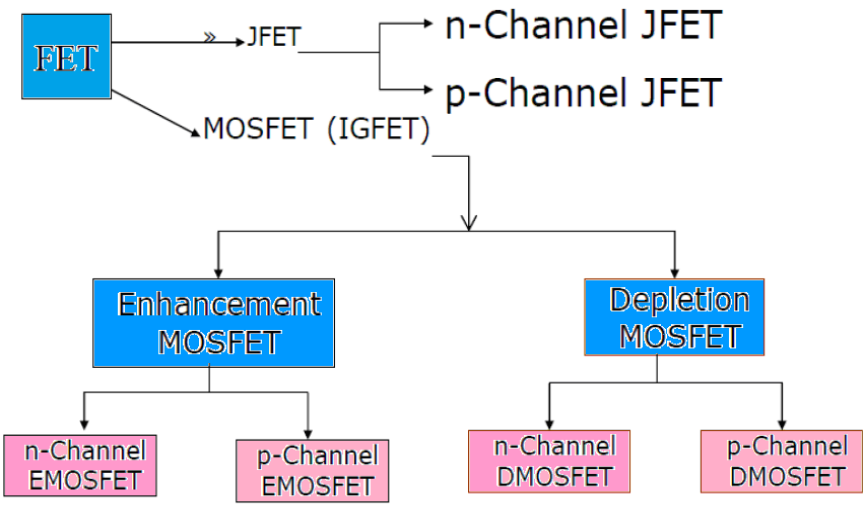
3. Unipolar Transistors (Field Effect Transistors)

The theory of Field Effect Transistor had been designed around 1920~1930 which is 20 years before the Bipolar Junction Transistor has been invented, from 1940's and through early 1950s. At that time J.E. Lilienfeld of America suggested a transistor model having two metal contacts at each side with metallic plate (Aluminum) on top of the semiconductor. The electric field at the semiconductor surface formed by the voltage applied to the metallic plate enabled the control of the current flow between the metal contacts, and this was the initial conception of the Field Effect Transistor. But due to the immature semiconductor materials and the technology, the progress of the development was very sluggish. In 1952, W. Shockley introduced JFET (Junction Field Effect Transistors), in 1953, Dacey and Ross materialized it. In JFET, the metallic plate of Lilienfeld structure was replaced by pn junction, and named the metal contact as source and drain, and also named the field effect electrode as gate. However, the materials processing technology was not mature enough until 1960 when John Attalla produced a working device.

A *field effect transistor* (FET) is a *unipolar* device, conducting a current using only one kind of charge carrier. If based on an N-type slab of semiconductor, the carriers are electrons. Conversely, a P-type based device uses only holes. Even though there were continuous researches of small-signal MOSFET after that, there was no prominent result for the power MOSFET, and the commercially available products started to come out by 1970s.

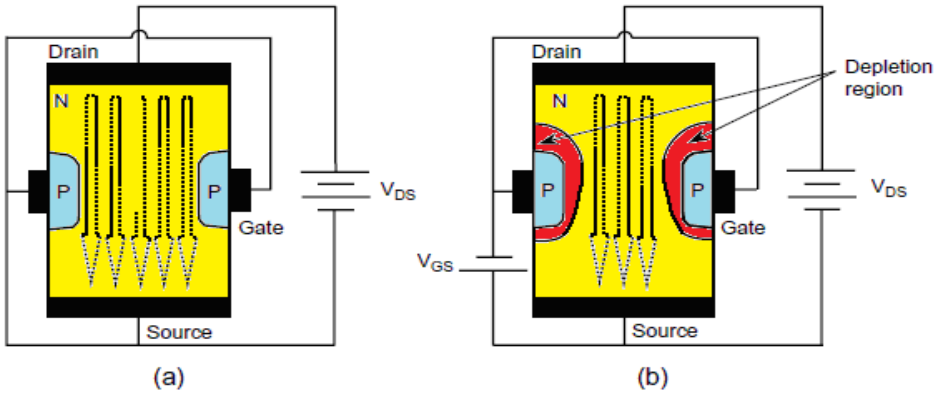
Important advantage of FET over conventional transistors

- unipolar device operation depends only on one type of charge carriers
- voltage controlled device (gate voltage controls drain current)
- very high input impedance
- source and drain are interchangeable in most low- frequency applications
- low voltage low current operation is possible (low power consumption)
- less noisy as compared to BJT
- no minority carrier storage (turn off is faster)
- self limiting device
- very small in size , occupies very small space in ICs
- low voltage low current operation is possible in MOSFETS
- zero temperature drift of out put is possible



3.1 JFET (Junction Field Effect Transistors)

There are two kinds of JFETs. One is n-channel type and the other is p-channel type. They both control the drain-to-source current by the voltage supplied to the gate.



(a) When VGS (Gate-source voltage) has not been supplied

(b) When VGS (Gate-source voltage) has been supplied

Figure.3.1: *the structure of JFET and its operation*

As shown in the Fig. 3.1 (a), if the bias is not supplied at the gate, the current flows from drain to source, and when the bias is supplied at the gate, depletion region begin to grow and reduces the current as shown in Fig. 3.1 (b). And the reason why the depletion region of the drain is wider than the depletion region of the source is because the reverse bias of the gate and the drain $V_{DG}(=V_{GS}+V_{DS})$ is higher than the V_{GS} (bias between the gate and the source).

3.2. Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

MOSFET device is the most widely used semiconductor device and is at the heart of each digital circuit. Without MOSFET there would be no computers systems, no computer industry, no digital telecommunication systems, no mobiles phones ,video games, no microelectronic devices and no digital wristwatches. MOS transistors are also increasingly used in analog applications such as switched capacitor circuits, analog-to-digital converters, and filters.

The exponential progress of MOS technology is best illustrated by the evolution of the number of MOS transistors integrated in a single memory chip or single microprocessor. Each memory cell of a dynamic random-access memory (DRAM) contains a MOS transistor and a capacitor [1]. The integration density of memory circuits is about 5 to 10 times higher than that of logic circuits such as microprocessors because of the more repetitive layout of transistors in memory chips. The increase in integration density is essentially due to the reduction of transistor size. The first experimental 1-gigabit DRAMs were reported in 1995 [2] where 1-gigabit DRAM contains over a billion MOSFETs. About four hundred of these chips can be fabricated on a single silicon wafer, 40 centimeters in diameter. Such a wafer, therefore, contains over 400,000,000,000 transistors. This number is equal to the number of stars in our galaxy...More MOSFETs have been fabricated during the last ten years than grains of rice have been harvested by humans since the dawn of mankind. The first working MOS transistor was realized in 1960 by Kahng and Attala.[3] and then introduced in the 70s .A few years later, the integrated circuit industry took off to reach incredible level and has become one of the leading industries worldwide . MOSFETs have become the dominant device technology for many reasons.

- MOSFET has very high gate impedance; it provides the simplest gate drive requirements.
- MOSFET is a voltage control device, it requires small gate currents to charge and discharge the high input gate capacitance;
- Channel conductivity can easily be controlled using low power integrated gate drive circuit.
- MOSFET is a majority carrier device hence there is no minority charge involved in its operation. The charging and discharging of the input capacitance dictate the MOSFET switching time.

- Its faster switching operation, hence no storage time is encountered.
- The MOSFETs have superior ruggedness and safe operation area (SOA) compared to bipolar transistors, which allows elimination of snubber circuits for protection in hard-switching Application.
- MOSFET's are majority carriers exhibit increased resistivity with temperature, thus thermal runaway behavior is avoided.

Due to the above-mentioned advantage of the MOSFET characteristics, it is desirable to utilize power MOSFETs even for high voltage and high power electronics applications after it was restricted only to the low and medium power electronics applications.

3.2.1 MOSFET Structure and Operation

The MOS transistor, also called MOSFET (Metal –Oxide Semiconductor Field- Effect transistor) or IGFET (Insulated-Gate Field- Effect Transistor) .MOSFET is based on the original field effect transistor introduced in the 70s. During that, there were bipolar devices with blocking voltage capacity of 500V and high current capabilities. The idea was to replace bipolar devices with MOSFETs for high power use. Fig.3.2. shows the device schematic structure and symbol of MOSFET.

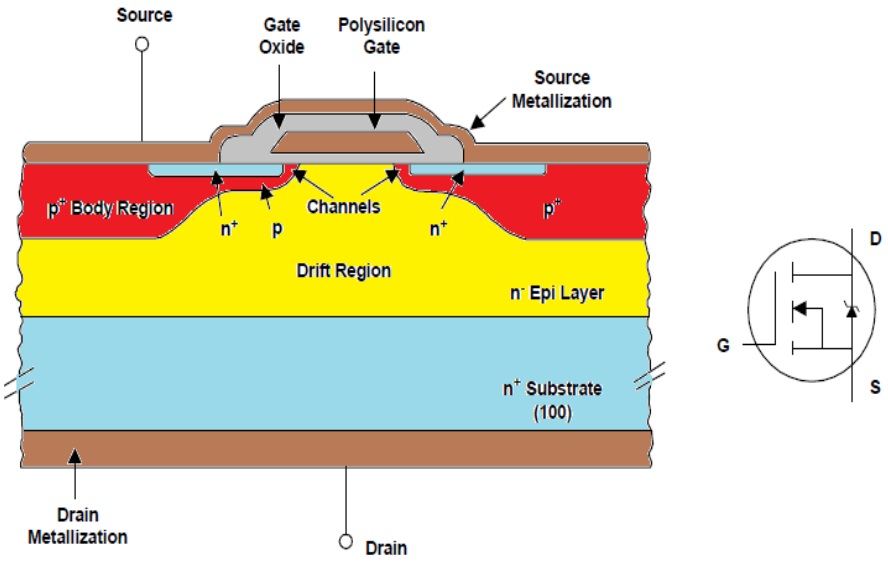


Figure. 3.2: *Schematic Diagram for MOSFET*

The MOSFET is a unipolar device and thus has a high switching speed faster than BJT or thyristor. On the other hand, the power handling capabilities of the MOSFET are lower compared to the thyristor because of high on-state resistance associated with high blocking voltage. The MOSFET is also a voltage controlled device where the junction

transistor is a current controlled device. Higher switching speed means operation at higher frequency where other system components such as inductors can be made smaller, and voltage control instead of current control means less internal energy loss in the device.

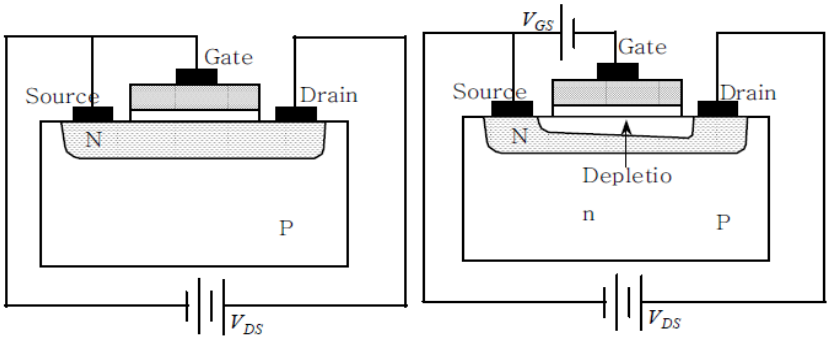


Figure. 3.3: *The structure of depletion type MOSFET and its operation*

(a) When VGS (Gate-source voltage) has not been supplied

(b) When VGS (Gate-source voltage) has been supplied

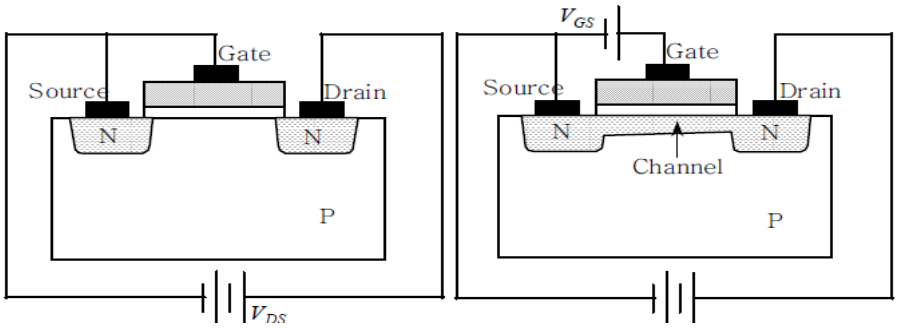


Fig. 3.4*: The structure of enhancement type MOSFET and its operation*

(a) When VGS (Gate-source voltage) has not been supplied

(b) When VGS (Gate-source voltage) has been supplied

There are depletion type and enhancement type, and each has n / p – channel type. Fig. 3.3 shows .The depletion type is normally on, and operates as JFET. And Fig. 3.4 shows the enhancement type is normally off, which means that the drain – to – source current increases as the voltage at the gate increases. And no current flows when there is no voltage supplied at the gate.

The lateral n-channel power MOSFET cell, often termed VDMOS,(vertically diffused MOSFET). It is shown in Fig.3.5: it is fabricated by epitaxially growing the N- drift

region on top of the N+ drain contact [4]. The P body region and the N+ source contact are created using diffusion process.

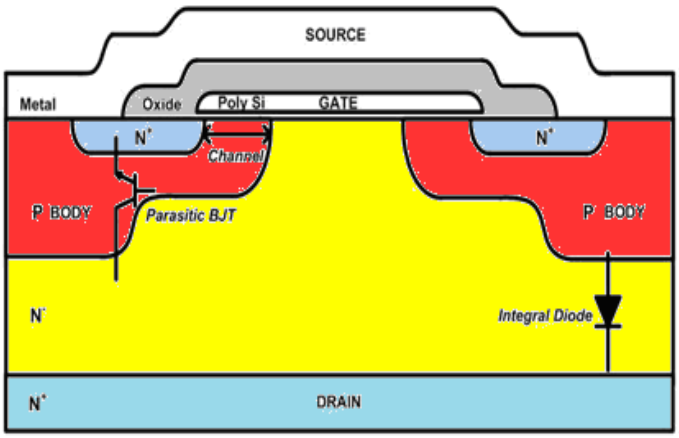


Figure. 3.5: *Basic VDMOS cross section*

Many thousands of these cells exist in a single power MOSFET. We will focus on the basic vertical diffusion power MOSFET cross section. There is a parasitic npn BJT between the drain and source of the MOSFET with the body region acting as the base of the BJT. Current can be fed to the body region of the MOSFET by changing the voltage across the drain and source terminals. To avoid the occurrence of this parasitic BJT turning on, the source and the body region are shorted together, creating an integral diode within the MOSFET. These modes of operation are shown in Fig. 3.6.

As with all enhancement mode, n-channel MOSFETS, when a small positive bias is applied to the gate of the power MOSFET, a depletion region is formed in the body immediately underneath the gate oxide layer. As this gate bias increases to a value that is greater than V_{Th} or equal to it. The electric field created by gate charge attracts a high density of free electrons to the body-oxide interface. This accumulation of negative charge, the inversion layer, effectively allows free electrons to pass through the p-type body region as if the free electrons were moving through an n-type semiconductor there are three primary modes of operation for the power MOSFET: ohmic, saturation, and forward blocking or cutoff.

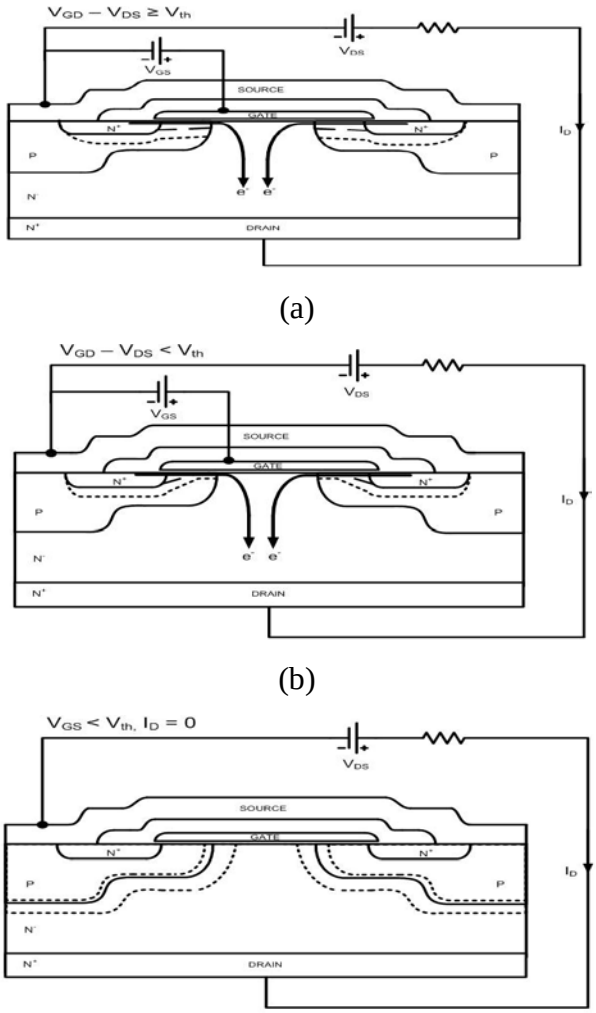


Figure .3.6: *Three primary modes of operation for the power MOSFET (a) conduction in the ohmic region; (b) conduction in the saturation region; (c) forward blocking.*

The output characteristics due to V_{DS} in many V_{GS} conditions (Fig.3.7)

Where V_{GS} is the gate -source voltage and V_{DS} is the drain – source *voltage.*

i. **Ohmic region**: Constant resistance region. If drain-to-source voltage is zero, the drain current also becomes zero regardless of gate–to-source voltage. This region is at the left side of $V_{GS} - V_{GS(th)} = V_{DS}$ boundary line ($V_{GS} - V_{GS(th)} > V_{DS} > 0$), and in this region, even if the drain current is very large, the power dissipation could be maintained by minimizing the $V_{DS(on)}$.

ii. **Saturation region**: Constant current region. It is at the right side of $V_{GS} - V_{GS(th)} = V_{DS}$ boundary line, and in this region, the drain current differs by the

gate– to-source voltage, not by the drain-to-source voltage. Here, the drain current is called saturated.

iii. **Forward blocking** (cut-off region): when the gate-to-source voltage is lower than $V_{GS(th)}$ (threshold voltage).

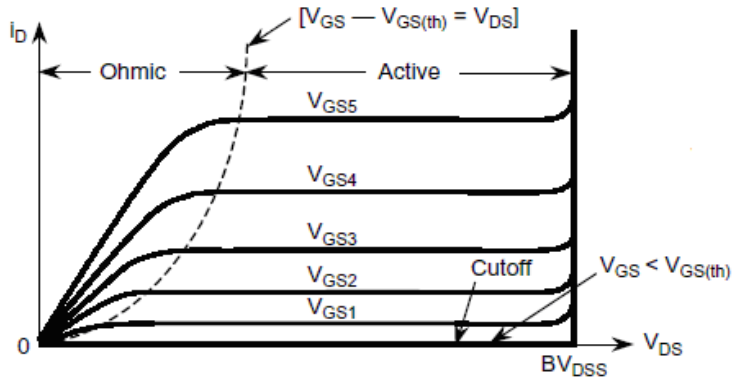


Figure .3.7: *the out put characteristics*

In the ohmic region where $V_{GS}>V_{Th}$, V_{DS} is small in comparison to V_{GS} ensuring nearly uniform thickness from source to the drain side of the inversion layer. As V_{DS} increases and the voltage potential between the gate and drain decreases, the inversion layer narrows on the drain end of the channel, and thus current density at this side of the channel increases. When V_{DS} becomes large enough where $V_{GS} - V_{DS} < V_{Th}$, the drain side of the inversion layer disappears, but current flow is maintained by the electric field between the source and drain areas. If the gate voltage is removed, the inversion layer completely disappears and electrons are no longer injected anywhere into the body region of the MOSFET.

3.2.2. Basic Principle of MOSFET

A circuit containing only n-channel devices is produced by an n-MOS process. Similarly, a p-MOS process fabricates circuits that contain only p-channel transistors.

An n-channel MOS transistor is fabricated in a P-type semiconductor substrate, usually silicon. Two N-type diffusions are made in the substrate and the current flow will take place between these two diffusions. The diffusion with the lowest applied potential is called the "source" and the diffusion with the highest applied potential is called the "drain". Above the substrate and between the source and the drain lie a thin insulating layer, usually Sio_2 silicon dioxide, and a metal electrode called "gate" (Fig.3.8). An electron-rich layer referred to as the "channel" can be created the basic operation of the

n-channel MOSFET is the following. We will first consider the case where the gate voltage is equal to zero while the P type substrate and the source are grounded (V_{sub}= V_S=0) the drain is connected to a positive voltage source for instance). Since the source and the substrate are at the same potential there is no current flow in the source-substrate junction.

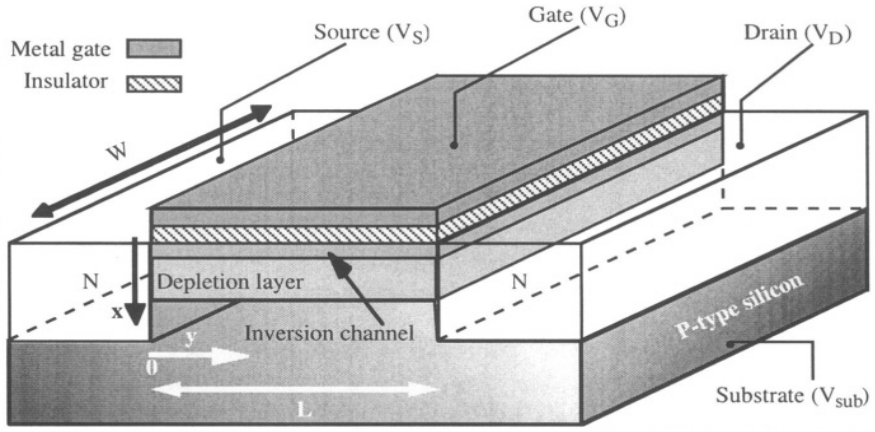


Figure 3.8: *N- channel MOS transistor.*

The drain-substrate junction is reverse biased and except for a small negligible reverse leakage current no current flows in that junction either. Under these conditions there is no channel formation, and therefore, no current flow from source to drain. In the second case a constant positive bias is applied to the gate. There is no gate current since the metal electrode is dielectrically insulated from the silicon. Because it is positively biased the gate electrode does; however, attract electrons from the semiconductor, and a thin, electron rich layer forms under the gate insulator. These electrons are supplied by the source and the drain which, being N-type, are large reservoirs of electrons. The electron-rich layer underneath the gate is called "channel". The N-type source and the N-type drain are connected by the electron rich channel, and current is now free to flow between sources and drain .The effect of the gate voltage controlling the concentration of electrons in the semiconductor through the gate oxide is called "field effect". The bias on the gate creates an electric field which can either induce or inhibit the formation of an electron-rich region at the surface of the semiconductor. The terms "source", "drain", "channel" and "gate" come to mind quite naturally since the electrons originate at the source, flow through the channel and are finally collected by the drain; the whole process being controlled by the bias on the gate. The current in the channel, from source

to drain can, to a first approximation, be estimated using Ohm's law. Using *V=IR* in a small channel element having a length *dy, and* a width *W* we obtain:

$$dV(y) = I\, dR(y) \tag{3.1}$$

The channel resistance as a function of *y* is obtained from

$$\sigma = q(n\,\mu_n + p\,\mu_p) \quad \text{and} \quad \rho = \frac{1}{\sigma} \tag{3.2}$$

Where $\sigma\ (\Omega^{-1}\mathrm{cm}^{-1})$ is the conductivity, and $\rho\ (\Omega\ \mathrm{cm})$ is the resistivity, of an homogeneously doped semiconductor. The electron concentration in the channel per unit area (unit :cm^{-2}) results from integrating the electron concentration per unit volume (unit :cm^{-3}) over the thickness of the device:

$$dR(y) = \frac{dy}{q\,\mu_n\, W \int_0^{\infty} n(x,y)\, dx} \tag{3.3}$$

Where *x* is the depth in the silicon (*x = 0* denotes **silicon/sio$_2$** interface). Note that the electron charge per unit area in the channel element can be written as:

$$Q_n(y) = q \int_0^{\infty} n(x,y)\, dx \quad (\mathrm{C\ cm}^{-2}) \tag{3.4}$$

The formation of a channel occurs when the gate voltage is positive and sufficiently high. In practice, the channel is formed if the gate voltage is larger than a given value named the "threshold voltage",(V_{TH}) . Considering that the Metal-Oxide-Semiconductor structure forms a parallel-plate capacitor, we can write:

$$Q_n(y) = C_{ox}\,(V_G - V_{TH} - V(y)) \tag{3.5}$$

Where C_{OX} is the capacitance of the gate oxide per unit area and *V(y)* is the local potential in the channel element, which varies from $V_{(y=0)} = VS = 0$ near the source to $V_{(y=L)} = V_D$ near the drain.

Introducing Equations (3.3) and (3.5) into Expression (3.1) we obtain:

$$I\,dy = \mu_n W C_{ox} (V_G - V_{TH} - V(y))\,dV \qquad \textbf{(3.6)}$$

Since and since V_S = 0V the current / is constant from source to drain, the integration of Equation (3.6) yields:

$$I \int_0^L dy = \mu_n W C_{ox} \int_0^{V_D} (V_G - V_{TH} - V(y))\,dV \qquad \textbf{(3.7)}$$

$$\Downarrow$$

$$I = \mu_n C_{ox} \frac{W}{L}\left((V_G - V_{TH})\, V_D - \frac{V_D^2}{2} \right) \qquad \textbf{(3.8)}$$

If the local potential between source and drain, *V(y),* becomes equal to or larger than $V_G - V_{TH}$ the formation of a channel can locally no longer be supported near the drain and the channel exists only between *y=0* and a location *y* where $V(y) = V_G - V_{TH}$. In practice, that location is very close to *L,* and the current is obtained by replacing V_D by $V_G - V_{TH}$ in Expression (3.8). The current is then called the saturation current" and noted I_{sat} . Saturation takes place when $V_D \geq V_G - V_{TH}$, and replacing V_D by $V_G - V_{TH}$ in Equation (3.8) we obtain:

$$I_{sat} = \mu_n C_{ox} \frac{W}{L} \frac{(V_G - V_{TH})^2}{2} \qquad \textbf{(3.9)}$$

Note that the current in saturation no longer a changes with the change drain voltage and that the potential drop in the y-direction in the channel is fixed at a value equal to $V_G - V_{TH}$ in saturation.

In a p-channel MOSFET the source is at the highest potential and supplies holes to the channel. The holes are finally collected by the drain, which is at lower potential than the source. In this case a negative bias relative to the substrate must be applied to the gate to create a hole-rich p-type channel. A study of the metal-insulator-semiconductor structure, called the "MOS capacitor", will aid in the understanding of the detailed operation of the MOS transistor.

3.2.3. Characteristics Of The MOS Capacitor

An understanding of the qualitative behavior of the MOS capacitor provides a basis for understanding operation of the MOSFET. At the heart of the MOSFET is the **MOS capacitor** structure depicted in Fig. 3.9. The MOS capacitor is used to induce charge at the interface between the semiconductor and oxide. The top electrode of the MOS capacitor is formed of a low-resistivity material, typically aluminum or heavily doped poly silicon (polycrystalline silicon). We refer to this electrode as the **gate (*G*)** for reasons that become apparent shortly. A thin insulating layer $\mathbf{T_{ox}}$ is the thickness of the gate oxide, typically silicon dioxide, isolates the gate from the substrate or body. The semiconductor region that acts as the second electrode of the capacitor. Silicon dioxide is a stable, high-quality electrical insulator readily formed by thermal oxidation of the silicon substrate. The ability to form this stable high-quality insulator is one of the basic reasons that silicon is the dominant semiconductor material today. The semiconductor region may be *n*- or *p*-type, as depicted in Fig. 3.9.

Semiconductor forming the bottom electrode of the capacitor has a substantial resistivity and a limited supply of holes and electrons. Because the semiconductor can therefore be depleted of carriers, the capacitance of this structure is a nonlinear function of voltage.

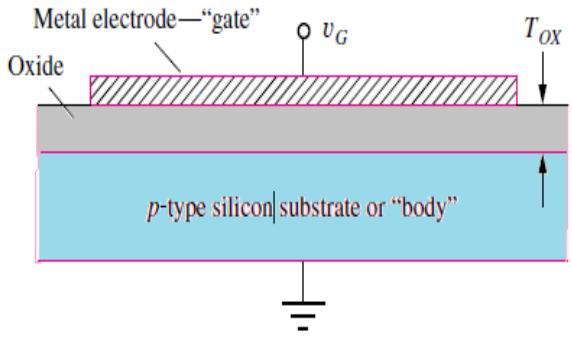


Figure.3.9: *MOS capacitor structure on p-type silicon.*

Figure 3.10 shows the conditions in the region of the substrate immediately below the gate electrode for three different bias conditions: accumulation, depletion, and inversion.

1-Accumulation Region

The situation for a large negative bias on the gate with respect to the substrate is depicted in Fig. 3.10(a). The large negative charge on the metallic gate is balanced by positively charged holes attracted to the Si-SiO_2 silicon dioxide interface directly below the gate. For the bias condition shown, the hole density at the surface exceeds the value met in the original *p*-type substrate, and the surface is said to be operating in the

accumulation region or just in **accumulation.** This majority carrier accumulation layer is extremely shallow, effectively existing as a charge sheet directly below the gate.

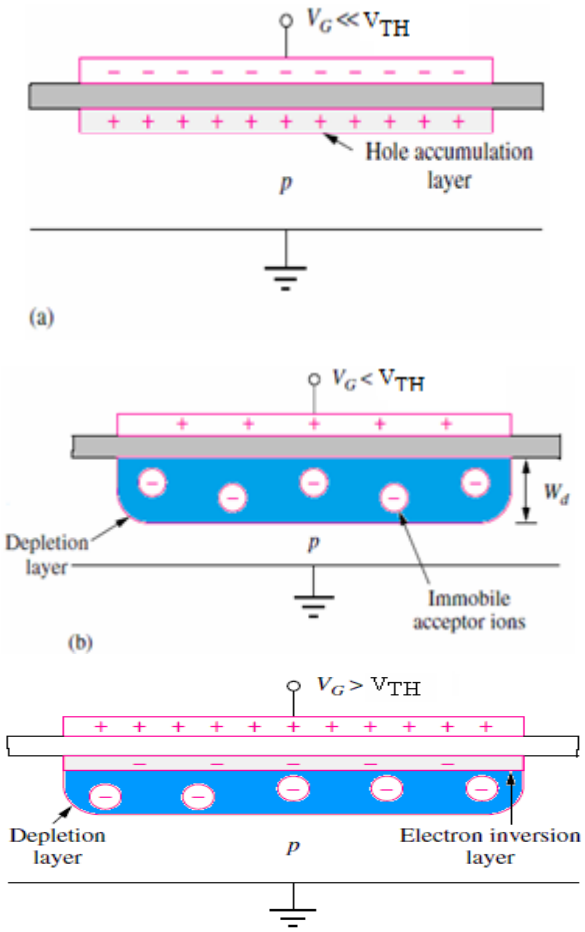


Figure.3.10: *MOS capacitor operating in (a) accumulation, (b) depletion, and (c) inversion. Parameter V_{TH} in the figure is called the threshold voltage and represents the voltage required to just begin formation of the inversion layer.*

2-Depletion Region

Now consider the situation as the gate voltage is slowly increased. First, holes are repelled from the surface. Eventually, the hole density near the surface is reduced below the majority-carrier level set by the substrate doping level, as depicted in Fig. 3.10(b). This condition is called **depletion** and the region, the **depletion region.** The region beneath the metal electrode is depleted of free carriers in much the same way as the depletion region that exists near the metallurgical junction of the *pn* junction diode. in Fig. 3.10(b), positive charge on the gate electrode is balanced by the negative charge of the ionized acceptor atoms in the depletion layer. The depletion-region width W_d can

range from a fraction of a micron to tens of microns, depending on the applied voltage and substrate doping levels.

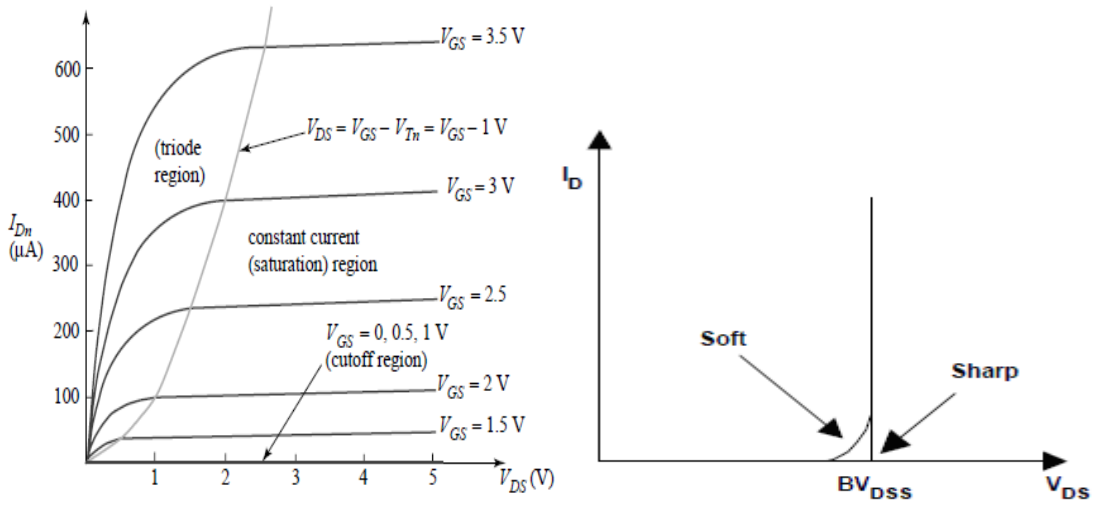
3-Inversion Region

As the voltage on the top electrode increases further, electrons are attracted to the surface. At a particular voltage level, which we will shortly define as the **threshold voltage,** the electron density at the surface exceeds the hole density. At this voltage, the surface has inverted from the *p*-type polarity of the original substrate to an *n*-type **inversion layer,** or **inversion region,** directly underneath the top plate as indicated in Fig. 3.10(c). This inversion region is an extremely shallow layer, existing as a charge sheet directly below the gate. In the MOS capacitor, the high density of electrons in the inversion layer is supplied by the electron–hole generation process within the depletion layer.The positive charge on the gate is balanced by the combination of negative charge in the inversion layer plus negative ionic acceptor charge in the depletion layer. The voltage at which the surface inversion layer is just formed plays an extremely important role in field-effect transistors and is called the **threshold voltage (V_{TH}).**

3.2.4. MOSFET Characteristics

3.2.4.1. Breakdown Voltage

Breakdown voltage, BVDSS, is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the source and drain by the avalanche multiplication process, while the gate and source are shorted together [5]. For drain voltages below BVDSS and with no bias on the gate, no channel is formed under the gate. The surface and the drain voltage is entirely supported by the reverse-biased body drift pn junction. The Current-voltage characteristics of a power MOSFET are shown in Fig. 3.11(a). For drain voltages below B_{VDSS} and with no bias on the gate, no channel is formed under the gate at the surface and the drain voltage is entirely supported by the reverse-biased body-drift p-n junction. Two related phenomena can occur in poorly designed and processed devices: punch-through and reach-through. Punch through is observed when the depletion region on the source side of the body-drift p-n junction reaches the source region at drain voltages below the rated avalanche voltage of the device.



(a) (b)

Figure.3.11: *Current-voltage characteristics of a power MOSFET*

This provides a current path between source and drain and causes a soft breakdown characteristic as shown in Fig. 3.11(b). The leakage current flowing between source and drain is denoted by I_{DSS}. There are tradeoffs to be made between $R_{DS(on)}$ requiring shorter channel lengths and punch-through avoidance for higher values channel length. The reach-through phenomenon occurs when the depletion region on the drift side of the body-drift p-n junction reaches the epilayer-substrate interface before avalanching takes place in the epi. Once the depletion edge enters the high carrier concentration substrate, a further increase in drain voltage will cause the electric field to quickly reach the critical value of $2x10^5$ V/cm where avalanching begins.

3.2.4 .2. On Resistance

The on resistance of a power MOSFET is the total resistance between the source and drain terminals during the on- state. It is the important device parameter because it determines the maximum current rating .The cell structure with each component of the specific on resistance is shown in the Figure.3.12: The on-state resistance of a power MOSFET consists of several components [5] .

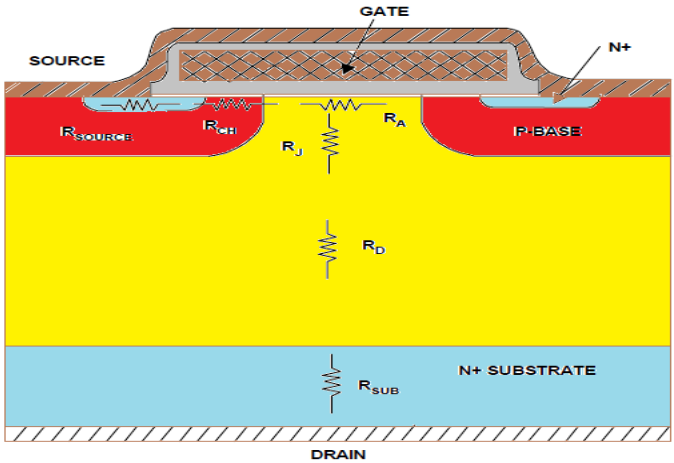


Figure3.12: *Origin of Internal Resistance in a Power MOSFET.*

Where:

R_S : Source diffusion resistance

R_{ch} : Channel resistance

R_A :Accumulation resistance

R_J :"JFET" component-resistance of the region between two body regions

R_D : Drift region resistance

R_{sub} : Substrate resistance

R_{wcml} - Sum of Bond Wire resistance, the Contact resistance between the source and drain Metallization and the silicon, metallization and Lead frame Contributions. These are normally negligible in high voltage devices but can become significant in low voltage devices. The relative importance of each of the components to $R_{DS(on)}$ over the voltage spectrum. At high voltages the $R_{DS(on)}$ is dominated by epi resistance and JFET component. This component is higher in high voltage devices due to the higher resistivity or lower background carrier concentration in the epi. At lower voltages, the $R_{DS(on)}$ is dominated by the channel resistance and the contributions from the metal to semiconductor contact, metallization, bond wires and lead frame. The substrate contribution becomes more significant for lower breakdown voltage devices.

3.2.4.3. Threshold Voltage

Threshold voltage, V_{th}, is defined as the minimum gate electrode bias required strongly inverting the surface under the poly and forming a conducting channel between the

source and the drain regions. V_{Th} is usually measured at a drain current of 250mA. Common values are 2-4V for high voltage devices with thicker gate oxides, and 1-2V for lower voltage, logic compatible devices with thinner gate oxides [5]. power MOSFETs with enhancing use in portable electronics and wireless communications where battery power is at a premium, the trend is toward lower values of $R_{DS(on)}$ and V_{th}.

3.2.4 .4. Diode Forward Voltage

The diode forward voltage, VF, is the guaranteed maximum forward drop of the body-drain diode at a specified value of source current. P-channel devices have a higher VF due to the higher contact resistance between metal and p-silicon compared with n-type silicon [5].

3.2.4 .5. Breakdown Voltages

There are basically two types of breakdown voltages, namely:

I. Avalanche breakdown

It is the mobile carriers' sudden avalanche caused by increasing electric field in the depletion region of body-drain pn junction up to a critical value, being it is the most dominant factor among other factors that drive the breakdown more clearly. The junction formed by the substrate and drain or source region will conduct a large current if the reverse bias applied to them exceeds a certain value (because the field in the junction near the surface is influenced by the presence of the gate, the above value depends on the gate potential and can be different from the predicted common pn junction theory). When the device is on, carriers, moving fast in the channel can have impact on silicon atoms and ionize them, producing electron-hole pairs; this is referred to as *impact ionization.* The newly generated pairs can gain enough energy to impact on silicon atoms and produce more electron-hole pairs. This is called *avalanche effect* and is more pronounced in the pinch-off region near the drain where field can be high. Currents larger than those predicted by common device model will then flow, and the phenomenon is referred to as *channel breakdown*.

Punch-Through breakdown

It occurs in devices with relatively short channels when the drain voltage is increased to the point that the depletion region surrounding the drain region extends through the

channel to the source. The drain current then increases rapidly. Normally, punch-through does not result in permanent damage of the device.

3.2.5 The Characteristics Of a MOSFET

3.2.5.1. Advantages

i. High input impedance - voltage controlled device - easy to drive. To maintain the on state, a base drive current which is 1/5th or 1/10th of collector current is required for the current controlled device (BJT). And also a larger reverse base drive current is needed for the high speed turn-off of the current controlled device (BJT). Due to these characteristics base drive circuit design becomes complicated and expensive. On the other hand, voltage controlled device MOSFET is a switching device which is driven by channel at the semiconductor surface due to the field effect produced by the voltage applied to the gate electrode. Being isolated from the semiconductor surface. And as the required gate current during switching transient as well as on, off state is small, the drive circuit design is simple and the cost of it can be reduced.

ii. (Unipolar device - majority carrier device - fast switching speed). As there are no delays due to storage and recombination of the minority carrier, as in the BJT, the switching speed is faster than the BJT by orders of magnitude. Hence, it has an advantage in a high frequency operation circuit where switching power loss is prevalent.

iii. Wide SOA (safe operating area). It has a wider SOA than the BJT because high voltage and current can be applied simultaneously for a short duration. This eliminates destructive device failure due to second breakdown.

iv. Forward voltage *drop with positive temperature coefficient* - easy to use in parallel. When the temperature increases, the forward voltage drop also increases. This causes the current to flow equally through each device when they are in parallel. Hence, the MOSFET is easier to use in parallel than the BJT, which has a forward voltage drop with negative temperature coefficient.

3.2.5.2. Disadvantage

In high breakdown voltage devices over 200V, the conduction loss of a MOSFET is larger than that of a BJT, which has the same voltage and current rating due to the on-state voltage drop.

3.2.6. DC Behavior of High Voltage Power –MOSFETs

The high voltage devices show some special effects due to high electric field inside the device e.g. self-heating, quasi-saturation and impact ionization effects. In fact, some of these effects (self-heating and impact ionization) are also visible in low voltage MOSFETs as electric field in these devices also becomes quite high as channel length is decreased. Even though above mentioned effects arise due to high electric fields in the device, some other special effects are also observed due to different device processes in these devices compared to conventional MOSFETs. One of the major difference in terms of device process is the lateral non-uniform doping in the channel and drift region in the drain side of HV devices. Here we will discuss the physical origin of these effects and their impact on device characteristics.

3.2.6.1 Quasi-Saturation Effect

The quasi-saturation effect [6, 7, 8, 9, 10] is one of the unique effects observed in HV devices other than bipolar devices [11, 12, 13, 14, 15, 16]. This effect originates due to velocity saturation or current crowding in the drift region when intrinsic MOS is still not saturated and represents a major problem in these devices as it results in high on resistance, which is not desired. If drift velocity is saturated and intrinsic MOS is in linear region, the increase in V_{GS} does not increase current level significantly and gate bias has small effect. Our drift resistance already includes the velocity saturation in the drift.If the VDIMOS is considered, it turns out to necessarily investigate drain current expressions in both channel and drift region described by simple model:

Channel:

$$I_D = \mu_n^* \frac{W}{L} C_{ox}' \frac{2(V_{GS} - V_T).V_{Ch} - (1+\delta)V_{Ch}^2}{1 + \frac{\mu_n^*}{L.v_S}.\frac{V_{GS} - V_T}{1+\delta}} \qquad \text{Channel in triode regime } V_{ch} < V_{GS}\text{-}V_T \qquad \textbf{(3.10)}$$

$$I_D = \mu_n^* \frac{W}{L} C_{ox}' \frac{\frac{(V_{GS}-V_T)^2}{1+\delta}}{1+\frac{\mu_n^*}{L.v_S}.\frac{V_{GS}-V_T}{1+\delta}} \qquad \text{Channel saturated } V_{ch} \geq V_{GS}-V_T \qquad \textbf{(3.11)}$$

Drift Region:

$$V_{DR} = \frac{v_S}{\mu_n}\left\{ W_A \frac{I_D}{I_{D0}-I_D} + \frac{L_P tg\alpha}{2}\frac{I_D}{I_{D0}} \ln \frac{\left(1+\frac{L_P}{L_d}\right)I_{D0}-I_D}{I_{D0}-I_D} + \frac{W_T - W_A - \frac{1}{2}L_P tg\alpha}{\left(1+\frac{L_P}{L_d}\right)I_{D0}-I_D} \right\} \qquad \textbf{(3.12)}$$

Both these characteristics exhibit the property of saturation (i.e. maximal value of drain current). The question that naturally arises is: which of these regions will be the first to get saturated. The answer is: that depends on applied V_{GS}: And to discuss the saturation mechanisms in HV devices [17] using output characteristics of VDMOS transistor shown in Fig.3.13 The current saturation on I_{DS} ¡ V_{DS} **characteristics can occur following one of these mechanisms:**

a) Low V_{GS} Values:

For a fixed gate voltage, if drain voltage is increased, the channel gets depleted and drain current gets saturated before velocity saturation occurs.

This effect is called pinch-off and it is also the normal saturation mechanism in long channel MOSFETs. In HV devices, the channel pinch-off is generally observed at low V_{GS} (see V_{GS} = 1V curve in Fig. 3.13).

$I_D(V_{DS})$ characteristic has two abruptly distinguished regions (triode region and saturation) drain current saturation happens first in channel;the drift region characteristic is still linear – very far from getting saturated – channel is the first to get saturated ,while drift region stays very far from saturation .

b) Medium V_{GS} :

Velocity saturation in the channel: If the lateral electric field in the channel is more than certain limit called as critical field, the velocity of the electrons gets saturated and thus there will be no further increase in the current for any further increase in the drain

voltage. This effect is called velocity saturation, which is quite common phenomenon in short channel MOSFETs. In HV devices, this effect is generally observed for medium to high V_{GS} (see I_{DS} *i* V_{DS} curves for V_{GS} = 1:5*;* 2*;* 2:5*;* 3*V* at V_{DS}=30V in Fig. 3.13). A simple way to see this effect is that when intrinsic MOS is velocity saturated, the output characteristics become equidistant for equal increase in V_{GS}.

Drain current still takes place in channel, but after velocity saturation onset (drift region is still rather far from saturation):

$$\frac{\mu_n^*}{L v_S^*}.\frac{V_{GS}-V_T}{1+\delta} \rangle\rangle 1 \Rightarrow \qquad \textbf{(3.13)}$$

$$I_D, ch^{SAT} \approx \mu_n^* \frac{W}{L} C_{ox}' \frac{\frac{(V_{GS}-V_T)^2}{1+\delta}}{1+\frac{\mu_n^*}{L.v_S}.\frac{V_{GS}-V_T}{1+\delta}} \approx v_S .WC_{ox}'.(V_{GS}-V_T) \qquad \textbf{(3.14)}$$

Obviously $I_{D,}ch^{SAT}$ is linearly dependent on V_{GS}, what results in equidistant I_D (V_{DS}) characteristics in saturation (clear announcement of "quasi -saturation ") . The nonlinear $I_D(V_{DR})$ dependence results in more smooth transition between triode regime and saturation .

c) High V_{GS} Value:

For extremely high values of V_{GS} the saturated drain current in channel achieves (over even surpasses) the saturated drain current in drift region .Anyway, the drift region characteristic slow strong nonlinear behavior ,what further result in very smooth transition between triode regime and saturation concerning total $I_D(V_{DS})$ characteristic . The existence of this very smooth transition is called (**QUASI-SATURATION**) and usually happens in high – voltage and high power devices .From point of view of further modeling of such devices this effect is undesirable (it actually introduces the third region).

$$EQUIDISTANT = \frac{\Delta I_D^{SAT}}{\Delta V_{GS}} = CONSTANT$$

The real drain current saturation happens for such greater values of V_{DS} . The

conventional triode regime described by quadratic $I_D(V_{DS})$dependence is followed by the **"extended"** triode region described by **(**almost/approximately**)** linear $I_D(V_{DS})$that gradually tends toward real drain current saturation .

Velocity saturation in the drift region: Another saturation mechanism can occur due to velocity saturation in the drift while intrinsic MOS is still not saturated. Actually this cannot be called saturation as current does not get saturated. If drift is velocity saturated and intrinsic MOS is in linear region, the increase in V_{GS} does not increase current level significantly and gate bias has no or little effect (see V_{GS} = 2*;* 2*:*5*;* 3*;* 3*:*3*V* in Fig. 3.13).

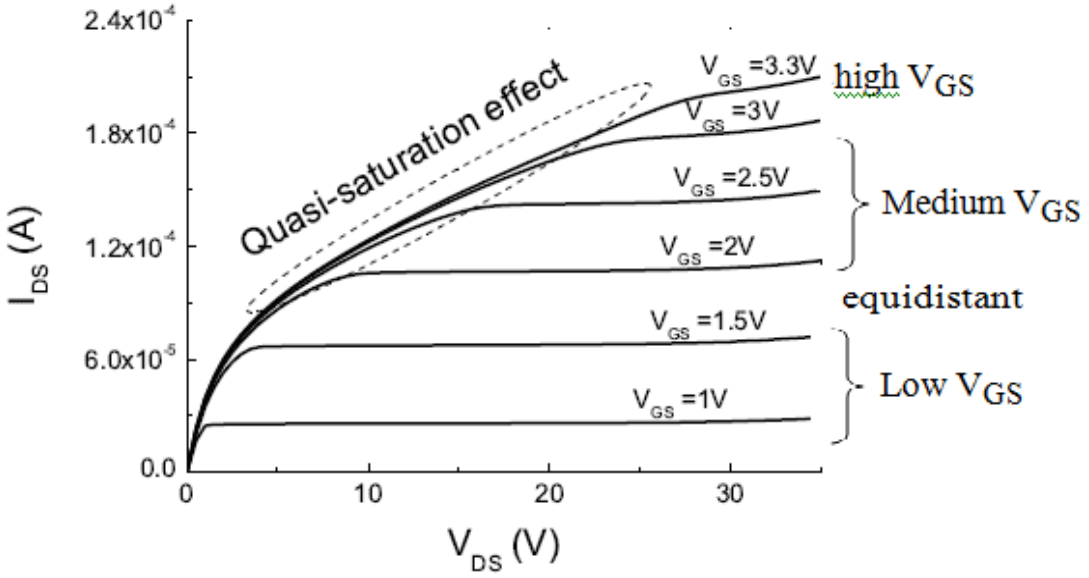


Figure 3.13: *I_{DS} vs. V_{DS} from device simulation of 50V VDMOS transistor. The quasi-saturation effect is evident at higher V_{GS} for this device.*

This effect is called quasi-saturation, which is generally observed at high V_{GS}. Note that all or any two of the three effects described above may superimpose with each other and, sometimes, they may not be separable from each other. The quasi-saturation effect can be reduced by reducing the resistivity of the drift region and parasitic JFET in VDMOS transistor [6]. The reduction in the quasi-saturation effect increases the current carrying capability of the devices and decreases the on-resistance. One possible method of achieving this is to exploit the trench technology [18], which allows the gate to be extended down into the inter cell region. Even though it reduces the quasi-saturation effect, it introduces a corner in the trench which affects the blocking capability of the device. Another method is to use the ion-implantation into the JFET structure of

VDMOS, which reduces the quasi-saturation effect with little change in the blocking capability [6].

3.2.6.2. Self-Heating Effect

The self-heating effect is another unwanted effect observed in high voltage devices. The high voltage and current gives rise to high power dissipation, which in turn increases the temperature inside the device. The rise in temperature severely affects the device characteristics giving rise to negative resistance on output characteristics.

That dissipated heat leads to an increase in the internal temperature of the device. The internal temperature increase influences the device characteristics mainly by affecting the mobility, threshold voltage and velocity saturation. The self-heating effect (SHE) [19, 20, 21, 22, 23, 24, 25, 26] represents the effect appears, and modifies the I ¡ V characteristics. Fig. 3.14. Shows the I_{DS} ¡ V_{DS} characteristics of a 40V LDMOS transistor.

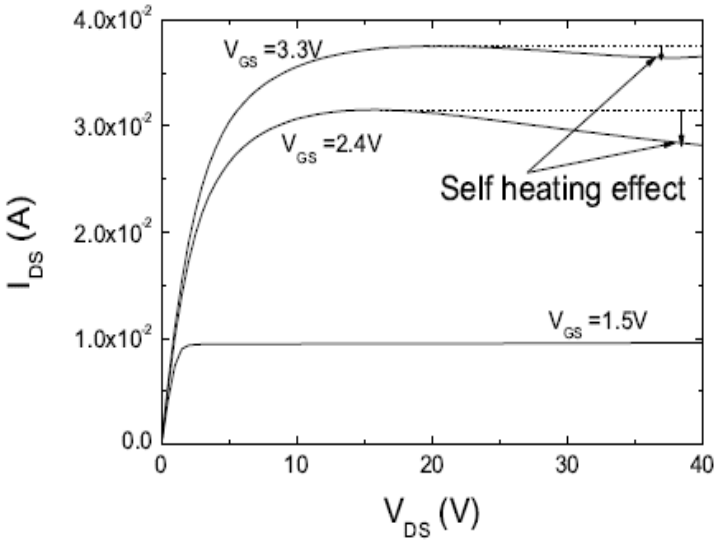


Figure 3.14: *Measured I_{DS} vs. V_{DS} of 40V LDMOS transistor. The decrease in the current with increasing V_{DS} is due to self heating effect.*

The decrease in the current with increasing V_{DS} is caused by the self heating effect. As V_{DS} increases, the current starts rising. The increase in the current (I_{DS}) as well as voltage across the device (V_{DS}) increase the power dissipation ($I_{DS}V_{DS}$) inside the device. As discussed above, the increase in power dissipation increases temperature which affects other transistor parameters (e.g. mobility, threshold voltage etc.). The rise

in temperature decreases mobility due to scattering which in turn decreases the current showing negative resistance on output characteristics. The internal temperature increase due to self heating effect influences the device characteristics mainly by affecting the mobility, threshold voltage and velocity saturation. In the literature, this effect was mainly studied on the SOI devices and the proposed models for SHE is distributed or non-distributed models. As expected, better accuracy is obtained from distributed models, which offer a larger flexibility for the current simulation. Still, the clear advantage of the non-distributed models over the distributed ones is the parameter extraction procedure, as non-distributed approach offers a simple and efficient representation of the problem. The detailed discussion of self-heating effect and its modeling has been covered in [26].

3.2.6.3. Impact Ionization Effect

The impact ionization effect occurs owing to high field in the device. The impact ionization in the high voltage devices occurs at places, the intrinsic MOS and drift region. The impact ionization in the intrinsic MOS region occurs at low to medium V_{GS} for certain V_{DS}, while impact ionization in the drift region dominates at higher gate voltages. Also the impact ionization current in the drift region does not decrease with increase in gate voltage, which is not the case in conventional MOSFET, where it decreases after giving a peak in the drain current for conventional low voltage MOSFETs [27].The increase in the V_{DS} in the MOSFET increases the longitudinal electric field in the channel increasing from source to drain. For abrupt source and drain junctions, the peak field is at the drain-to-channel junction, and its value depends on V_{DS} and channel length L. When carriers move in the fields that exceed the value of the onset of velocity saturation, they continue to acquire kinetic energy from the field but their velocity is randomized by the excessive collisions such that their velocity along the field direction no longer increases but their kinetic energy does. Depending on the statistics of scattering, a small fraction of the overall carrier population acquires a significant amount of energy, and these are called hot carriers. Clearly, the higher the field, the higher the proportion of hot carriers. Generally, in MOSFETs, the high fields are encountered in saturation in the pinch off region. For large longitudinal electric field, the cool electrons are coming into the pinch off region and are heated by the field. Some of them acquire enough energy to create impact ionization of silicon atoms, whereby

new electrons and holes are created; this effect is also referred to as weak avalanche. The new electrons join the stream of channel electrons and move toward the drain. The normal depletion field in the channel pushes the holes into the substrate, where they give rise to drain-to-substrate current (I_{DB}). This current is proportional to the number of electrons available per unit time, which in turn is proportional to I_{DS}. Also, according to above discussion, I_{DB} is an increasing function of the maximum field at the drain; this field is, in turn, a function of the excess drain voltage_(V'_{DS}). Fig. 3.15 shows the typical I_{DB} ¡ V_{GS} curve for MOSFET. For a given V_{DS}, when V_{GS} is increased starting from low values, I_{DS} increases, and thus I_{DB} increases too, according to above discussion. Further increase in V_{GS} increases the saturation voltage significantly, causing a strong decrease in V_{DS} ¡$V'_{D\,S}$, and thus in the maximum field at the drain. The maximum I_{DB} is observed, roughly, at V_{GS} = V_{DS}=2.

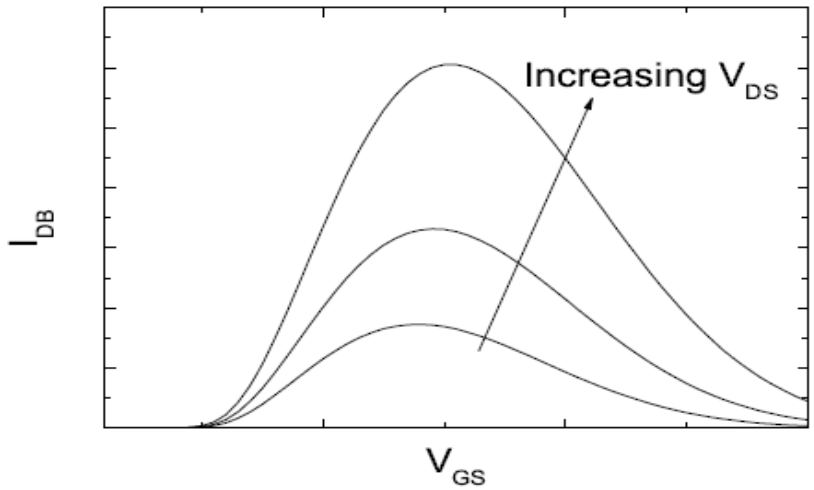


Figure 3.15: *Substrate current vs. gate-source voltage, with drain-source voltage as a parameter. for the LDMOS transistor The impact ionization in the drift can be reduced with the field plate configuration [28].*

3.3. Silicon carbide unipolar devices

Power devices mainly belong to two categories - unipolar and bipolar. Schottky diodes, (JFET) junction field effect transistor and (MOSFETs) metal oxide semiconductor field effect transistor are examples of unipolar devices. Which have been subject to remarkable progress in this decade? In a unipolar device, only one type of carrier (either a majority electron or a majority hole) is responsible for current flow. Unipolar SiC devices can operate at higher frequencies which results in lower switching losses, at higher temperatures. [29]. There is a flow of both majority and minority carriers in bipolar devices. The slower minority carriers have to be injected and removed to get the device to turn on and off, so in bipolar devices there is power loss due to switching and leakage current. Amongst the various polytypes of SiC, 4H-SiC polytype has the widest bandgap energy, high intrinsic carrier mobility.

It has higher and more isotropic mobility compared to other polytypes and hence is used to fabricate MOSFET devices [30,31]. it is considered the most promising for high power MOSFET design capable of blocking several kilovolts in the off state so it is material of choice , (SiC) devices promising to substitute silicon (Si) devices in high voltage ,high frequency applications, owing its higher breakdown voltage . Lower on – state resistance and better high temperature operation capability. and if we compare bipolar n- channel Si- MOSFET with unipolar n- channel SiC- MOSFET we will find The n-channel Si-MOSFET is a good choice for low voltages (around 100V); it can operate at high switching speed, 100 kHz. But as the blocking voltage increases, the on-state resistance increases drastically. In the same time SiC-MOSFET enables us to achieve higher operating voltages (order of kilo volts) with higher switching speed. This is possible because SiC has a high critical breakdown field, almost 7 times that of Si. This advantage is that at higher_critical field of SiC means a much thinner drift region can support the source-drain voltage in blocking state. The superior critical field of SiC permits to use a far thinner drift layer of higher doping concentration and thus greatly reduces the drift resistance's contribution. Moreover, due to unipolar nature of the device we do not have to deal with stored charge and hence MOSFET will have higher switching speed. SiC exists in different polytypes. 4H-SiC polytype has the widest bandgap energy. It has higher and more isotropic mobility compared to other polytypes and hence is used to fabricate MOSFET devices [25, 26]. To use SiC to its full potential, we must continue to work to improve the electrical characteristics of the SiO_2/SiC

interface by developing more efficient processes to passivate defects at the interface that form during the oxidation process. These defects trap carriers (electrons) from the channel to become charged, thereafter acting as Coulomb scattering centers for other channel electrons. The result of trapping and scattering is lower effective channel mobility. At present there is a standard passivation process based on post-oxidation annealing in nitric oxide (NO) [32,33]. These passivations increase the fin version electron channel mobility of a SiC-MOSFET.

3.3.1. Mobility Models

It is well known that an accurate I-V model is strongly based on physical and accurate mobility and velocity saturation models for any devices. At low normal electric fields, the carrier mobility in a semiconductor is a function of the total doping concentration and the temperature. As in the case of Si, lattice scattering (acoustic phonons) and ionized impurity scattering, together with anisotropic scattering [34], seem to be the most relevant mechanisms to limit the mean free path of carriers at low electric fields in SiC [35,36,37]. Since the free-carrier mobilities depend strongly on the magnitude of electric field, the mobility model in MEDICI consists of low field and high field mobility components. An optional module that described the anisotropic mobility is also available.

3.3.1.1. Low Field Mobility

For the low drift mobility, the empirical model given by the Caughey-Thomas equation, as has been confirmed in the case of Si [38], can be selected for simulating 4H SiC. At room temperature, it can be expressed as :

$$\mu_o = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left(\frac{N_D + N_A}{N_{ref}} \right)^{\alpha}} \qquad \textbf{(3.15)}$$

The parameter (μ_{max}) represents the mobility of UN doped or unintentionally doped samples, where lattice scattering is the main scattering mechanism, while (μ_{min}) is the mobility in highly doped material, where ionized impurity scattering is dominant. NREFN (N_{ref}) is the doping concentration at which the mobility is halfway between μ_{max} and μ_{min}, ALPHAN (α) is a measure of how quickly the mobility changes from

μ_{max} *to* μ_{min}, and (N_D+N_A) is the total doping concentration. For N-type 4H SiC doped with nitrogen (N), detailed mobility data measurements reported in [39,40,41,42] are available for curve fitting. The resulting fit of Eq.3.15 to the experimental data at 300 K are shown in Fig.3.16, using $\mu_{Hall} = \mu_{drift}$ [43], with the parameter values listed in Table 3.1.

Table.3.1: *Parameter of low field mobility (Eq.3.15) for 4HSiC at 300K [43].*

Parameter	4H SiC
μ_{min}	40 cm^2/Vs
μ_{max}	950 cm^2/Vs
N_{ref}	$2x10^{17}$ cm^{-3}
α	0.76

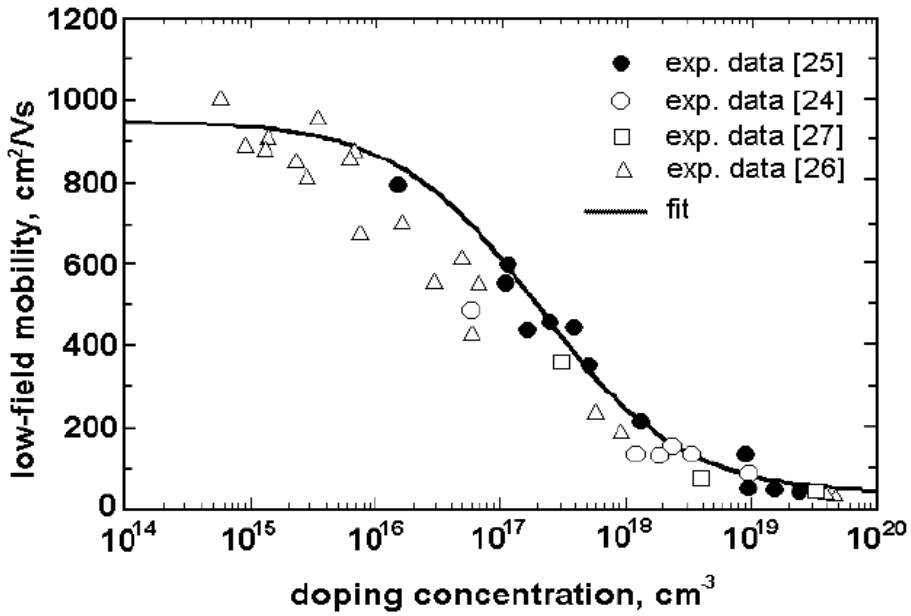


Figure.3.16: *Low field electron mobility as function of doping concentration in 4H SiC (perpendicular to the c-axis, T=300 K). The empirical best fit as shown in solid line is generated using Eq. 3.15 with parameter values given in Table 3.1 [43].*

3.3.1.2. High Field Effect

The high-field mobility component becomes important in the saturation regime of MOSFET operation. At large drain biases, there is a large lateral field near the drain-bulk junction. This causes saturation of the velocity of surface mobile carriers causing

high field mobility to become very small near the drain. Therefore, velocity saturation limits the mobility and thereby current in the saturation region. The high-field mobility reduces with temperature mainly because optical phonon scattering increases causing the Saturation velocity decrease [45]. The behavior of total surface mobility near the drain-bulk junction is quite complex. With a large drain bias, a depletion region develops near the drain-bulk junction causing the mobile electrons to be pushed away. This then causes a reduction in the amount of occupating traps near the drain. Resulting in an improvement in the low-field mobility near the drain. This opposes the reduction in mobility due to velocity saturation. Therefore, the total surface mobility is a complex function of drain bias and temperature. `The analytically expressed in terms of the drift velocity as a function of the electric field in the direction of current flow, defining.

$$\mu(E) = \frac{v_d(E)}{E} \qquad \textbf{(3.16)}$$

The effect of parallel field on the low drift electron mobility model as described in Eq.3.15 uses an expression that is frequently exploited for modeling the field dependence of mobility of silicon [38]:

$$\mu_n = \frac{\mu_{S,n}}{\left[1+\left(\frac{\mu_{S,n}\,E_{\parallel}}{\upsilon_{sat}}\right)^{\beta_{sat}}\right]^{\frac{1}{\beta_{sat}}}} \qquad \textbf{(3.17)}$$

Here $\mu_{S,n}$ is the low field mobility which may include the scattering mechanisms as will be describe in latter section , (υ_{sat}) is the saturation velocity , and(β_{sat}) is a constant that controls how abruptly the velocity goes into saturation. Until now, only few temperature dependent high-field data for SiC had been published. The only experimental data comes from Khan and Cooper [44], where the drift velocity in epitaxial 4H SiC (n-doped to about 1.3 x 10^{17} cm-3) was measured as a function of the applied electric field. A fit of Eq.3.17 through the experimental high field data by Khan and Cooper as in Fig.3.17, which resulted in the parameter values as listed in table 3.2.

***Table.3.2**.Parameters of the velocity field Eq. 3.17 for 4H SiC at two temperatures [44].*

Parameter	Temperature	
	23 °C	320 °C
$\mu_{s,n}$	450 cm^2/Vs	130 cm^2/Vs
υ_{sat}	$2.2x10^7$ cm/s	$1.6x10^7$ cm/s
β_{sat}	1.2	2.2

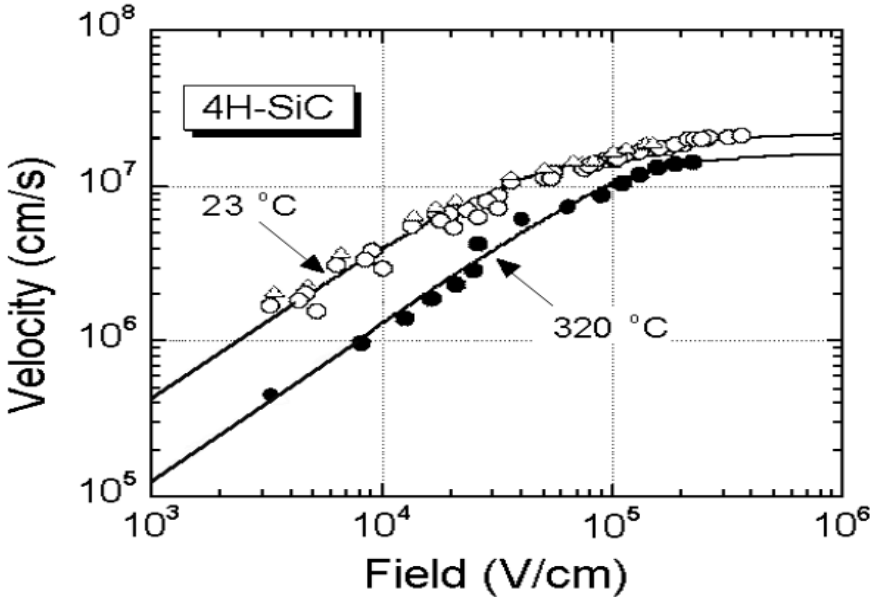


***Figure.3.17:** Drift velocity of electron (at 23 −°C and 320 −°C) in 4H SiC as functions of the applied field. An empirical best fit to these curves as shown in solid lines are generated using Eq. 3.17 with parameter values given in Table 3.2 [44].*

3.3.1.3. Anisotropic Mobility

The polytypes of SiC exhibit anisotropic mobility due to its crystal structure arrangement. This effect is more dominant in the 3C-SiC and 6H-SiC polytypes and less in 4H-SiC [46,47]. For 4H-SiC:

$$\frac{\mu_{n\perp}}{\mu_{n\parallel}} = 0.8 \qquad \textbf{(3.18)}$$

Whereas for 6H-SiC:

$$\frac{\mu_{n\perp}}{\mu_{n\parallel}} = 5.0 \qquad \textbf{(3.19)}$$

Where $\mu_{n\perp}$ denotes the mobility perpendicular to the c-axis [1120] and $\mu_{n\parallel}$ denotes mobility parallel to c-axis [0001]. The high ratio of mobility in 6H-SiC has severe impact in current voltage characteristics of a DMOS device (not discussed in this research). Even though the anisotropic nature of mobility is not very significant in 4H-SiC, it has still been included in the simulation to obtain accurate results. In Silvaco ATLAS, Anisotropic Mobility is included by defining separate MOBILITY statements with separate mobility parameters perpendicular and parallel to c-axis [48].

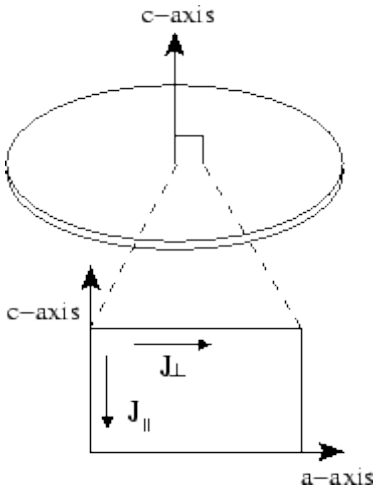


Figure.3.18: *Wafer with surface perpendicular to the c-axis: current transport parallel and vertical to the c-axis.*

The first statement defines the mobility parallel to c-axis and the second statement configures the mobility perpendicular to c-axis by using parameters ***N.ANGLE = 90°*** and ***P.ANGLE = 90°*** [46, 47, 49]. Only the cubic 3C structure has completely isotropic bulk properties. A mong several SiC polytype, 4H- SiC is the most attractive one due to the higher carrier mobility and more isotropic nature of it's properties .

The hexagonal SiC substrates are typically cut perpendicular or offset a few degrees to the c- axis of the crystal .thus one needs to be concerned with the carrier mobility either perpendicular to the c-axis (in direction of the basal of the crystal) or parallel to c- axis, depending on the device structure and operation. In all hexagonal types, the carrier transport properties exhibit an anisotropic behavior with regard to crystallographic orientation in each polytype. The high mobility model expresses the dependence of carrier mobility on the component of electric field that is parallel to the current flow due to anisotropic behavior of SiC material, the effect caused by anisotropic in scattering need to be included in the device model. It is clear that due to the anisotropic nature of

the SiC crystal structure, anisotropic electronic properties should be expected. This means that electrical characteristics will be different depending on the orientation of the device with respect to the crystal. The most commonly used orientation has the wafer surface perpendicular to the c-axis (Fig. 3.18), which means that the current transport is better in the lateral device compared with a vertical device. However, most electrical devices depend on the vertical current transport, since it is easier to manufacture a blocking layer parallel to the surface. It is generally assumed that the semiconductor material is isotropic, which is the case for cubic materials such as Si and GaAs. For SiC and for various nitrides, which generally crystallize in structures of symmetry lower than cubic (except for 3C-SiC), a rigorous model implementation in device simulation programs must account for the anisotropic properties.

The anisotropic characteristics of the Hall mobilities have been investigated independently using epitaxial layers grown on [1100] and [1120] surfaces. The results for N-doped (n-type) and Al-doped (p-type) 4H-SiC can be expressed as similarly for 6H-SiC, for directions orthogonal ($\perp$) and parallel ($\parallel$) to the hexagonal c-axis. Thus, the largest Hall mobility is related to a current flow parallel to the c-axis in 4H-SiC and perpendicular to the c-axis in 6H-SiC. No dependence on the impurity concentration has been reported for these ratios. On the other hand, a rather large dependence on temperature for these ratios has been reported.

3.4 Silicon Carbide Power MOSFETs

The first MOSFETs in SiC were reported in late 1980s and the first power MOSFETs was in 1994. SiC power MOSFETs are attractive because of their low on-resistance, high blocking voltage capability, and high switching speed compared to Si-based power devices. In a power MOSFET, the blocking voltage can be a achieved by the separation of source and drain (i.e. thickness of the drift region). Higher blocking capability means high drift region resistance, which increases the ON state voltage and power losses. And thus the drift region resistance is considered to reach the minimum possible theoretical limit for the on-resistance of a MOSFET. The power MOSFET is determined by the drift region only. Power MOSFETs are inherently capable of operating at very high frequencies compared to bipolar power switches like the BJT, due to absence of minority carrier transport. Also, high input impedance greatly simplifies the gate drive circuitry.

The ability to function under extreme high temperature, high power, and high radiation environments. Power MOSFETs are switches which have the ability to produce large on currents during the on-state and can support large breakdown voltages during the off state. And it also can be considered as a heart of all power electronic systems. The increased power capabilities, ease of control, and reduced costs of power switches have made power electronic systems affordable in a large number of applications. The first power switches were thyristors and bipolar transistors developed in 1950's.thyristors were used in higher power systems because their ratings were scaled at faster pace than bipolar transistors .Bipolar transistors were favored for low and medium power applications because of their faster switching capability .The ratings of these grew steadily until the late 1970's, the year in which the first power MOSFETs were introduced [50] . since the introduction of the first power MOSFETs Si power MOSFETs have been immensely improved and have become the dominant device technology since 1980s for many applications for many reasons .first MOSFET has a very high input impedance and due to it's MOS gate structure provides the simplest gate drive requirements .The creation of either inversion layers or accumulation layers under the MOS channel can be controlled using integrated circuits because of the small gate current that is required to charge and discharge the high input gate capacitance. Second, MOSFET is a majority carrier device hence there is no minority charge storage involved in its operation. Switching time for the MOSFET is dictated by the ability to charge and discharge the input capacitance. No storage time is encountered and current rise and fall times can be very rapid. This results in faster switching operation. Third, compared to bipolar transistors the MOSFETs has superior ruggedness and forward biased safe operating area (FBSOA) which allows elimination of snubber circuits for protection of the switch during operation in typical hard-switching applications. Fourth, as the majority carriers in silicon exhibits increasing resistivity with temperature, the thermal runaway behavior is avoided in MOSFETs.

Due to these excellent electrical characteristics, it would be desirable to utilize power MOSFETs for high voltage/power electronic applications. However, the blocking voltage capability of the MOSFET is based on the ratings of the reverse body diode of the drift region. This blocking voltage is determined in part by the distance from source to drain.High blocking voltage capability implies high resistance because of the geometry, so there is trade off between low drift region resistance, R_{on}-drift, values and

device voltage capability. This trade off between low on-state resistance and the device voltage capability prevents its advantages in high voltage/power electronic applications. The Power MOSFETs that are available today perform the same function as bipolar transistors except the former are voltage controlled in contrast to the current controlled bipolar devices. Today MOSFETs owe their ever-increasing popularity to their high input impedance and to the fact that being a majority carrier device, they do not suffer from minority carrier storage time effects, thermal runaway, or second breakdown. The breakdown electric field of SiC is approximately eight times higher than in silicon. This makes it possible to design power switching devices having correspondingly higher blocking voltages than their silicon counterparts. Unipolar SiC devices can operate at much higher switching frequency with lower switching losses, at higher temperatures , More importantly, the specific on-resistance (i.e. resistance area product) of a power device scales inversely as the cube of the breakdown field, so the on-resistance of SiC power MOSFETs are 100-200 times lower than comparable devices in silicon.

3.4.1. Types of Power MOSFET

The power devices were the vertical trench MOSFETs a Vertical Channel Structure The drain and the source are placed in the opposite side of the wafer, and it is suitable for a power device as more space could be used as source region, and as the length between the source region and the drain region is reduced, it is possible to increase the drain-to-source current rating, and it could also increase voltage blocking capability by growing the epitaxial layer (drain drift region). Or UMOSFETs. UMOSFETs are attractive because the base and source regions are formed epitaxially without the need for ion implantation and associated high temperature annealing. In UMOSFETs, the MOS channel is formed on the sidewalls of trenches created by RIE. However, SiC UMOSFETs have been reported to have two serious problems:

a) a high electric field occurs in the gate oxide caused by higher electric fields in the SiC drift region. This problem occurs at the trench corners leading to catastrophic failure of the gate oxide at higher drain voltages, thus restricting the maximum operating voltage to less than 40% of ideal breakdown voltage.

b) The low inversion layer mobility along the trench sidewalls results in high specific on resistance, which nullifies the advantage of low drift region in SiC. By 1995,

UMOSFETs fabricated on the carbon face of SiC had achieved the breakdown voltage of about 260V.

3.4.1.1. DIMOSFET

The first commercialized structure was V- groove structure at the gate region. As shown in Fig. 3.19.

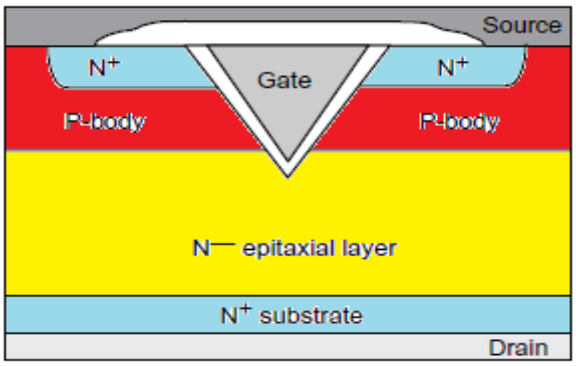


Figure 3.19: *structure of VMOSFET*

This VMOSFET structure was pushed out by the DMOSFET structure_figure (3.20) .The first SiC DMOS power transistors were developed in 1996 [51,52] These devices exhibited blocking voltages in excess of 760V. It has double-diffusion structure having P-base region and N+ source region, and it is the most commercially successful structure. The vertical power devices are composed of two parts: the top one creates the function and the bottom one called the drift layer permits to spread the equipotent lines when the chip is blocked and induces the majority of the chip's resistance. A positive bias on the poly- silicon gate creates a surface inversion layer at the interface between the Sio_2 and the P-type SiC .electronic flow from the N^+ source along the inversion layer to the N- drift region .Upon reaching the drift region, electrons flow vertically to the N^+ drain at the bottom . The thick› lightly doped N-drift region is needed for large drain voltage when the device is in the off state (gate at ground).

In order to reach higher breakdown voltage (V_{BR}), one must increase the drift layer's thickness and lower its doping level. With Si, building device with high voltage blocking capability above 1.2kV requires thick drift layers with very low doping inducing a major resistance. Using unipolar SiC devices the superior critical field of SiC permits to use a far thinner drift layer of higher doping concentration and thus greatly reduces the drift resistance's contribution.

Since then the SiC VMOS device has been revolutionizing the power electronic technology. Thanks to the progresses in all the SiC fabrication steps, CREE and RHOM are now capable to produce and commercialize them. The table 3.3 summarizes the different VMOS devices available commercially.

Table 3.3: *commercially available SiC VMOS*

Provider	V_{BR}	Current	Year
Cree	1200V	24-33A	2011
RHOM	600V	10A	21/12/2010
	1200V	20A	2011

The major challenge with the VMOS integration on SiC is to obtain an inversion channel of good quality. This channel is created by the inversion of the p-type area under the gate when positively biased. Typically, the SiC/SiO_2 interface is worst than with Si. Many years of worldwide investigation have permitted to identify certain sources of the degradation and find solutions.

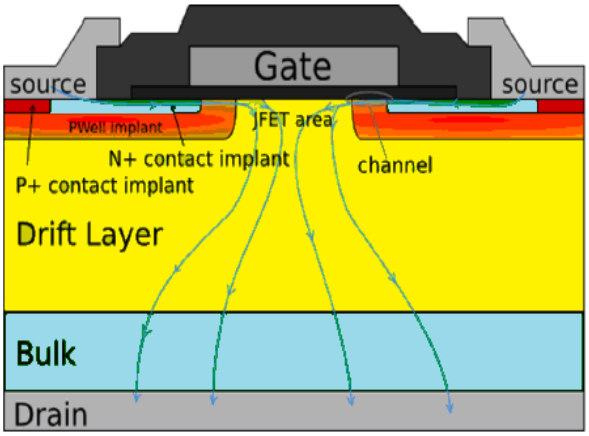


Figure. 3.20: *structure of DMOSFET*

Another issue comes from the creation of p-well, as the diffusion of impurities in the SiC is impossible and impractical in SiC because of the very low diffusion coefficients at any temperature, so the base and source regions are formed by selective ion implantation using aluminum or boron for the p-type base and nitrogen for n+ source.

Because p-type implants are conducted at temperatures between 1600 and 1700 ^{O}C, The simplest solution is to use implantation to selectively dope areas and especially the p-well; this process creates surface crystal defects that will later deteriorate the channel's quality. So Until now, the fabrication on SiC of vertical MOSFETs (VMOS) was a major objective for all the SiC players.

3.4.1.2. UMOSFET

As shown in Fig. 3.21 (c), this structure has U-groove at the gate region. This structure has higher channel density so that it can reduce on-resistance compared to the VMOSFET and the DMOSFET. UMOSFET structure using trench etching technique was commercialized in 1990s.The UMOSFET is formed by reactive ion etching, and the substrate acts as the drain electrode. The p-type base layer is grown by epitaxy and is grounded. In UMOSFETs the maximum blocking voltage depends on oxide breakdown and not on the semiconductor breakdown. [53]. the electric fields in the blocking state (transistor off) the electric field in the oxide at the bottom of the trench is higher than the peak field in the semiconductor, which leads to catastrophic breakdown of the oxide. This oxide breakdown problem represents a major limitation to the UMOSFET structure in SiC. And it can be solved by integrated oxide protection.

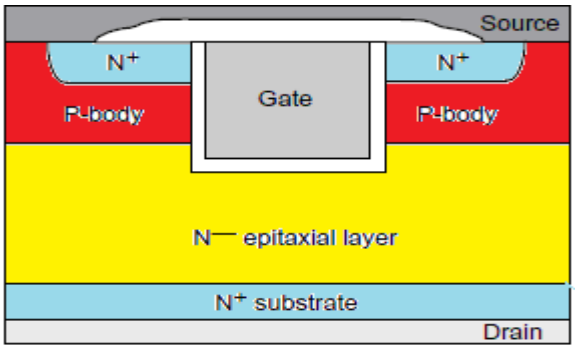


Figure .3.21: *structure of UMOSFET*

3.4.1.3. Lateral or LDMOSFET

Lateral n-MOSFETs test devices made on the same wafer as the VMOS have been implemented with the same channel properties and processes. And it is suitable for the integration but not for obtaining high power ratings as the length between the source region and the drain region must be far away from each other to obtain better voltage

blocking capability, and as the drain-to-source current is inversely proportional to the length. In order to overcome the limitations of vertical-type MOSFETs we use the lateral type MOSFET. The structure of lateral DMOSFET is shown in Figure 3.22 in then the depletion layer spreads mainly into the lightly-doped drift region. Once the depletion region reaches the insulating substrate, it continues spreading toward the drain. Here, the maximum voltage is not limited by the thickness of the layer [54]... As in the of vertical devices, the drift region component of the total LDMOST specific on resistance depends on its dimensions and doping concentration.

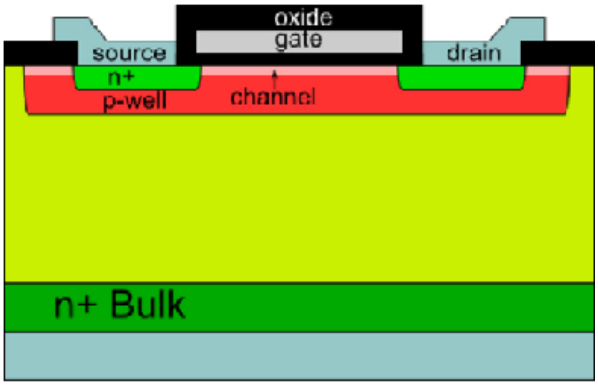


Figure.3.22: *structure of lateral LDMOSFET*

3.5. Material Advantage of 4H-SiC for unipolar Power Devices

The major difference in the device structure of the power MOSFETs from the conventional lateral MOSFETs is the presence of low doped and thick layer of drift region at the drain. The drift layer has been introduced in power MOSFETs to support a large blocking voltage when the device is in OFF state. At ON state, current has to flow through the channel and drift region. The drift region resistance is one of the major parts of the MOSFET on-resistance. Therefore, drift region resistance plays a dominant role in the ON state voltage drop. If we neglect the resistance associated with the ohmic contacts and the JFET region, the specific on-resistance, *Ron-sp*, in any standard power MOSFET can be expressed as,

$$R_{on-sp} = R_{channel} + R_{drift} \qquad \textbf{(3.20)}$$

In case of ideal MOSFET, $R_{on\text{-}sp}=R_{drift}$, therefore, the specific on-resistance, $R_{on\text{-}sp}$, and the blocking voltage capability of a power MOSFET can be related to the doping level and

the thickness of the drift region analysis. By approximating the depletion layer spread over the uniformly doped drift region as an abrupt junction formed with the *p*-body regions, the doping level N_B of the drift region required to support a given breakdown voltage V_B and depletion width W_D can be calculated as follows [55]:

$$N_B = \frac{\varepsilon_r E_c^2}{2qV_B} \tag{3.21}$$

$$W_B = \frac{2V_B}{E_c} \tag{3.22}$$

The specific on-resistance associated with the drift layer to support *VB* is

$$R_{on-drift} = \frac{W_D}{qN_B\mu_{bulk}} \tag{3.23}$$

$$= \frac{4V_B^2}{\varepsilon_r E_c^3 \mu_{bulk}} \tag{3.24}$$

Where ε_r is the relative permittivity of the semiconductor, μ_{bulk} is the drift region mobility ,E_C is the critical electric field of the semiconductor, and V_B is the blocking voltage. The denominator term $(\varepsilon_\mu E^3_C)$ has been defined as Beluga's Figure of Merit (BFOM). This Figure of Merit can be used to compare the relative performance of the various semiconductor materials for power device fabrication [56].

The mobility of electron in the inversion layer as well as in the bulk and the breakdown electric field depend on doping concentration, *NB*. In Si, the well-known empirical relationship describing the dependency of the electron mobility and the breakdown field on the doping concentration can be expressed as [57]:

$$\mu_n = \frac{5.10x10^{18} + 92N_B^{0.91}}{3.75x10^{15} + N_B^{0.91}} \tag{3.25}$$

The relationship between the drift layer width and breakdown voltage can be expressed as [58]:

$$N_B = 2.01x10^{18} V_B^{-1.33} \quad \textbf{(3.26)}$$

$$W_D = 2.58x10^{-6} V_B^{1.167} \quad \textbf{(3.27)}$$

Substituting Eq. 3.21 and Eq. 3.22 in Eq. 3.10 and using room temperature mobility at low doping levels, *Ron-drift* for Si can be expressed as:

$$R_{on-drift} = 5.98x10^{-9} V_B^{2.5} \quad \textbf{(3.28)}$$

For 4H-SiC, the dependency of μ_n on N_B at room temperature can be described as:

$$\mu_n = \frac{1.28x10^{16} + 40N_B^{0.76}}{1.41x10^{13} + N_B^{0.76}} \quad \textbf{(3.29)}$$

Table. 3.4: *Values of Doping Concentration, Electron Mobility, Drift Layer Thickness and Specific On-Resistance as a Function of Breakdown Voltage*

Breakdown Voltage, V_B (V)	Doping Concentration, N_B (cm^{-3})	Electron Mobility, μ_n ($cm^2/V{\cdot}s$)	Thickness, W_D (μm)	Specific On-Resistance, R_{on-sp} ($\Omega{\cdot}cm^2$)
4H-SiC				
200	$3.74x10^{17}$	388	0.75	3.23e-6
500	$1.04x10^{17}$	606	2.26	2.24e-5
1000	$3.93x10^{16}$	745	5.19	1.11e-4
5000	$4.13x10^{15}$	905	35	6e-3
10000	$1.57x10^{15}$	928	82	3.5e-2
Silicon				
200	$1.72x10^{15}$	1351	12.48	3.35e-3
500	$5.06x10^{14}$	1356	36	3.3e-2
1000	$2.01x10^{14}$	1357	82	1.88e-1
5000	$1.84x10^{13}$	1359	659	10.48

Using the Eqs. (3.25-3.29), the drift region analysis for an ideal MOSFET can be performed in terms of the drift region: thickness, doping concentration, mobility, and specific on resistance as a function of breakdown voltage. Table.3.4 provides calculated

values of N_B, W_D, μ_n, and $R_{on\text{-}sp}$ of an ideal power MOSFET on Si and 4H-SiC as a function of breakdown voltage.

SiC has a high critical electric breakdown field (1.5- 4x10^6). From the data in Table.3.4, it is clear that a much higher doping level can be achieved and device layer can be made thinner in SiC MOSFET than that of Si power MOSFET for the same breakdown voltage rating. SiC devices exhibit smaller on- resistance, which reduces the conduction losses and results in higher efficiency. Due to the high breakdown field, high voltage rated power devices can be fabricated in SiC.

3.6 - 4H-SiC DIMOSFET (Introduction)

The Double Implanted Metal-Oxide Semiconductor (DIMOS) field effect transistor has been frequently used in high voltage power electronics applications. Power switching devices are reaching the upper limits imposed by low breakdown field of silicon, and high breakdown voltage can be achieved only using a semiconductor with a higher breakdown field. SiC is unique among compound semiconductors since its native oxide is SiO_2,(the same oxide as of silicon). This means that power devices used in silicon can all be fabricated in SiC. DMOS transistors are common in silicon power device technology where the p-base and n^+ source regions are formed by diffusion of impurities through a common mask opening.

3.6.1 DIMOS Structure for Modeling

An analytical model for a DIMOS field effect transistor is developed using 4H-SiC material. The model is developed based on the methodology for a vertical double diffusion MOS model.

The DIMOS structure is fabricated by using a planar diffusion technology with a refractory gate such as poly – silicon. In these devices, the phase and N^+- source regions are diffused through a common window defined by the edge of the poly silicon gate. The surface channel region is defined by the difference in the lateral diffusion between the P-base and N^+ –source region. The forward blocking capability is achieved by the PN-junction between the P-base region and the N^+- drift region. During the device operation, a fixed potential to the P-base region is established by connecting it to the source metal by a break in the – source region. Short circuiting the gate to the source

and applying a positive bias to the drain ,the P-base / N^+ -drift region junction becomes reversed biased and this junction supports the drain voltage by the extension of a depletion layer extending primarily into the N^+ - drift region . Applying a positive bias to the gate electrode, a conductive path extending between the N^+ - drift region is formed. The detail of DIMOS structure identifying different regions of operation is shown in Fig. 3.23. With the following notation:

h : drift-region height of the device (cm)(depends on Vb and doping profile),

W: width of t he device (cm),

W_j : height of the p-body (cm),

W_t : total vertical height (cm),

W_d : depletion width (cm),

L : channel length formed under the gate and inside the p-body(cm),

L_p: length of p-body (cm),

L : diff separation of p-bodies (cm),

Z : total length of the device (cm),

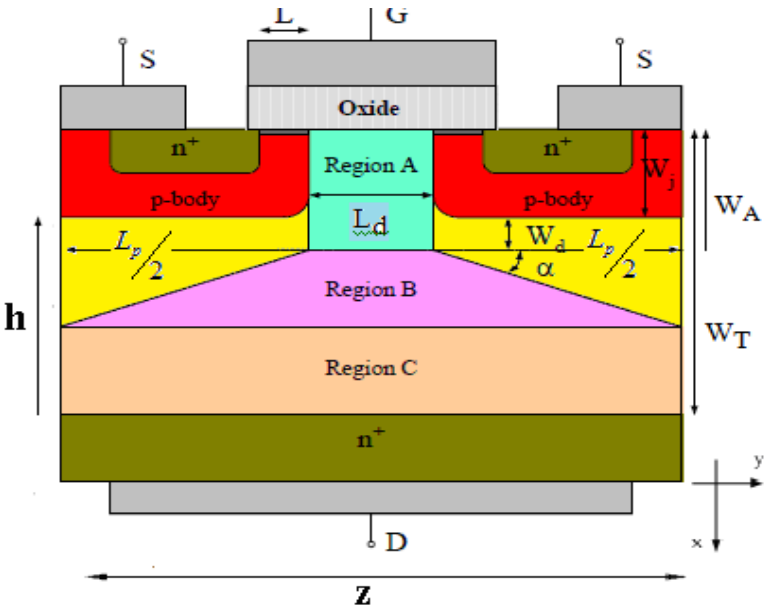


Figure.3.23: *DIMOS structure*

t_{ox} : oxide thickness (cm),

V_T : threshold voltage of the device (volt),

V_{GS} : applied gate to source voltage (volt),

V_{sat} : saturation velocity (cm/sec),

q : Electronic charge (C),

α : angle of slope oft he drift region narrowing (degree),

ε_o : permittivity constant in free space (F/cm),

ε_{ox} : oxide permittivity (F/cm).

ε_{sic} : silicon carbide permittivity (F/cm),

A : cross-sectional area of the device (cm2), and

C_{ox} : oxide capacitance (F).

The drift region is divided into three parts: an accumulation region- A, a drift region- B with a varying cross-section (area), and a drift region-C with constant cross-section. The corresponding voltages to these regions are V_A, V_B, and V_C for regions A, B, and C, respectively and they are given by the following expression [59].

Total drift region voltage is the sum of the voltages of three regions,

$$V_{drift} = V_A + V_B + V_C \tag{3.30}$$

Where :

The starting point is drain current expression that takes into account velocity saturation:

$$I_D = \frac{qN_D \mu . W . L_d}{1 + \frac{1}{E_c}\left(+\frac{dV}{dx}\right)} \cdot \left(+\frac{dV}{dx}\right) \tag{3.31}$$

(the sign (+) reminds of the fact that the x-axis direction of the current flow).

Relation (3.31) implies : $0 \le t \le W_A$ **A – region:**

$$I_D + \frac{I_D}{E_C} \cdot \frac{dv}{dx} = + qN_D \, \mu W L_d \cdot \frac{dv}{dx} \Rightarrow$$

$$+\frac{dv}{dx} = \frac{I_D}{qN_D \mu W L_d - \frac{I_D}{E_C}} \Rightarrow dv = \frac{I_D \, . \, dx}{qN_D \mu W L_d - \frac{I_D}{E_C}} \tag{3.32}$$

Having on mind that I_D remains constant along x-axis the integration of relation (3.32) because straightforward:

$$V_A = \frac{I_D}{qN_D\mu WL_d - \frac{I_D}{E_C}} \int_0^{W_A} dx \quad \Rightarrow$$

$$V_A = \frac{I_D \ W_A}{qN_D\mu L_d - \frac{I_D}{E_C}} \qquad \textbf{(3.33)}$$

Along **B -region** the situation is not so simple because cross- section is not constant.

$$I_D = \frac{qN_D\mu W\left[L_d + 2(x - W_A)ctg\alpha\right]}{1 + \frac{1}{E_C}\cdot\frac{dv}{dx}} \cdot \frac{dV}{dx} \Rightarrow$$

$$\Rightarrow dV = \frac{I_D . dx}{qN_D\mu W\left[L_d + 2(x - W_A)ctg\alpha\right] - \frac{I_D}{E_C}}$$

$$V_B = \int_{W_A}^{W_A + \frac{1}{2}L_p tg\alpha} \frac{I_D . dx}{qN_D\mu W\left[L_d + 2(x - W_A)ctg\alpha\right] - \frac{I_D}{E_c}}$$

$$= \frac{I_D}{2qN_D\mu Wctg\alpha} \ln \left\{ qN_D \ \mu W\left[L_d + 2(x - W_A)ctg\alpha\right] - \frac{I_D}{E_C} \right\}_{W_A}^{W_A + \frac{1}{2}L_p tg\alpha}$$

$$= \frac{I_D}{2qN_D\mu Wctg\alpha} \ln \frac{qN_D\mu W\left(L_d + L_p\right) - I_D / E_c}{qN_D WL_d - I_D / E_c}$$

$$V_B = \ = \frac{I_D}{2qN_D\mu Wctg\alpha} \ln \frac{qN_D\mu W\left(L_d + L_p\right) - I_D / E_c}{qN_D WL_d - I_D / E_c} \qquad \textbf{(3.34)}$$

In **C- region** the cross section is constant again:

$$I_D = \frac{qWN_D \ \mu\left(L_d + L_p\right)}{1 + \frac{1}{E_c}\cdot\frac{dv}{dx}} \cdot \frac{dV}{dx} \quad \Rightarrow$$

$$dV = \frac{I_D}{qWN_D\mu\left(L_d + L_p\right) - \frac{I_D}{E_C}} . dx$$

$$V_C = \frac{I_D}{qWN_D\mu(L_d + L_P) - \frac{I_D}{E_C}} \int_{W_A+\frac{1}{2}L_p tg\alpha}^{W_T} dx \quad \Rightarrow$$

$$V_C = \frac{I_D \cdot \left(W_T - W_A - \frac{1}{2}L_P tg\alpha\right)}{qWN_D\mu(L_d + L_P) - \frac{I_D}{E_C}} \qquad \textbf{(3.35)}$$

The denominator of equation (3.35) doesn't have any singularity

$qWN_D\mu(L_d + L_P) - \frac{I_D}{E_C} > 0$ because $I_D < qWN_D\mu L_d . E_C$

Where:

W_j : is the depth of n+ contact region,

W_d : is the depth of depletion region,

W_t : is the total thickness of epilayer,

L_S : is th e length of accumulation region, and

L_p : is the length of p-body.

The current/voltage characteristic in the triode region is given by Eq.

$$I_{ch} = \frac{W\mu_n}{2L\left[1+(\mu_n/2V_{satL})V_{ch}\right]} V_{ch}\left[2C_{ox}(V_{GS} - V_T) - (C_{ox} + C_{do})V_{ch}\right] \qquad \textbf{(3.36)}$$

The proposed device structure and the device dimensions are selected in such a way that a practical device can be built on the basis of currently available SiC technology [59].

3.6.2. MOS Physics

When a P-type semiconductor region is assumed, then the analysis of current transport in the n channel power MOS will be applicable. In this analysis, the oxide layer is assumed to be a perfect insulator that doesn't allow any charge carrier between gate and semiconductor. The energy band diagrams for an ideal MOS structure is with a P-type semiconductor for different bias potential at metal is shown in Fig3.24. The change in the inversion region plays a key role for determination of current transport in MOSFET devices. Here the ideal MOSFET has the Following properties:

a) The insulator has infinite resistivity,

b) Charge can exist only in semiconductor and on the metal electrode,

c) There is no energy difference between the work function of the metal and the semiconductor.

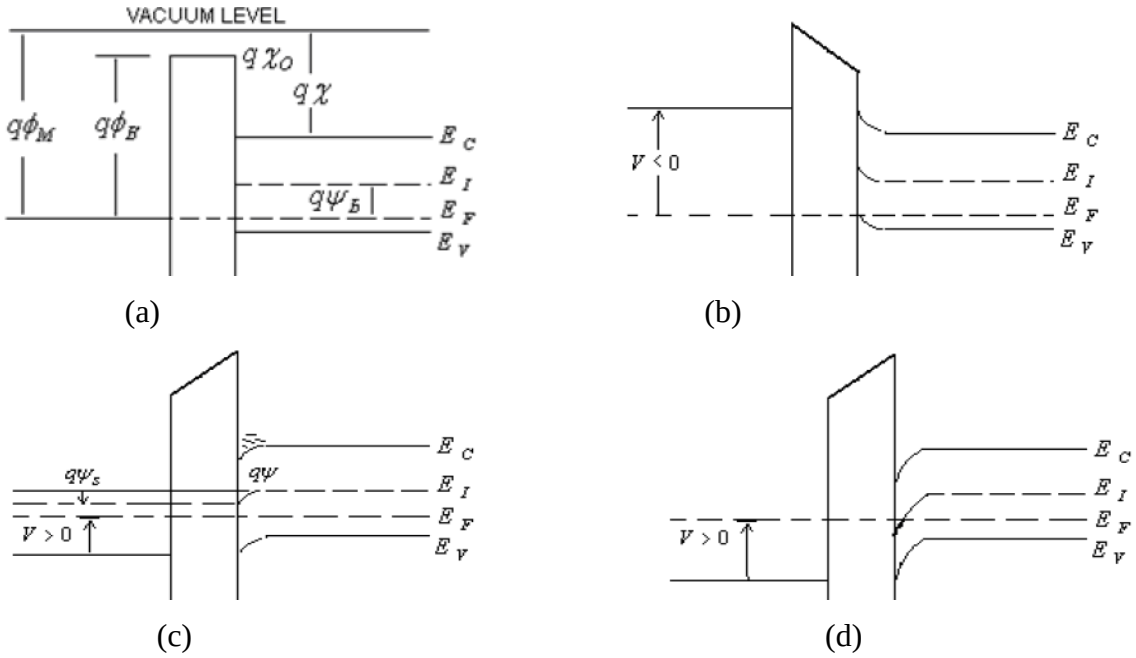


Figure.3.24: *MOS structure with P- type semiconductor under different region (a) flat band energy band diagram (zero gate voltage) , (b) accumulation (negative gate voltage), (c)depletion (positive gate voltage),(d) inversion (positive gate voltage) [56].*

3.6.3. Forward Conduction Characteristics

The current flow in the power DIMOS during forward conduction is achieved applying positive gate bias voltage for N-channel device to create the conductive path. This flow is limited by the total resistance between source and drain. This consists of several components as shown below in Fig.32.5. Where R_N is the contribution from then+-sources diffusion region, CR is the channel resistance, R_A is the accumulation layer resistance ,R_D is the drift region resistance and ,R_S is the substrate resistance and the portion of the drift region that comes to the upper surface between cells contributes R_J that is enhanced at high drain voltage due to pinch – off action of depletion layer extending from the P-base regions. This phenomenon is called JFET action.

3.6.4. Basic Device Equations

3.6.4.1. On Resistance

The on resistance of a power MOSFET is the total resistance between the source and drain terminals during the on-state [60]. It is the important device parameter because it determines the maximum current rating. DIMOS cell structure with each components of the specific on – resistance is shown below in Fig. 3.25. The application of a positive drain voltage results in a current flow between drain and source through the N-drift region and conductive channel. For an ideal DIMOSFET, the resistances associated with the n^+-source, the n^-channel, the accumulation region and the n^+- substrate are usually neglected and the specific on-resistance of the power MOSFET is determined by the drift region alone.

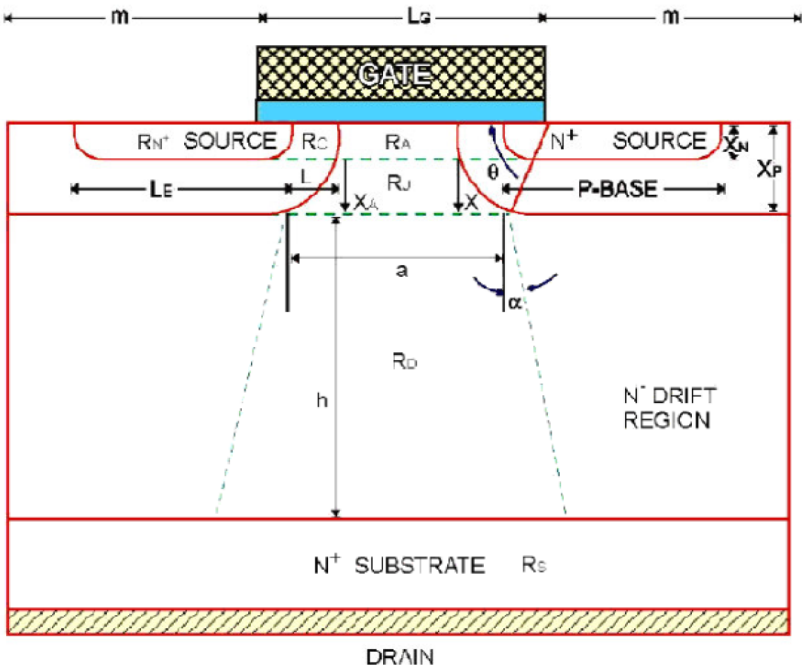


Figure. 3.25: *DIMOS cell structure [62]*

In a power MOSFET, the blocking voltage appears across the drift layer and so the drift-region resistance is considered to be the minimum possible theoretical value for the on-resistance of a MOSFET.

The total specific on-resistance [61] is determined as:

$$R_{on\text{-}sp} = R_n + R_C + R_A + R_J + R_D + R_S \qquad \textbf{(3.37)}$$

Where

$R_{on\text{-}sp}$: is the specific on-resistance,

R_{n+} : is the contribution from the n+ -source,

R_C : is the channel resistance,

R_A : is the accumulation layer resistance,

R_J : is the resistance from the drift region between the p-base regions by virtue of the JFET pinch off action,

R_D : is the drift region resistance and RS is the substrate resistance.

The powers MOSFETs have different structure than the lateral MOSFETs as with all power devices, their structure is vertical and not planar structure. in a planner structure, the current and breakdown voltage ratings are both functions of the channel dimensions (respectively width and length of the channel), resulting in inefficient use of the silicon estate with a vertical structure, the voltage rating of the transistor is a function of the doping and thickness of the N epitaxial layer, while the current rating is a function of the channel width. This makes possible for the transistor to sustain both high blocking voltage and high current within a compact piece of silicon. SiC has been projected to have tremendous potential for high voltage solid state power devices with very high voltage and current ratings because of its high electric breakdown field of 1.5 - 4×10^6 V/cm and high thermal conductivity of 2.3 - 4W/cmK, depending on the doping level [63] .

1- The channel resistances and drift are considered as the major contribution to the specific on-resistance in any standard power MOSFET. The channel resistance per square centimeter for linear cell structure having gate oxide thickness is [64] .

$$R_{ch,sp} = \frac{1}{2}\frac{L(L_G + 2m)}{\mu_{ns} C_{ox}(V_G - V_T)} \qquad \textbf{(3.38)}$$

With following notation:

L : is typical channel length

L_G : is the length of the gate electrode,

m : is the cell diffusion window,

V_G : is the gate drive voltage (10V),

C_{OX} : is the oxide capacitance, and

V_T : is the threshold voltage.

It can be reduced by reducing the gate oxide thickness.

2- To calculate the **sources resistance**, if a linear cell is considered with 1-cm extension perpendicular to the cross section as shown above in Fig.3.23, the source resistance per square centimeter due to N-emitter region is given by:

$$R_{n^+,sp} = \frac{1}{2}\rho_{n^+} L_E (L_G + 2m) \qquad \textbf{(3.39)}$$

Where, L_G is the length of the gate electrode,

$\rho_{n+}$is the sheet resistance of then diffusion,

2m is the cell diffusion window,

L_E is the emitter length and

(L_G + 2m) is the cell repeat spacing.

It is negligible compared to all other resistances.

3- The **accumulation region resistance** determines the current flow from the channel into the drift region. The accumulation region resistance per square centimeter is:

$$R_{A,sp} = \frac{K(L_G - 2x_p)(L_G + 2m)}{\mu_{nA} C_{ox} (V_G - V_T)} \qquad \textbf{(3.40)}$$

Where, K is the multiplying factor (3 nearly) ,

C_{OX} : Oxide capacitance per unit area, and

V_T : is the threshold voltage.

4- Similarly JFET region resistance is given by the expression

$$R_{J,sp} = 2\rho_D (L_G + 2m)\left[\frac{1}{\sqrt{1-(2x_p/L_G)^2}} \tan^{-1}(0.414)\sqrt{\frac{L_G + 2x_p}{L_G - 2x_p}} - \frac{\pi}{8}\right] \qquad \textbf{(3.41)}$$

Where, ρ_D is the resistivity of the drift region.

5- The **drift region resistance** per unit square centimeter is given by

$$R_{D,sp} = \rho_D \frac{(L_G + 2m)}{\tan(\alpha)} \ln\left[1 + 2\frac{h}{a}\tan(\alpha)\right] \quad \textbf{(3.42)}$$

Current spreading angle:

$$\alpha = 28^0 - \left(\frac{h}{a}\right) \qquad \text{if h} \geq \text{a}$$

$$\alpha = 28^0 - \left(\frac{a}{h}\right) \qquad \text{if h} \leq \text{a}$$

Where h is the drift region thickness (≈ a) so the ratio (h/a) = 1

The drift region resistance is largest if compared to any other resistances so only the drift region resistance will be considerable.

3.6.4.2. Current Equation

The current/voltage characteristic in the triode region is given by Eq.

$$I_{dh} = \frac{W\mu_n}{2L\left[1 + (\mu_n / 2V_{satL})V_{dh}\right]} V_{dh}\left[2C_{ox}(V_{GS} - V_T) - (C_{ox} + C_{do})V_{dh}\right] \quad \textbf{(3.43)}$$

where W is the channel width, L is the channel length, V_{ch} is the channel voltage, V_T is the threshold voltage, V_{GS} is the gate voltage, C_{ox} is the oxide capacitance, C_{do} is the body depletion capacitance, μ_n is the electron mobility, v_{sat} is the electron saturation velocity.

3.7.References

[1] G. Moore, "Cramming more components onto integrated circuits", *Electronics*, Vol. 38, No. 8, p. 114, 1965

[2] T. Sakata, M. Horiguchi, T. Sekiguchi, S. Ueda, H. Tanaka, E. Yamasaki, Y.Nakagome, M. Aoki, T. Kaga, M. Ohkura, R. Nagai, F. Murai, T. Tanaka, S. Iijima, N.Yokoyama, Y. Gotoh, I. Shoji, T. Kisu, H. Yamashita, T. Nishida, and E. Takeda, "An experimental 220-MHz 1-Gb DRAM with a distributed-column-control architecture", *IEEE Journal of Solid-State Circuits*, Vol. 30, No. 11, p. 1165, 1995

[3] D. Kahng and .M. Atalla, "Silicon-silicon dioxide field induced surface devices", *IRE Solid-State Device Research Conference*, Carnegie Institute of Technology, Pittsburg, 1960

[4] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed. USA: John Willey & Sons, Inc., 2003.

[5] MOSFET Basics By Vrej Barkhordarian, International Rectifier, El Segundo, Ca

[6] Z. M. LI, P. A. MAWBY, and K. BOARD, "A physical insight into the quasi-saturation effect in VDMOS power transistors," *International Journal of Electronics*, vol. 83, no. 1,pp. 13 – 22, July 1997.

[7] J. Rebollo, E. Figueras, J. Milln, E. Lora-Tamayo, and F. Serra-Mestres, "Analysis of the quasi-saturation region of high voltage VDMOS devices," *Solid-State Electronics*, vol. 30,no. 2, pp. 177–180, February 1987.

[8] C.-K. Park and K. Lee, "Experiments and 2D-simulations for quasi-saturation effect in power VDMOS transistors," in *IEEE International Symposium on Power SemiconductorDevices and ICs*, June 1990, pp. 219–224.

[9] M. N. Darwish, "Study of the quasi-saturation effect in VDMOS transistors," *IEEE Transactionson Electron Devices*, vol. 33, no. 11, pp. 1710– 1716, Nov 1986.

[10] K. H. Lou, C. M. Liu, and J. B. Kuo, "Analysis of the quasi-saturation behavior considering the drain-to-source voltage and cell-spacing effects for a vertical DMOS power transistor," *Solid-State Electronics*, vol. 36, no. 1, pp. 85–91, January 1993.

[11] B. Y. Chen and J. B. Kuo, "An accurate knee current model considering quasi-saturation for BJTs operating at high current density," *Solid-State Electronics*, vol. 38, no. 6, pp.1282–1284, June 1995.

[12] J. S. Yuan andW. R. Eisenstadt, "Circuit modeling of collector current spreading effects in quasi-saturation for advanced bipolar transistors," *Solid-State Electronics*,

vol. 31, no. 12,pp. 1725–1731, December 1988.

[13] A. W. Alden and A. R. Boothroyd, “Modelling of VHF and microwave power transistors operating in quasi-saturation,” *Solid-State Electronics*, vol. 25, no. 8, pp. 723–731, August 1982.

[14] H. C. de Graaff and R. J. van der Wal, “Measurement of the onset of quasi-saturation in bipolar transistors,” *Solid-State Electronics*, vol. 17, no. 11, pp. 1187–1192, Nov 1974.

[15] M. Kumar and K. N. Bhat, “Collector recombination lifetime from the quasi-saturation analysis of high-voltage bipolar transistors,” *IEEE Transactions on Electron Devices*,vol. 37, no. 11, pp. 2395–2398, Nov 1990.

[16] S. Roy and M. Kumar, “Enhanced breakdown voltage, diminished quasi-saturation, and self-heating effects in SOI thin-film bipolar transistors for improved reliability: a TCAD simulation study,” *IEEE Transactions on Device and Materials Reliability*, vol. 6, no. 2,pp. 306– 314, June 2006.

[17] C. Anghel, N. Hefyene, A. Ionescu, M. Vermandel, B. Bakeroot, J. Doutreloigne,R. Gillon, S. Frere, C. Maier, and Y. Mourier, “Investigations and Physical Modelling of Saturation Effects in Lateral DMOS Transistor Architectures Based on the Concept of Intrinsic Drain Voltage,” in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2001, pp. 399 – 402.

[18] J. Zeng, P. A. Mawby, M. S. Towers, and K. Board, “Numerical analysis of a trench VDMOST structure with no quasi-saturation,” *Solid-State Electronics*, vol. 38, no. 4, pp.821–828, April 1995.

[19] L. Su, K. Goodson, D. Antoniadis, M. Flik, and J. Chung, “Measurement and Modeling of Self-Heating Effects in SOI NMOSFETs,” in *IEEE International Electron DevicesMeeting (IEDM)*, 1992, p. 357 360.

[20] G. Wachutka, “Rigorous Thermodynamic Treatment of Heat Generation and Conduction in Semiconductor Device Modelling,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 9, no. 11, p. 1141 1149, 1990.

[21] P. Mautry and J. Trager, “Investigation of Self-Heating in VLSI and ULSI MOSFETs,” in *International Conference on Microelectronic Test Structures (ICMTS)*, March 1990, p.221 226.

[22] J. Jomaah, G. Ghibaudo, and F. Balestra, “Analysis and Modeling of Self-Heating Effects in Thin-Film SOI as a Function of Temperature,” *Solid-State Electronics*,

vol. 38, no. 3,pp. 615–618, 1995.

[23] L. McDaid, S. Hall, P. Mellor, W. Eccleston, and J. Alderman, “Physical Origin of Negative Differential Resistance in SOI Transistors,” *IEE Electronics Letters*, vol. 25, no. 13,p. 827 828, 1989.

[24] C. Anghel, N. Hefyene, R. Gillon, M. Tack, M. Declercq, and A. Ionescu, “New method for temperature-dependent thermal resistance and capacitance accurate extraction in highvoltage DMOS transistors,” in *IEEE International Electron Devices Meeting (IEDM)*,Dec. 2003, pp. 5.6.1 – 5.6.4.

[25] C. Anghel, R. Gillon, and A. Ionescu, “Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs,” *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 141 – 143, March 2004.

[26] C. Anghel, “High voltage devices for standard MOS technologies : characterisation and modelling,” Ph.D. dissertation, EPFL, 2004, thesis No. 3116.

[27] Y. Tsivids, “,” in *Operation and Modeling of The MOS Transistor*. McGraw-Hill, 1999.

[28] G. Cao, S. Manhas, E. Narayanan, M. D. Souza, and D. Hinchley, “Comparative study of drift region designs in RF LDMOSFETs,” *IEEE Transactions on Electron Devices*,vol. 51, no. 8, pp. 1296– 1303, Aug. 2004.

[29] B. J. Baliga, *Silicon Carbide Power Devices*, (World Scientific, 2005).

[30] J. A. Cooper Jr. and A. Agarwal, *Proceedings of the IEEE* **90**, 956 (2002).

[31] S. Dhar, S. Wang, J. R. Williams, S. T. Pantelides, and L. C. Feldman, *MRS Bulletin* **30**, 288 (2005).

[32] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, Robert A. Weller, S. T. Pantelides, Leonard C. Feldman, Member,O. W. Holland, M. K. Das, and John W. Palmour, *IEEE Elec. Dev. Lett.* **22**, 176 (2001).

[33] J. Senzaki, K. Kojima, S. Harada, R. Kosugi, S. Senzaki, and K. Fukuda, *IEEE Elec. Dev. Lett.* **23**,13 (2002).

[34] S. Nishino, H. Suhara, H. Ono, and H. Matsunami, epitaxial growth and electric characteristics of cubic SiC on silicon ‧, J. Appl. Phys., vol. 61, p. 4889, 1981.

[35] T. Tachibana, H. S. Kong, Y. C. Wang, and R. F. Davis, wall measurements as a function of temperature on monocrystalline SiC thin films ‧, J. Appl. Phys., vol. 67, p. 6375, 1990.

[36] C. T. Sah, T. H. Ning, and L. L. Tschopp, the scattering of electrons by surface oxide charges and lattice vibrations at the silicon-silicon dioxide interface・, Surf. Sci., vol. 32, p. 561, 1972.

[37] Y. C. Cheng and E. A. Sullivan, elative importance of phonon scattering to carrier mobility in Si surface layer at room temperature・, J. Appl. Phys., vol. 44, p. 3619, 1973.

[38] D. M. Caughey and R. E. Thomas, carrier mobilities in silicon empirically related to doping and field・, Proc. of the IEEE, vol. 52, p. 2192, 1967.

[39] S. Nakashima and H. Harima, characterization of structural and electrical properties in SiC by Raman spectroscopy・, in Inst. Phys. Conf. Series, p. 269, (1996).

[40] W. J. Schaffer, G. H. Negley, K. G. Irvine, and J. W. Palmour, conductivity anisotropy in epitaxial 6H and 4H SiC・, in Mat. Res. Soc. Symp. Proc., vols. 339, p. 595, 1994.

[41] C. H. Carter Jr. et al, ・ Progress in SiC: From material growth to commercial device development・, Mat. Sci. Eng., vols. B61-62, p. 1, 1999.

[42] T. Kinoshita, K. M. Itoh, J. Muto, M. Schadt, G. Pensl, and K. Takeda, 鼎alculation of the anisotropy of the Hall mobility in N-type 4H- and 6H-SiC・, Mat. Sci. Forum, vols. 264-268, p. 295, 1998.

[43] M. R. Roschke and F. Schwierz, electron mobility models for 4H, 6H, and 3C SiC・, *IEEE Trans. Elect. Dev., vol. 48, p. 1442, 2001.*

[44] I. A. Khan and J. A. Cooper, Jr., measurement of high-field electron transport in silicon carbide・, IEEE Trans. Elect. Dev., vol. 47, p. 269, 2000.

[45] C. Jacoboni and L. Reggiani, “The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials,” Rev. Mod.Phys., vol. 55, no. 3, pg. 645 (1983)

[46]. Lades, Martin. *Modeling and Simulation of Wide Bandgap Semiconductor Devices: 4H/6H-SiC*.Diss.TechnicalUniversityat Munich, Germany,2000.Web.<http://tumb1.biblio.

[47]. Ayalew, Tesfaye. *SiC Semiconductor Devices Technology, Modeling and Simulation*. Diss. Technical University of Vienna, Vienna, Austria, 2004. Web. <http://www.iue.tuwien.ac.at/phd/ayalew/>.

[48]. Silvaco© "ATLAS User's Manual", January 18, 2012. <http://www.Silvaco.com>

[49]. Lee, Sang-Kwon. *Processing and Characterization of Silicon Carbide (6H- and 4H-SiC) Contacts for High Power and High Temperature Device Applications*. Diss. Royal Institute of Technology, Stockholm, Sweden,2002.

[50] Y. Tarui, Y. Hayashi, and T. Sekigawa, diffusion self-aligned MOST: A new approach for high speed device ･, in Proc. 1st Conf. on Sol. Stat. Dev., Tokyo, 1969, Suppl. to J. Japan. Soc. Appl. Phys., vol. 39, p. 105, 1970.

[51] J.N. shenoy,M. R. Melloch, and J. A .Cooper,jr., High – voltage double- implanted MOS power transistors in 6H-SiC ,IEEE Device Reserch conf., santa Barbara ,CA,june 24-26 ,1996.

[52]] J.N. shenoy , J.A. Cooper, jr., and M.R. Melloch, High – voltage double-implanted MOS power transistors in 6H-SiC ,IEEE Electronic Device Lett., 18,93(1997)

[53] J. Tan, J. A. Cooper, Jr., and M. R. Melloch, "High-voltage accumulation-layer UMOSFETs in 4H SiC", IEEE Electron Device Lett., 1998, 19, 487-489.

[54] J. Spitz, J. A. Cooper, and M. R. Melloch, “High-voltage lateral DMOSFETs in 4HSiC”,IEEE Electron Device Lett., 1998, 19, 100-102.

[55]. B.J. Baliga, “Power Semiconductor Device Figure of Merit for High-frequency Application”, IEEE Electron Device Letters, Vol.10, pp. 455, 1989.

[56]. B.J. Baliga, “Power Semiconductor Devices, Boston: PWS Publishing, 1995.

[57]. C. Jacoboni, C. Canali, G. Ottaviani, and A.A. Quaranta, “A review of some charge transport properties of silicon”, Solid-Ststе Electronics, Vol. 20, p. 7,1977.

[58]. B.J. Baliga, Modern Power Devices, New York: Wiley 1987.

[59] Design, Modeling, and Characterization of Power MOSFET in 4H-SiC for Extreme Environment Applications Md Hasanuzzaman, Syed K. Islam, Leon M. Tolbert

[60] K. Shenai, R. S. Scott, and B. J. Baliga, “Optimum semiconductors for high power electronics,” IEEE Trans. Electron Devices, 1989, 36, 1811-1823.

[61] Sze, S. M., Physics of Semiconductor Devices, 2nd. ed., Wiley-Interscience

[62] S.C.SunandJ. D. Pulmmer, “Modeling of the on resistance of LDMOS, VDMOS, and VMOS power transistors, ”IEEETransactiononElectron Devices,vol.27,pp.356-367,1980.

[63] J.W.Palmour,R.singh,R.Glass,O.Kordina,and C.H. Carter,Jr., power semiconductor devices and IC’s, in Proceedings of the international symposium on power

semiconductor devices and IC's,pp.25-32, 1997.
[64] "Physical Modeling and Scaling Properties of 4H-SiC Power Devices"
T.Hatakeyama, J. Nishio, C. Ota and, T. Shinohe

4. DIMOSFET Mathematical Modeling and Simulation

Introduction

In the previous chapters we studied silicon carbide and compared it with silicon. According to that comparison we confirmed that silicon carbide is the promising material for the future high voltage power electronics with out any competitive, on the other chapter we had unipolar silicon carbide in more details.

In this chapter our investigative attention has been paid to VDIMOSFET silicon carbide trying to exploit a special interest in high voltage power electronic devices. So geometric and technological parameters will play the leading role in making contribution to better understanding and modeling in VDIMOSFET. Also the influence of anisotropy related to (μ_n is the electron mobility, v_{sat} is the electron saturation velocity, temperature) and 4H – SiC material has been chosen because of its almost two times larger low field mobility in comparison to 6H-SiC [1,2]. This device can carry large currents (and voltages) during the „on“ state and is capable of sustaining large „blocking“ voltages in the „off“ state. The two facts can provide large drain currents, what together with high voltage makes this structure convenient for use in power electronics. and both cases the crucial role is played by its „vertical“ section, usually denoted as „drift“ region [3]. The first step necesarry to be performed is to properly investigate and describe the general I_D (V_{DS}) characteristic for the entire device. especially for higher values of drain current and subsequently drift region voltages.

4.1. General Features of the VDIMOS Structure

A structure considered is shown in Fig.4.1. [4]. its crucial component (not met in the convenient MOS structure) is a vertical drift region. It is usually assumed to be divided into three sections (A – the accumulation layer, B – the flow narrowing region and C – the wide flow region) as shown in Fig. 4.1. But there also exist some simplified models suggesting that the vertical „drift“ region comprises only two sections (A – the accumulation layer and the flow narrowing region B) [5].

In the figure: W denotes the width of the sample (along z-axis), L_d and L_p are the lengths of accumulation region and p-body respectively (both along y-axis according to Fig.4.1), W_T is the total epilayer thickness, while W_A is the thickness of accumulation region (both in x-direction); the angle α describes B-region profile, μ is the bulk mobility of carriers in SiC and N_D is its doping concentration of the ionized donors, W_A W_A $=W_j+W_d$ is the accumulation layer depth, Other geometric parameters are labeled in

figures.

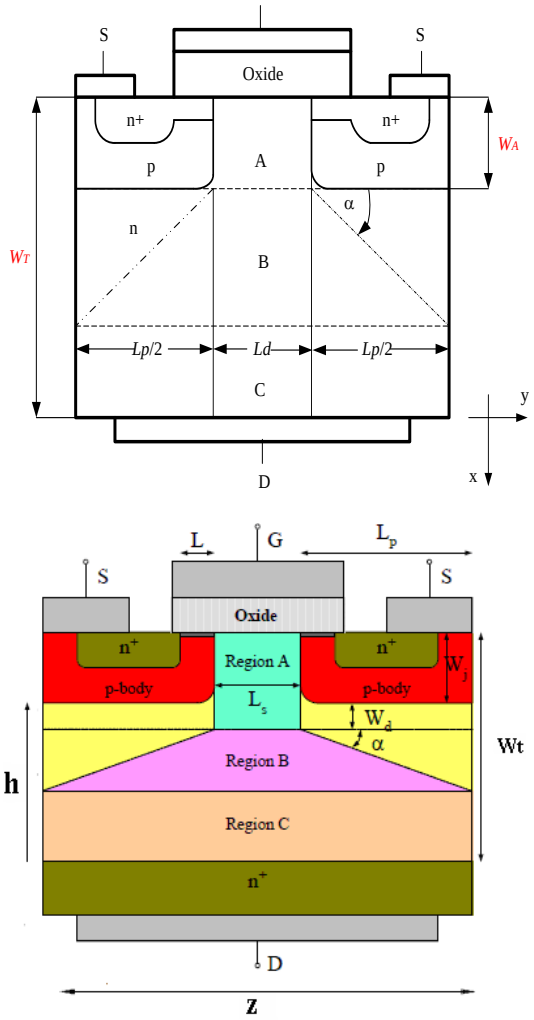


Figure.4. 1: *The schematic cross section of the conventional SiC VDIMOS structure expressing three sections model*

Deeply. It begins with a narrow section embedded in p-body substrate (section A) occupied by a constant vertical drain current I_D in the above direction. The region of greater width is positioned beneath region A and three important sections can be recognized in it: just beneath p-body layers two sections arise (left and right) which are supported not to be occupied by drain current; between them, the section B is embedded – its width steeply increases in downward direction and it is fulfilled by drain current; just above drain bias and beneath B section region C of constant and as great as possible width exists (fulfilled by drain current again). The drift region is supposed to be lightly n-doped and fully ionized [6, 7].

The heavily doped n^+-regions beneath source bias are encircled by p-bodies and

connected with A-section of a vertical drift region by horizontal channels (left and right) occupied by drain current and so providing the global continuity equation to be satisfied. These channels are rather short (~1μm) and their modeling must be carefully performed. The described structure (denoted as VDMOS) has been proposed and developed in order to meet several requirements. The channel region and the drift region can be investigated and modeled almost separately; the common quantity for both regions is drain current, while drain-to-source voltage is a sum of voltage drops across drift region and one of the channels [8].

4.2.The Analytical Model For Vertical DIMOS Transistor in 4H-Silicon Carbide.

An analytical model for double implanted metal-oxide semiconductor (DIMOS) field effect transistors is developed using SiC material system. The model is developed based on the methodology for a vertical double diffusion MOS model Figure 4.1 shows the details of device structure identifying the different regions of operation Since the diffusion process in SiC is negligible, ion implantation is the only way to form the *p* bodies and the *n*+ region for the vertical structure. Double implantation technology consists of the deep range acceptor followed by the shallow range donor implantation is used to make the necessary MOSFET structure. The thickness and the doping level of the drift region largely determine the breakdown voltage. The larger the thickness of the drift region, the bigger is the blocking voltage. However, the current SiC technology has a limitation of the achievable epilayer thickness.

For the conventional SiC VDIMOS structure cosidered in this investigationis presented in Figure.4.1. The domain of interest is a vertical „drift“ region. It is usually assumed to be divided into three sections , or vertical „drift“ region comprises only two sections as described before. None of the available references makes a judgement which of these two models describes the „drift“ region in a more adequate manner .

The answer to this question will be searched for demonstrating the validity of the least action principle in both cases. To construct the corresponding Lagrangian electric field strengths in each of the sections are necessarily determined [9]. Hence the starting point will be the approximate, but accurate enough, analysis of the field distribution across the flow-occupied part of drift region. First, all over the drift region Poisson's equation must be satisfied [10]:

$$\frac{\partial^2 V}{\partial x^2}+\frac{\partial^2 V}{\partial y^2}=e\cdot\left(N_D-n\right)=0 \qquad \textbf{(4.1)}$$

(the substrate is supposed to be electrically neutral in its each point). In the accumulation region A (in both cases) the constant current along *x*-axis causes the existence of nonzero electric field in the same direction only; their mutual dependence is given by drift diffusion transport model relation [10]:

$$I_D=-\frac{e\cdot W\cdot N_D\cdot\mu\cdot L_d}{1-\frac{1}{E_C}\cdot\frac{dV}{dx}}\cdot\frac{dV}{dx} \qquad \textbf{(4.2)}$$

what immediately gives:

$$\frac{dV}{dx}=-\frac{I_D}{e\cdot W\cdot N_D\cdot\mu\cdot L_d-\frac{I_D}{E_C}};\qquad 0\le x\le W_A;\qquad \frac{dV}{dy}=0;\qquad \left|y\right|\le\frac{L_d}{2} \qquad \textbf{(4.3)}$$

The situation with the middle section B of drift region is not so simple. Due to its varying cross-section the nonzero horizontal electric field also exists. Similar to accumulation section A vertical electric field can be expressed in terms of drift current [10,11]:

$$\frac{\partial V}{\partial x}=-\frac{I_D}{e\cdot W\cdot N_D\cdot\mu\cdot\left[L_d+2\left(x-W_A\right)\cdot ctg\alpha\right]-\frac{I_D}{E_C}};$$

$$W_A\le x\le W_A+\frac{L_p}{2}\cdot tg\alpha;\qquad \left|y\right|\le\frac{L_d}{2}+\left(x-W_A\right)\cdot ctg\alpha \qquad \textbf{(4.4)}$$

And hence

$$\frac{\partial^2 V}{\partial x^2}=-\frac{2\cdot I_D\cdot e\cdot W\cdot N_D\cdot\mu\cdot ctg\alpha}{\left\{e\cdot W\cdot N_D\cdot\mu\cdot\left[L_d+2\left(x-W_A\right)\cdot ctg\alpha\right]-\frac{I_D}{E_C}\right\}^2}=-\frac{\partial^2 V}{\partial y^2} \qquad \textbf{(4.5)}$$

Straightforward integration of the relation (4.5) with respect to y and having on mind the symmetry of E_y with respect to *x* axis:

$$\frac{\partial V}{\partial y} = -\frac{2 \cdot I_D \cdot e \cdot W \cdot N_D \cdot \mu \cdot ctg\alpha}{\left\{ e \cdot W \cdot N_D \cdot \mu \cdot \left[L_d + 2\left(x - W_A\right) \right]^2 - \frac{I_D}{E_C} \right\}^2} \cdot y \qquad \textbf{(4.6)}$$

The situation in the wide section (C) at the bottom of the drift region (if it exists) is analogous to that in the accumulation (A) region; therefore the corresponding expressions are slightly modified [10,11]:

$$\frac{\partial V}{\partial x} = -\frac{I_D}{e \cdot W \cdot N_D \cdot \mu \cdot \left(L_d + L_p\right) - \frac{I_D}{E_C}};$$

$$\frac{dV}{dy} = 0; \quad W_A + \frac{L_p}{2} \cdot tg\alpha \le x \le W_T; \quad |y| \le \frac{L_d}{2} + \frac{L_p}{2} \qquad \textbf{(4.7)}$$

The straight forward integration of relations (4.3), (4.4) and (4.7) with respect to the vertical coordinate x gives the expressions for voltage drop along each of the investigated regions [10]:

$$V_A = \frac{I_D \cdot W_A}{e \cdot W \cdot N_D \cdot \mu \cdot L_d - \frac{I_D}{E_C}} \qquad \textbf{(4.8a)}$$

$$V_B = \frac{I_D \cdot tg\alpha}{2 \cdot e \cdot W \cdot N_D \cdot \mu \cdot} \cdot \ln \frac{e \cdot W \cdot N_D \cdot \mu \cdot \left(L_d + L_p\right) - \frac{I_D}{E_C}}{e \cdot W \cdot N_D \cdot \mu \cdot L_d - \frac{I_D}{E_C}} \qquad \textbf{(4.8b)}$$

$$V_C = \frac{I_D \cdot \left(W_T - W_A - \frac{1}{2} L_p \cdot tg\alpha \right)}{e \cdot W \cdot N_D \cdot \mu \cdot \left(L_d + L_p\right) - \frac{I_D}{E_C}} \qquad \textbf{(4.8c)}$$

$$V_{DRIFT} = V_A + V_B + V_C \qquad \textbf{(4.9)}$$

The parameter E_C is defined as the ratio v_s/μ (v_s is the saturated drift velocity of carriers, and μ_n the low field electron mobility.The majority of these parameters (W, N_D, μ, L_d, L_p, E_C, W_T) are given by the sample specification. they can be varied by hand and will not be in the special focus of this study . The other two quantities W_A, tgα are not fixed; they will depend on the drain current in our sample. An attempt to determine their values and discuss the influence on the current-voltage characteristic of the drift region

has been described in this investigation. To examine the behaviour of these two variables is neccessary in order to construct the model in a closed form, especially in the case of larger values of drain current.

At this point we shall stop the investigation of Poisson's equation and its consequences and turn to the construction of the quantity called „action“ [5]:

$$S(t_1,t_2)=\int_{t_1}^{t_2} L\left(qi,\dot{qi},t\right)\cdot dt \qquad \textbf{(4.10)}$$

obeying the famous rule – „least action principle“. Shortly, among all possible trajectories with fixed initial and final positions the real one is the trajectory with the fulfilled condition of minimal (or not often maximal) action. Due to the stationary character of current flow (Lagrangian functional $L\left(qi,\dot{qi},t\right)$ does not depend explicitly on time) one is allowed to make a conclusion that minimal action coincides with the minimal Lagrangian functional L; hence the described values of W_A, tgα can be determined from the following set of equations:

$$\frac{\partial L}{\partial W_A}=0\,; \qquad \frac{\partial L}{\partial tg\alpha}=0 \qquad \textbf{(4.11)}$$

The Lagrangian functional is constructed by means of its local density Z:

$$L=\int_V Z\cdot dV = W\cdot\int_{S_{xy}} dx\cdot dy\cdot Z(x,y) \qquad \textbf{(4.12)}$$

where S_{xy} denotes the horizontal cross-section of the drift region (Fig.4. 1). Magnetic field being neglected and having on mind that the drift region is considered electrically neutral (with the equal amounts of ionized donors and mobile electrons), the Lagrangian density turns out to depend only on electric field strength [12]:

$$L=W\cdot\int_0^{W_T} dx\int_{-Y(x)}^{Y(x)} dy\cdot Z(x,y)\,; \qquad Z=\frac{1}{2}\varepsilon\cdot\left[\left(\frac{\partial V}{\partial x}\right)^2+\left(\frac{\partial V}{\partial y}\right)^2\right] \qquad \textbf{(4.13)}$$

If a three section model (A, B, C in Fig.4.1) is accepted, the integration over the following domain (Fig.4.1):

A: $\quad 0\le x\le W_A\,; \quad |y|\le\frac{L_d}{2}\,;$

B: $\quad W_A\le x\le W_A+\frac{L_p}{2}\cdot tg\alpha\,; \quad |y|\le\frac{L_d}{2}+(x-W_A)\cdot ctg\alpha\,;$

$$\text{C:} \quad W_A + \frac{L_p}{2} \cdot tg\alpha \le x \le W_T; \qquad |y| \le \frac{L_d + L_p}{2} \tag{4.14}$$

after tedious, but straightforward calculations gives:

$$\begin{aligned} L_{ABC} = {} & \frac{1}{2} \cdot \varepsilon \cdot W \cdot \frac{L_d \cdot {I_D}^2}{{\lambda_d}^2} \cdot W_A + \frac{1}{4} \cdot \varepsilon \cdot W \cdot \left(\frac{I_D}{e \cdot W \cdot N_D \cdot \mu} \right)^2 \cdot \\ & \cdot \left\{ tg\alpha \cdot \left[\ln \frac{\lambda_{dp}}{\lambda_d} + \frac{I_D}{E_C} \cdot \left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}} \right) \right] + ctg\alpha \cdot \left[\frac{1}{3} \cdot \ln \frac{\lambda_{dp}}{\lambda_d} + \frac{I_D}{E_C} \cdot \left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}} \right) + \right. \right. \\ & \left. \left. + \frac{1}{2} \left(\frac{I_D}{E_C} \right)^2 \cdot \left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}} \right)^2 + \frac{1}{3} \left(\frac{I_D}{E_C} \right)^3 \cdot \left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}} \right)^3 \right] \right\} + \\ & + \frac{1}{2} \cdot \varepsilon \cdot W \cdot \frac{\left(L_d + L_p \right) \cdot {I_D}^2}{{\lambda_{dp}}^2} \cdot \left(W_T - W_A - \frac{1}{2} L_p \cdot tg\alpha \right) \end{aligned} \tag{4.15}$$

with the abbreviations used:

$$\lambda_d = e \cdot W \cdot N_D \cdot \mu \cdot L_d - \frac{I_D}{E_C}; \qquad \lambda_{dp} = e \cdot W \cdot N_D \cdot \mu \cdot \left(L_d + L_p \right) - \frac{I_D}{E_C} \tag{4.16}$$

Although the expression (4.15) seems rather clumpsy, the set of equations (4.11) is simply reduced to:

$$\frac{\partial L_{ABC}}{\partial W_A} = 0 \quad \Rightarrow \quad \frac{1}{2} \cdot \varepsilon \cdot W \cdot {I_D}^2 \cdot \left(\frac{L_d}{{\lambda_d}^2} - \frac{L_d + L_p}{{\lambda_{dp}}^2} \right) = 0 \tag{4.17a}$$

$$\frac{\partial L_{ABC}}{\partial tg\alpha} = 0 \Rightarrow$$

$$tg\alpha = \sqrt{\frac{\frac{1}{3} \cdot \ln \frac{\lambda_{dp}}{\lambda_d} + \frac{I_D}{E_c} \cdot \left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}} \right) + \frac{1}{2} \left(\frac{I_D}{E_C} \right)^2 \cdot \left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}} \right)^2 + \frac{1}{3} \left(\frac{I_D}{E_C} \right)^3 \cdot \left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}} \right)^3}{\ln \frac{\lambda_{dp}}{\lambda_d} + \frac{I_D}{E_c} \cdot \left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}} \right) - \frac{\left(e \cdot W \cdot N_D \cdot \mu \right)^2 \cdot \left(L_d + L_p \right) \cdot {I_D}^2}{{\lambda_{dp}}^2}}} \tag{4.17b}$$

The equation (4.17a) can never be satisfied. The expression on the right side remains positive as far as λ_d>0 (what is always fulfilled). Consequently $L(W_A)$ has no local minimum /maximum inside the domain of drift region; it reaches its minimal value for $W_A=W_J+W_d$, where W_J denotes the depth of p contact region and W_d is the depletion region depth, and therefore W_A is suggested to be chosen as:

$$W_A = W_J + W_d \tag{4.18}$$

This can be understood as follows: the narrowing of our current flow profile needs some additional energy to be spent; hence this narrowing happens not earlier than it is caused by some external constraints (the existence of n^+ - regions and p-bodies). The expresssion under the square root in relation (4.17b) is easily verified to be always positive, hence no difficulties considering the existence of tanα are expected to arise.

The alternative two sections model (A, B) of drift region implies the integration of relation (4.13) over the modified domain (Fig.4.2)

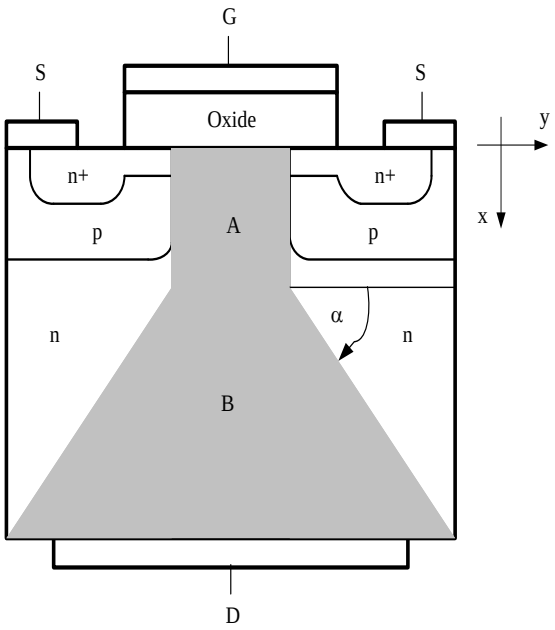


Figure.4. 2: *The schematic cross section of the conventional SiC VDIMOS structure expressing two sections model*

A: $0 < x < W_A$; $\quad |y| \le \frac{L_d}{2}$

B: $W_A < x < W_T$; $\quad |y| \le \frac{L_d}{2} + \frac{L_p}{2} \cdot \frac{x - W_A}{W_T - W_A}$ **(4.19)**

which after lengthy calculation gives:

$$L_{AB} = \frac{1}{2} \cdot \varepsilon \cdot W \cdot \frac{L_d \cdot {I_D}^2}{{\lambda_d}^2} \cdot W_A + \frac{1}{4} \cdot \varepsilon \cdot W \cdot \left(\frac{I_D}{e \cdot W \cdot N_D \cdot \mu} \right)^2 \cdot$$
$$\cdot \left\{ \frac{2 \cdot (W_T - W_A)}{L_p} \cdot \left[\ln \frac{\lambda_{dp}}{\lambda_d} + \frac{I_D}{E_C} \cdot \left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}} \right) \right] + \frac{L_p}{2 \cdot (W_T - W_A)} \cdot \right. \quad \textbf{(4.20)}$$
$$\left. \left[\frac{1}{3} \cdot \ln \frac{\lambda_{dp}}{\lambda_d} + \frac{I_D}{E_C} \cdot \left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}} \right) + \frac{1}{2} \left(\frac{I_D}{E_C} \right)^2 \cdot \left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}} \right)^2 + \frac{1}{3} \left(\frac{I_D}{E_C} \right)^3 \cdot \left(\frac{1}{\lambda_d} - \frac{1}{\lambda_{dp}} \right)^3 \right] \right\}$$

Obviously tanα appears no more as a variable, and the first derivative with respect to the only one left becomes:

$$\frac{\partial L_{AB}}{\partial W_A}=\frac{1}{2}\cdot\varepsilon\cdot W\cdot\frac{L_d\cdot {I_D}^2}{{\lambda_d}^2}\cdot W_A-\frac{1}{4}\cdot\varepsilon\cdot W\cdot\left(\frac{I_D}{e\cdot W\cdot N_D\cdot\mu}\right)^2\cdot$$
$$\cdot\left\{\frac{2}{L_p}\cdot\left[\ln\frac{\lambda_{dp}}{\lambda_d}+\frac{I_D}{E_C}\cdot\left(\frac{1}{\lambda_d}-\frac{1}{\lambda_{dp}}\right)\right]-\frac{L_p}{2\cdot\left(W_T-W_A\right)^2}\cdot\right. \qquad \textbf{(4.21)}$$
$$\left.\left[\frac{1}{3}\cdot\ln\frac{\lambda_{dp}}{\lambda_d}+\frac{I_D}{E_c}\cdot\left(\frac{1}{\lambda_d}-\frac{1}{\lambda_{dp}}\right)+\frac{1}{2}\left(\frac{I_D}{E_C}\right)^2\cdot\left(\frac{1}{\lambda_d}-\frac{1}{\lambda_{dp}}\right)^2+\frac{1}{3}\left(\frac{I_D}{E_C}\right)^3\cdot\left(\frac{1}{\lambda_d}-\frac{1}{\lambda_{dp}}\right)^3\right]\right\}>0$$

The right-hand side of expression (4.21) is always positive, so the choice $w_A=w_J+w_d$ still holds. At the end of this section the drift region voltage drop in the latest case can be calculated as follows [11,13]:

$$V_{DRIFT}=V_A+V_B=$$
$$=\frac{I_D\cdot W_A}{e\cdot W\cdot N_D\cdot\mu\cdot L_d-\frac{I_D}{E_C}}+\frac{I_D}{e\cdot W\cdot N_D\cdot\mu}\cdot\frac{W_T-W_A}{L_p}\cdot\ln\frac{e\cdot W\cdot N_D\cdot\mu\cdot\left(L_d+L_p\right)-\frac{I_D}{E_C}}{e\cdot W\cdot N_D\cdot\mu\cdot L_d-\frac{I_D}{E_C}} \qquad \textbf{(4.22)}$$

4.2.1. Comparison of Simulation and Experimental Data with the Results of Our Investigation And Parameter Extraction

The model which we developed in this study has been tested for a specific set of geometric and technological parameters: $N_D=4\cdot10^{21}\text{m}^{-3}$, $v_s=2\cdot10^5$m/s, $\mu=0.08\text{m}^2/(\text{V}\cdot\text{s})$, $W_J=30\mu$m, $W_d=2\mu$m, $L_d=10\mu$m, $L_p=25\mu$m, $W_T=70\mu$m, $W=40\mu$m. For better understanding of the results it is useful to write relations (4.8), (4.16), (4.17b) and (4.22) in a more transparent manner:

a) if three sections A, B, C are formed;

$$V_{DRIFT}=\frac{v_s}{\mu}\cdot W_A\cdot\frac{I_D}{I_K-I_D}+\frac{v_s}{\mu}\cdot\frac{L_d}{2}\cdot tg\alpha\cdot\frac{I_D}{I_K}\cdot\ln\frac{\left(1+\frac{L_p}{L_d}\right)\cdot I_K-I_D}{I_K-I_D}+$$
$$+\frac{v_s}{\mu}\cdot\left(W_T-W_A-\frac{1}{2}\cdot L_p\cdot tg\alpha\right)\cdot\frac{I_D}{\left(1+\frac{L_p}{L_d}\right)\cdot I_K-I_D} \qquad \textbf{(4.23)}$$

$$\eta_d=I_K-I_D;\qquad \eta_{dp}=\left(1+\frac{L_p}{L_d}\right)\cdot I_K-I_D;\qquad I_K=e\cdot W\cdot N_D\cdot L_d\cdot v_s \qquad \textbf{(4.24)}$$

$$tg\alpha = \sqrt{\frac{\frac{1}{3}\cdot\ln\frac{\eta_{dp}}{\eta_d}+\left(\frac{I_D}{\eta_d}-\frac{I_D}{\eta_{dp}}\right)\cdot\left[1+\frac{1}{2}\cdot\left(\frac{I_D}{\eta_d}-\frac{I_D}{\eta_{dp}}\right)+\frac{1}{3}\cdot\left(\frac{I_D}{\eta_d}-\frac{I_D}{\eta_{dp}}\right)^2\right]}{\ln\frac{\eta_{dp}}{\eta_d}+\left(\frac{I_D}{\eta_d}-\frac{I_D}{\eta_{dp}}\right)-\frac{{I_K}^2\cdot\left(1+\frac{L_p}{L_d}\right)\cdot\frac{L_p}{L_d}}{{\eta_{dp}}^2}}} \qquad \textbf{(4.25)}$$

b) if two sections A, B are formed the relation (4.23) turns to:

$$V_{DRIFT} = \frac{v_s}{\mu}\cdot W_A\cdot\frac{I_D}{I_K - I_D}+\frac{v_s}{\mu}\cdot\frac{L_d}{2}\cdot\left(W_T - W_A\right)\cdot\frac{I_D}{I_K}\cdot\ln\frac{\left(1+\frac{L_p}{L_d}\right)\cdot I_K - I_D}{I_K - I_D} \qquad \textbf{(4.26)}$$

It is important to stress the role of the introduced quantity I_k. Although this current is never achieved, its value has a great impact on calculated V_{DRIFT} even for very small drain current. The „referent“ current I_k is completely controlled by the parameters of the structure and hence imposed by hand.

According to the relations (4.24) and (4.25) the slope of the region B for different values of drain current has been calculated (tgα(I_D)) and presented in Fig.4.3. For small values of drain current „tgα“ is slightly smaller than 1 and remains almost unchanged; in the available references the value of parameter „tgα“ is not discussed at all ,in details, so it can be reasonably assumed that its silently accepted value is close to unity. For greater values of drain current the parameter „tgα“ experiences a dramatic increase, which can be stopped only by existence of the upper limit for „tgα“:

$$tg\alpha \le \frac{W_T - W_A}{\frac{L_p}{2}} \qquad \textbf{(4.27)}$$

At this value of „tgα“ the section C ceises to exist and we turn to the two section model (A, B) in order to reliably describe current voltage characteristic for even higher values of drain current I_D.

As long as three section model (A, B, C) of drift region is considered „tgα“ is an increasing function of I_D; hence it can easily be proven that for each value of drain current holds:

$$L_{ABC} < L_{AB} \qquad \forall I_D > 0 \qquad \textbf{(4.28)}$$

This statement implies the following conclusion: the formation of three section flow (A, B, C) is more preferable than the formation of two section flow (A, B) because its restitution needs less energy to be spent. The angle (α) (and „tgα“ as well) increases

with the increase of drain current I_D untill the limit (4.27) is reached. At that moment the onset of two section flow (A, B) occurs, which reliably enough describes the situation for even higher values of drain current.

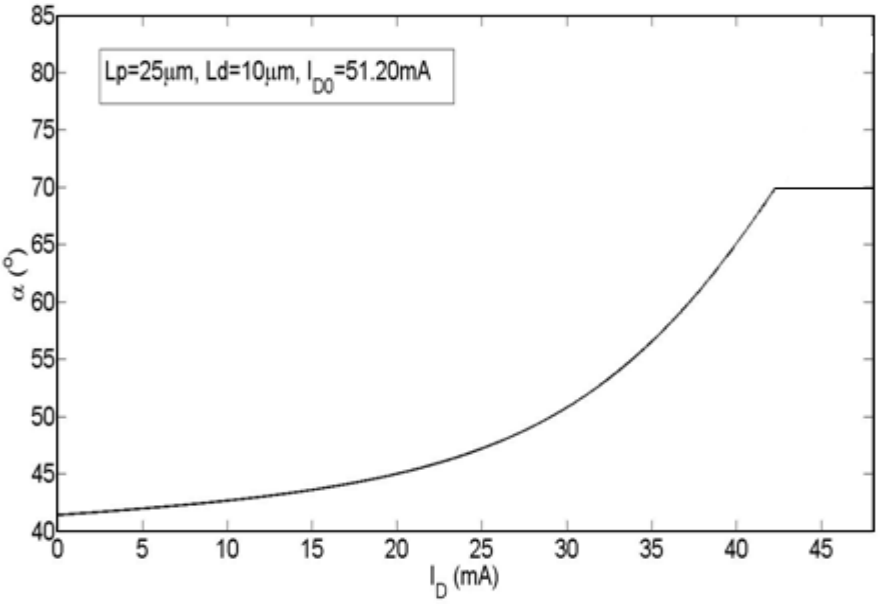


Figure.4.3 a: *The angle α versus drain current I_D calculated according to the procedure developed*

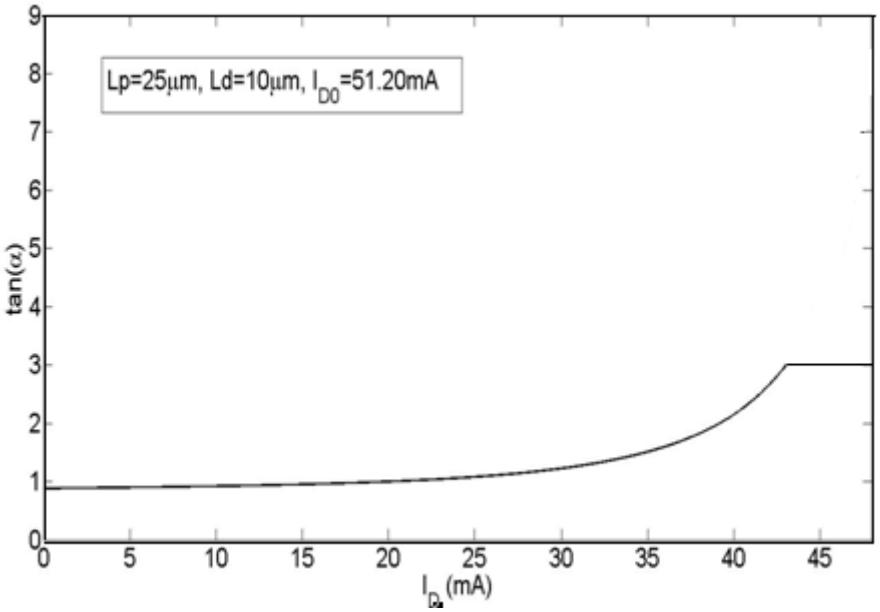


Figure4.3 b: *The tgα versus drain current I_D calculated according to the procedure developed*

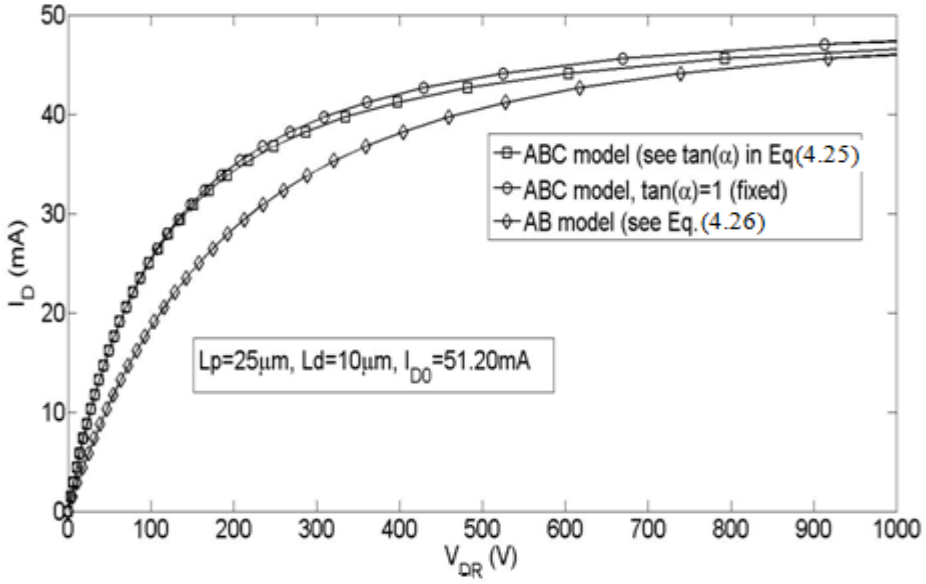


Figure 4.4. *The calculated current – voltage characteristic of drift region I_D (VDRIFT) in three different cases: a) if three sections A, B, C are formed with tgα calculated according to the procedure which was developed. b) if three sections A, B, C are formed with tgα assumed invariant and close to unity, c) if only two sections A, B are formed .*

Figure.4.4.exhibits current-voltage characteristic of the drift region $I_D(V_{DRIFT})$ considering three cases:

a) combination of ABC section model for smaller and AB section model for higher values of drain current (developed in this investigation),

b) simplified two section (AB) model over the entire region of applied drain current, and

c) simulations according to the models available in the literature with the probably accepted value tanα=1.

As expected graphs a) and b) show a significant level of coincidence for higher values of drift current; for its moderate and low values these two models differ from each other very much. Graph c) coincides with a) for smaller values of drain current very well, while for higher values some discrepancy occurs. Nevertheless, the choice for „tgα“ (≈1) in case c) had to be somehow vindicated, what was successfully performed in our investigation and exposed in Fig.4.4.

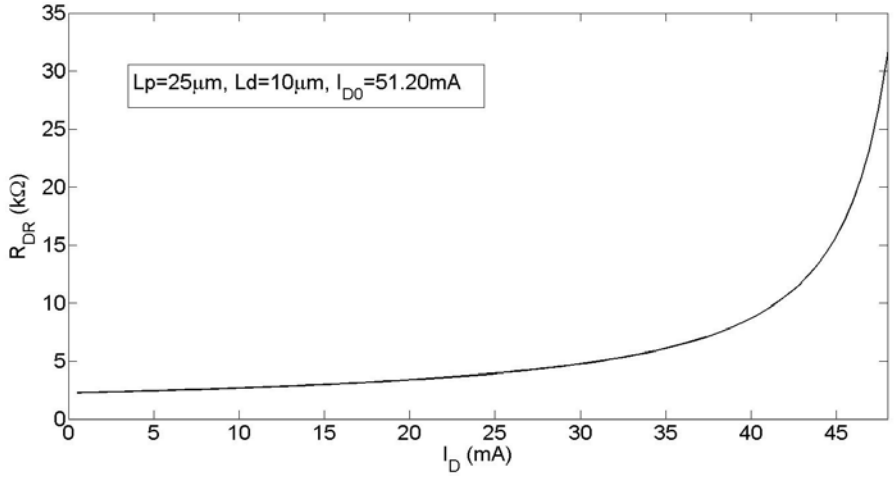


Figure4.5. *Drift region on-resistance versus drain current according to the model proposed*

Sometimes it is useful to define drift-region static resistance as a following ratio (three section ABC picture is accepted) [14]:

$$R_{DR} = \frac{V_{DRIFT}}{I_D} = \\ = \frac{v_s}{\mu} \cdot \left\{ \frac{W_A}{I_K - I_D} + \frac{L_d}{2} \cdot tg\alpha \cdot \ln \frac{\left(1 + \frac{L_p}{L_d}\right) \cdot I_K - I_D}{I_K - I_D} + \right. \\ \left. + \left(W_T - W_A - \frac{1}{2} \cdot L_p \cdot tg\alpha \right) \cdot \frac{I_D}{\left(1 + \frac{L_p}{L_d}\right) \cdot I_K - I_D} \right\} \qquad \textbf{(4.29)}$$

which concerns over the entire domain of drain current. Its nonlinear character is obvious from relation (4.29) as well as from the Figure4.5; especially if we have on mind relation (4.25). For small values of drift current the relation (4.29) is simply reduced to:

$$R_{DR} = \frac{v_s}{\mu} \cdot \frac{1}{I_K} \left\{ W_A + \frac{L_d}{2} \cdot tg\alpha \cdot \ln\left(1 + \frac{L_p}{L_d}\right) + \frac{\left(W_T - W_A - \frac{1}{2} \cdot L_p \cdot tg\alpha \right)}{1 + \frac{L_p}{L_d}} \right\} \qquad \textbf{(4.30)}$$

Hence the relation (4.25) and Figure 4.3 have established a constant value of „tgα“ for small drain current, the drift region resistance calculated according to relation (4.30) became independent on drain current, suggesting that way the linear (ohmic) current-

voltage characteristic.

The external bias (V_G, V_{DS}) can affect the drift region resistance, primarily by reducing the thickness of the accumulation layer, as well as the drain current increase is limited by the saturation onset which occurs in lateral channels accompanied to this structure, but these questions are beyond the scope of this analysis.

4.3. Drift Region Saturation, Channel Saturation

4H-SiC VDMOS semiconductor structure is consists of two considerably different regions. One of them is vertical drift region, while as the other one appears horizontal channel with its left and right section corresponding to source bias. In each of these regions current-voltage can become saturated regardless of the status of another region, Channel resistance plays an important role an in vertical MOSFET, which changes with the gate bias. The drain and source contact resistances are not considered because of the highly dominant drift region resistance and channel resistance. Total drift region voltage, $V_{drift} = V_A + V_B + V_C$, and voltage across the drain to source:

$$V_{DS} = V_{drift} + V_{ch} \tag{4.31}$$

Detailed derivations have already derived. The voltages and the currents of the above mentioned two sets of equations for the drift region and the channel region are implicitly related. The drain current, I_D equals to total channel current I_{ch}, which sets a relationship between the two sets of equations. An iterative solver was developed to evaluate the voltages and the currents.

The channel region is nothing else but the convenient MOS structure in detail investigated and modeled in the literature. In this study, the following approximate form to describe current-voltage characteristic has been adopted [15,16]:

$$I_{D,ch} = \mu_n^* \cdot \frac{W}{L} \cdot C_{ox}' \cdot \frac{2\left(V_{GS} - V_T\right) \cdot V_{ch} - \left(1+\delta\right) \cdot V_{ch}^{\,2}}{1 + \frac{\mu_n^*}{L \cdot v_s^*} \cdot \frac{V_{GS} - V_T}{1+\delta}}$$

$$V_{ch} \le V_{GS} - V_T \tag{4.32a}$$

$$I_{D,ch}^{\,SAT} = \mu_n^* \cdot \frac{W}{L} \cdot C_{ox}' \cdot \frac{\frac{\left(V_{GS} - V_T\right)^2}{1+\delta}}{1 + \frac{\mu_n^*}{L \cdot v_s^*} \cdot \frac{V_{GS} - V_T}{1+\delta}}$$

$$V_{ch} \geq V_{GS} - V_T \qquad \textbf{(4.32b)}$$

Where W and L are channel width and length respectively, while C_{ox}' denotes the oxide layer capacitance per unit area. It is worth mentioning that surface mobility μ_n* and surface saturated velocity v_s* are considerably smaller compared to corresponding bulk values (for practical conditions and lightly doped substrates the surface mobility is roughly half of the bulk mobility). The zero-order estimate for correction coefficient δ (sufficient for rough calculations) is accepted as follows [16, 17]:

$$\delta = \frac{\gamma}{4\sqrt{2\Phi_F}} = \frac{\frac{\sqrt{2\varepsilon N_A \in_S}}{C_{ox}'}}{4\sqrt{2\Phi_t \ln\left(\frac{N_A}{n_i}\right)}} \qquad \textbf{(4.33)}$$

In equation (4.33) N_A is the doping level of p-bodies, Φ_t thermal voltage, n_i the intrinsic concentration and Φ_F the Fermi level. The short channel effects have been accounted for exploiting velocity saturation concept, what makes this model reliable enough. For the sake of this investigation, only the saturated drain current (4.32b) will play an important role.

As mentioned earlier, the conducting part of drift region can be divided in three sections (A, B, C). Transport properties of drift region are assumed not to be different from the bulk case. In the frame of drift-diffusion model, transport is adequately described by the (bulk) low field mobility μ_n and saturation velocity (in the bulk again) v_s.

The shape of transport characteristic reliable enough for the purpose of this investigation is given by:

$$v = \frac{\mu_n \cdot \frac{dV}{dx}}{1 + \frac{\mu_n}{v_s} \cdot \frac{dV}{dx}}, \quad j = e \cdot n \cdot v \qquad \textbf{(4.34)}$$

Where j labels current density (current per unit area). Obviously, for the accumulation section A of drift region (cross-section WL_d, geometric quantities labeled in Fig. 4.1), the drain current becomes:

$$I_D = eWN_D\mu_n L_d \cdot \frac{\left|\frac{dV}{dx}\right|}{1+\frac{\mu_n}{v_s}\cdot\left|\frac{dV}{dx}\right|} \qquad \textbf{(4.35)}$$

The extraction of $\left|\frac{dV}{dx}\right|$ out of relation (4.35) and its integration over accumulation section length W_A simply gives the corresponding voltage drop V_A [8]:

$$V_A = \frac{I_D W_A}{eWN_D\mu_n L_d - \frac{\mu_n}{v_s} I_D} = \frac{I_D\left(W_J + W_d\right)}{eWN_D\mu_n L_d - \frac{\mu_n}{v_s} I_D} \qquad \textbf{(4.36)}$$

It is worth mentioning that the accumulation layer turns out to be as short as possible, i.e. the region between p- bodies with depletion width added, what perfectly agrees with basic principles of physics.

The section B is assumed to have uniformly changing cross-section. Similarly to the relation (4.35), the expression for drain current becomes ($W_A \le x \le W_A + 0.5 L_p \mathrm{tg}\alpha$) [16, 18]:

$$I_D = \frac{eWN_D\mu_n\left[L_d + 2\left(x - W_A\right)ctg\alpha\right]\cdot\left|\frac{dV}{dx}\right|}{1+\frac{\mu_n}{v_s}\cdot\left|\frac{dV}{dx}\right|} \qquad \textbf{(4.37)}$$

Or

$$\left|\frac{dV}{dx}\right| = \frac{I_D}{eWN_D\mu_n\left[L_d + 2\left(x - W_A\right)\cdot ctg\alpha\right] - \frac{\mu_n}{v_s} I_D} \qquad \textbf{(4.37a)}$$

$$V_B = \frac{I_D}{2eWN_D\mu_n ctg\alpha}\cdot \ln\frac{eWN_D\mu_n\left(L_d + L_p\right) - \frac{\mu_n}{v_s} I_D}{eWN_D\mu_n L_d - \frac{\mu_n}{v_s} I_D} \qquad \textbf{(4.38)}$$

The parameter α (tgα) can also be estimated from the basic principles. Rough calculations sufficient for the purpose of this study suggest its value very close to tgα=1 [16].

The carrier transport in section C is rather similar to that in section A, but with the increased cross-section. Therefore the expression for the corresponding voltage drop can be written straightforward:

$$V_C = \frac{I_D\left(W_T - W_J - W_d - \frac{1}{2}L_p tg\alpha\right)}{eWN_D\mu_n\left(L_d + L_p\right) - \frac{\mu_n}{v_s}I_D} \qquad \textbf{(4.39)}$$

Where $\left(W_T - W_J - W_d - \frac{1}{2}L_p tg\alpha\right)$ clearly denotes the C section height (vertical dimension). The entire voltage drop over the whole drift region now becomes:

$$V_{DRIFT} = V_A + V_B + V_C \qquad \textbf{(4.40)}$$

What together with the relation (4.31) gives drain-to-source voltage V_{DS} unavoidable in constructing usual current voltage characteristic $I_D(V_{DS})$. There are several developed procedures of doing it, but the focus of this investigation is something else. Obviously, the relations (4.36) and (4.38) cause very big values of voltage drops V_A, V_B (tending to infinity) for some specific values of drain current. In other words, the drain current limit exists and can not be exceeded for arbitrary high values of drift region voltage. This effect reminds of saturation very much, hence it will be called drift-region saturation and the described maximal drain current becomes [4, 6]:

$$I_{Do} = eWN_D L_d v_s \qquad \textbf{(4.4 1)}$$

When the denominator of (4.36) turns to zero.

On the other hand, drain current in horizontal channels also has its upper limit defined by the expression (4.32b). While none of these values can be exceeded, the conclusion will be rewritten in an elegant form:

$$I_D^{SAT} = \min\left(I_D^{ch,SAT}, I_{D0}\right) \qquad \textbf{(4.42)}$$

Expression (4.41) implies that drift-region saturation drain current is controlled through the doping level of drift region, together with the charge of geometric parameters W, L_d. The channel saturation itself is controlled through the change of gate voltage V_{GS}, accompanied by the design of geometric parameters W, L, t_{ox} etc. The expression (4.42) is conveniently illustrated in Figure 4.6. The almost linear dependence of channel-saturation

drain current on V_{GS} (except for its very small values) gives a hint that the quasi-

saturation really takes place for even higher values of V_{GS} , as expected in high voltage power devices [19].

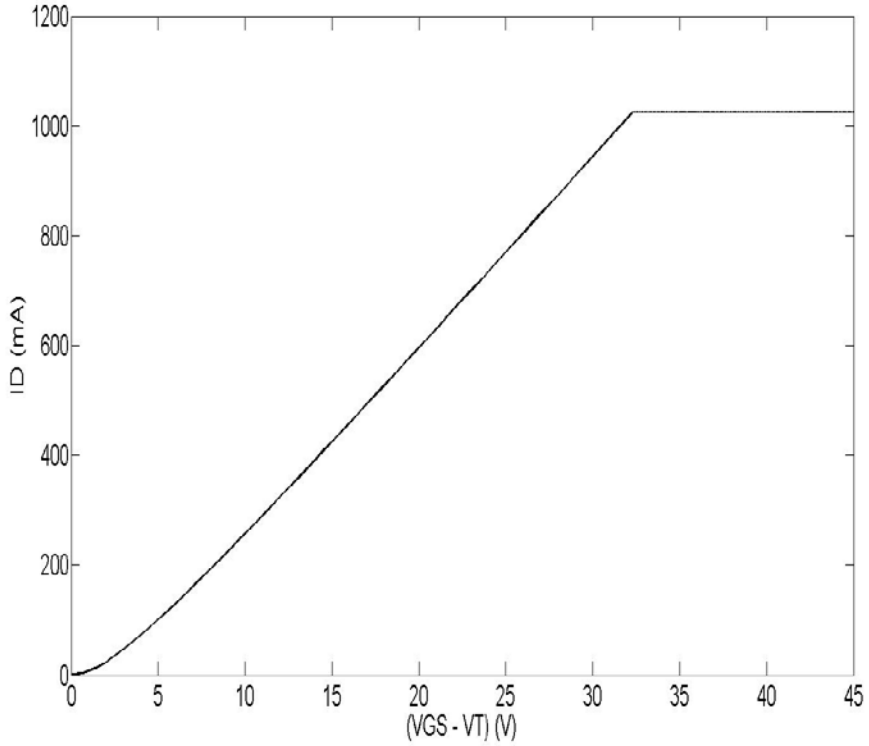


Fig. 4.6. *The cumulative saturation drain current (I_{D0}) versus gate voltage V_{GS}*

It is also worth noticing that we are unable to reach the drain current values arbitrary close to I_{DO} .The breakdown electric field EB sets a strict border for it which is efficiently 1% smaller than (I_{D0}) :

$$I_{DOeff} = I_{DO} \cdot \frac{E_B}{\frac{v_s}{\mu_n} + E_B} \tag{4.43}$$

This fact also imposes a strict theoretical border for V_{DRIFT}:

$$V_{DRIFT} \le E_B W_A + \frac{v_s L_d}{2\mu_n} tg\alpha \cdot \ln\left(\frac{L_p}{L_d} \cdot \frac{E_B \mu_n}{v_s}\right) + \\ + \frac{v_s}{\mu_n} \cdot \frac{L_d}{L_p} \cdot \left(W_T - W_A - \frac{1}{2} L_p \cdot tg\alpha\right) = V^B{}_{DRIFT} \tag{4.44}$$

For the sake of this investigation's goal, the drift region voltage drop will be rewritten in

a more transparent form obtained by inserting relation (4.41) into expression (4.40):

$$V_{DRIFT} = \frac{v_s}{\mu_n} \cdot W_A \cdot \frac{I_D}{I_{DO} - I_D} + \\ + \frac{v_s}{\mu_n} \cdot \frac{L_d tg\alpha}{2} \cdot \frac{I_D}{I^{q,SAT}} \cdot \ln \frac{\left(1 + \frac{L_d}{L_p}\right) I_{DO} - I_D}{I_{DO} - I_D} + \\ + \frac{v_s}{\mu_n} \cdot \left(W_T - W_A - \frac{1}{2} L_p tg\alpha\right) \cdot \\ \cdot \frac{I_D}{\left(1 + \frac{L_p}{L_d}\right) I_{DO} - I_D} \qquad \textbf{(4.45)}$$

Obviously, drift region voltage drop becomes rather simple and for further analysis convenient function of the ratio I_D / I_{DO} what will be thoroughly exploited in the next part.

4.3.1. Comparison Of Simulation And Experimental Data With The Results Of Our Investigation And Parameter Extraction

The model derived in this study has been tested for a specific set of geometric and technological parameters describing the investigated structure [7, 8]:

W=400μm W_J=30μm N_D=4·10^{21}m^{-3}

L=1μm W_d=2μm N_A=4·10^{23}m^{-3}

v_s=2·10^{5}m/s L_d=20μm t_{ox}=50nm

μ_n=0.08m2/Vs L_p=50μm W_T=70μm E_B=2.2·10^{8}V/m

The results of this simulation are shown in figure4.7. The shape of the characteristic agrees with expectations and deserves some additional comments necessary for the correct understanding of device's operation and the requests imposed in front of it.

The region of small drain currents and small drift region voltages (I_D≤400mA, V_{DR}≤100V for a chosen set of technological and geometric parameters) can be recognized as linear regime. Drift region voltage drop is proportional to drain current with a calculable resistance value. The operation of such device is entirely governed by the phenomena taking place in the channel, while drift region behaves just as an ohmic

resistor added in a series to the pair of conventional MOSFETs. To this regime no further attention should be paid, i.e. such device could not meet the specific requests for high power VDMOS design and application. The regime corresponds to V_{GS} voltages not greater than 15V.

The next region observed in Fig. 4.7, will be denoted as nonlinear regime (approximately 400mA≤I_D≤750mA and 100V≤V_{DR}≤400V, corresponding values of V_{GS} lying between 15V and 25V). The departure of the characteristic from linear regime towards saturation is obvious, while the achieved values of drain current and consequently calculated drift region voltages start meeting the requests of application in power electronics. The regime is believed to have considerable importance.

The most interesting region arising from Fig.4.7 is the strongly nonlinear sub drift-region saturation regime.

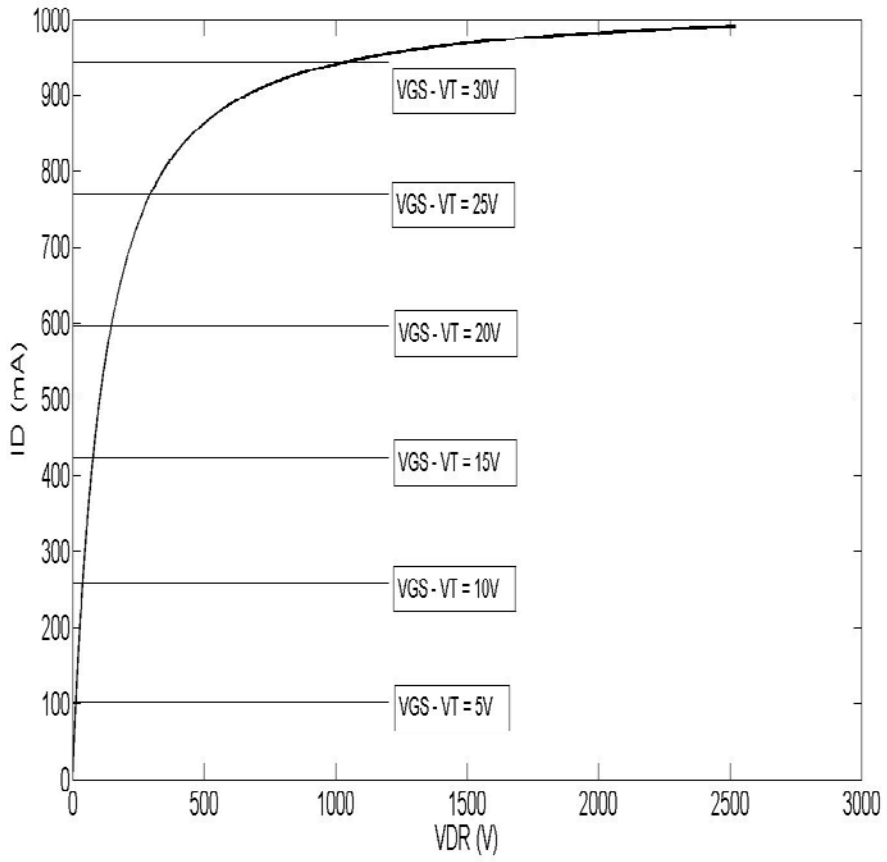


Figure. 4.7. *Drain current versus drift region voltage drop*

Its most important features are relatively narrow range of drain current values (750mA≤I_D≤I_{DOeff}) accompanied by a wide range of drift region voltage values

(V_{DR}≥400V). It is necessary to say that the drift region voltage drop corresponding to the achievement of breakdown electric field lies too high (~7kV) and never occurs. For practical purposes, one can assume that device operation becomes seriously disturbed, i.e. the developed model becomes questionable at the moment when the depleted region is spread as much as possible beneath n+ region. In this Case, C-region (Fig. 4.1) disappears, while A region reaches its maximal value and region B survives. For the chosen set of geometric and technological parameters, this happens for drift region voltage drop of approximately 2.5kV. Last but not least, the sub-saturation regime requires gate-to-source voltage V_{GS} to be above 25V (V_{GS}≥25V). The channel itself must also be kept safe from breakdown. The conventional MOSFET theory neglects horizontal (lateral) electric field in comparison to the vertical one and the constraint that vertical electric field must not exceed breakdown electric field E_B sets the upper border for gate-to-source voltage at about 45V (V_{GS}<45V).

The power electronics application demands relatively high values of drain current I_D and drain-to-source voltage V_{DS} (whose biggest part is accompanied to the drift region), what recommends the nonlinear regime and especially sub-quasi-saturation regime as operation regimes of the greatest interest. The limiting fact concerning these regimes safe from breakdown is a rather narrow “gap” of gate voltages providing it (20V≤V_{GS}≤35V). As the upper limit is fixed, the only way to alleviate this problem is to somehow reduce the lower limit (adjusting geometric and technological parameters in the allowed range or designing a similar.

4.4. The Influence of Anisotropy

Silicon Carbide (4H-SiC as well as 6H-SiC) is known to be an anisotropic material. Among others, the transport parameters like low field mobility and saturation velocity are moderately different in c direction compared to a and b directions in the case of 4H-SiC, while this difference becomes dramatic in the case of 6H-SiC.

The anisotropic character and temperature dependence of transport parameters (low field mobility, saturation velocity, β - parameter describing specific features of drift-diffusion transport model in silicon and related materials) into analytical model for drift region current-voltage characteristic [20, 21]. The procedure has been carried out analytically as long as possible. The horizontal channel itself has been modeled in the literature describing conventional MOS (Metal Oxide Semiconductor) structures; hence

no special attention has been paid to it in this investigation.

The conventional 4H-SiC VDIMOS investigated in the previous section and shown in Fig. 4.1. As the domain of special interest is a vertical “drift” region and the current flow in it is assumed to be divided into three sections A, B, C Fig.4.1. The total current in each of these three regions should be the same. It is vertical and equal to drain current. The previous analyses of “drift” region have led to the development of its widely accepted analytical Model suggesting following expressions for voltage drop in each of its sections [22, 23, 24]:

The expressions (4.8a, 4.8b, 4.8c) have been obtained by means of drift-diffusion model and the most prominent formula describing carriers’ transport in silicon unipolar devices in the presence of velocity saturation.

$$v = \frac{\mu_n \cdot E_x}{1 + \frac{\mu_n}{v_s} \cdot E_x} = \frac{\mu_n \cdot \frac{dV}{dx}}{1 + \frac{\mu_n}{v_s} \cdot \frac{dV}{dx}} \qquad \textbf{(4.46)}$$

This model is realized with the limited number of parameters to be fitted to the experimental data. The expression (4.46) also provides the analytical development of the model far enough, as well as the straightforward implementation of the letter in more complex circuit simulation. As 4H-SiC is recognized as a material with certain level of anisotropy, i. e. its transport properties (and hence corresponding coefficients) are different in c-direction compared to a and b directions [25]. These coefficients also depend on the operating temperature, what begins to play an important role having on mind that silicon-carbide devices are supposed to be engaged in the high temperature range. The model can also be improved by introducing parameter β responsible for transport characteristic $v_x(E_x)$ fine tuning. The parameter itself is also anisotropic and shows the considerable temperature dependence. The modern literature concerning drift-diffusion model suggests replacing the expression (4.46) by a more detailed one:

$$v = \frac{\mu_n \cdot E_x}{\left[1 + \left(\frac{\mu_n}{v_s} \cdot E_x\right)^{\beta}\right]^{1/\beta}} = \frac{\mu_n \cdot \frac{dV}{dx}}{\left[1 + \left(\frac{\mu_n}{v_s} \cdot \frac{dV}{dx}\right)^{\beta}\right]^{1/\beta}} \qquad \textbf{(4.47)}$$

This formula is also consistent with the main features of hydro-dynamic model, which

itself is based upon the Boltzmann transport equation and consequent moments leading to balance equations. Therefore relation (4.47) can be regarded as a product of serious theoretical consideration rather than a consequence of simple fitting to the experimental data. Once having this formula adopted, its implementation in the “drift” region model causes no unavoidable difficulties in its accumulation layer A:

$$I_D = e \cdot W \cdot N_D \cdot L_d \cdot v = \frac{e \cdot W \cdot N_D \cdot \mu_n \cdot L_d \cdot \dfrac{dV}{dx}}{\left[1 + \left(\dfrac{\mu_n}{v_s} \cdot \dfrac{dV}{dx}\right)^{\beta}\right]^{1/\beta}} \qquad \textbf{(4.48a)}$$

Straight-forward leading to expressions:

$$\frac{dV}{dx} = \frac{I_D}{\left[\left(e \cdot W \cdot N_D \cdot \mu_n \cdot L_d\right)^{\beta} - \left(\dfrac{\mu_n}{v_s} \cdot I_D\right)^{\beta}\right]^{1/\beta}} \qquad \textbf{(4.48b)}$$

And:

$$V_A = \frac{I_D \cdot W_A}{\left[\left(e \cdot W \cdot N_D \cdot \mu_n \cdot L_d\right)^{\beta} - \left(\dfrac{\mu_n}{v_s} \cdot I_D\right)^{\beta}\right]^{1/\beta}} \qquad \textbf{(4.48c)}$$

The calculation of voltage drop over varying cross-section layer B causes some more trouble:

$$I_D = \frac{e \cdot N_D \cdot \mu_n \cdot W \cdot \left[L_d + 2 \cdot \left(x - V_A\right) \cdot ctg\alpha\right] \cdot \dfrac{dV}{dx}}{\left[1 + \left(\dfrac{\mu_n}{v_s} \cdot \dfrac{dV}{dx}\right)^{\beta}\right]^{1/\beta}} \qquad \textbf{(4.49a)}$$

And hence:

$$V_B = \int_{W_A}^{W_A+\frac{L_p}{2}\cdot tg\alpha} \frac{I_D \cdot dx}{\left\{\left[e \cdot W \cdot N_D \cdot \mu_n \cdot \left(L_d + 2 \cdot \left(x - W_A\right) \cdot ctg\alpha\right)\right]^{\beta} - \left(\frac{\mu_n}{v_s} \cdot I_D\right)^{\beta}\right\}^{1/\beta}} \quad \textbf{(4.49b)}$$

The above expression becomes simpler after introducing a new variable:

$$z = e \cdot W \cdot N_D \cdot \mu_n \cdot \left[L_d + 2 \cdot \left(x - W_A\right) \cdot ctg\alpha\right] \quad \textbf{(4.49c)}$$

With the final result:

$$V_B = \frac{I_D \cdot tg\alpha}{2 \cdot e \cdot W \cdot N_D \cdot \mu_n} \int_{e \cdot W \cdot N_D \cdot \mu_n \cdot Ld}^{e \cdot W \cdot N_D \cdot \mu_n \left(L_d + L_p\right)} \frac{dz}{\left[z^{\beta} - \left(\frac{\mu_n}{v_s} \cdot I_D\right)^{\beta}\right]^{1/\beta}} \quad \textbf{(4.49d)}$$

The analytical evaluation of V_B would be possible only for specific values of coefficientβ. The procedure is tedious and hence not worth performing. It is much more convenient to calculate V_B by means of any of adequate software tools (MATHLAB, MATHEMATICA…). The expression (4.49d) can be reorganized as follows:

$$V_B = \frac{I_D \cdot tg\alpha}{2 \cdot e \cdot W \cdot N_D \cdot \mu_n} \cdot \left\{ f\left[e \cdot W \cdot N_D \cdot \mu_n \cdot \left(L_d + L_p\right)\right] - f\left(e \cdot W \cdot N_D \cdot \mu_n \cdot L_d\right)\right\} \quad \textbf{(4.50a)}$$

With the abbreviation:

$$f(z) = \int \frac{dz}{\left[z^{\beta} - \left(\frac{\mu_n \cdot I_D}{v_s}\right)^{\beta}\right]^{1/\beta}} \quad \textbf{(4.50b)}$$

Similar to the accumulation layer A, the voltage drop over region C can easily be calculated:

$$V_C = \frac{I_D \cdot \left(W_T - W_A - \frac{1}{2} \cdot L_p \cdot tg\alpha \right)}{\left\{ \left[e \cdot W \cdot N_D \cdot \mu_n \cdot \left(L_d + L_p \right) \right]^{\beta} - \left(\frac{\mu_n}{v_s} \cdot I_D \right)^{\beta} \right\}^{1/\beta}} \qquad \textbf{(4.51)}$$

The entire voltage drop over the whole drift region turns out to be:

$$V_{drift} = V_A + V_B + V_C \qquad \textbf{(4.52)}$$

And is calculated by means of relations (4.48c), (4.49d) and (4.51). In each of these expressions, low field electron mobility μ_n, saturation velocity v_s and the curvature coefficient β in overall formula (4.47) play an important role. As already mentioned, these coefficients show a certain level of anisotropy, i. e. their values for c direction and for a and b directions are remarkably different. Same parameters also depend on operating temperature. Low field mobility has been taken from state–of–the-art measurements and fitted by the following expressions [26, 27, and 28]:

$$\mu_{n\perp c} = 40 + \frac{950 \cdot \left(\frac{T}{300} \right)^{-2.4} - 40}{1 + \left(\frac{T}{300} \right)^{-0.76} \cdot \left(\frac{N_D}{2 \cdot 10^{17}} \right)^{0.76}} \frac{cm^2}{Vs} \qquad \textbf{(4.53a)}$$

$$\mu_{n//c} = 48 + \frac{1140 \cdot \left(\frac{T}{300} \right)^{-2.4} - 48}{1 + \left(\frac{T}{300} \right)^{-0.76} \cdot \left(\frac{N_D}{2 \cdot 10^{17}} \right)^{0.76}} \frac{cm^2}{Vs} \qquad \textbf{(4.53b)}$$

The high field mobility parameters v_s, β are extracted from the full band Monte-Carlo simulations and can be comprised by following formulae [26, 27]:

$$v_{S\perp c} = \frac{2.77 \cdot 10^7}{1 + 0.23 \cdot e^{\left(\frac{T}{600} \right)}} \frac{cm}{s} \qquad \textbf{(4.54a)}$$

$$v_{S//c} = \frac{2.55 \cdot 10^7}{1 + 0.30 \cdot e^{\left(\frac{T}{600}\right)}} \frac{cm}{s} \qquad \textbf{(4.54b)}$$

$$\beta_{\perp c} = 0.60 + 1 \cdot 10^{-3} \cdot T \qquad \textbf{(4.55a)}$$

$$\beta_{\| c} = 1.01 + 0.3 \cdot 10^{-3} \cdot T \qquad \textbf{(4.55b)}$$

The expressions (4.53), (4.54) and (4.55) have been inserted into main relations of the developed model (4.48c), (4.49d) and (4.51)) and so far the drift region voltage drops in various cases have been calculated.

4.4.1. Comparison of Simulation and Experimental Data with the Results of Our Investigation and Parameter Extraction

The model described above has been tested for structure parameters usually met in the relevant references and recommended in commercial device manuals (W=40μm, W_A=1μm, W_T=10μm, L_d=2μm, L_p=10μm, N_D=4x10^{21}m^{-3}).

The model itself offers some general remarks directly from relations (4.49a), (4.50b), (4.51), (4.52) without any calculation:

a) for any specific value of drain current I_D, the drift region voltage drop V_{drift} always remains proportional to μ_n^{-1};

b) Drift region voltage drop V_{drift} should decrease if saturation velocity v_s increased;

c) The transport characteristic fine tuning parameter β maintains its role and becomes responsible for the shape of drift region current-voltage global characteristic.

The results of the calculation performed according to the proposed model are given in Figures 4.8. And 4.9. The Fig. 4.8. Shows the influence of anisotropy on the current-voltage characteristic of drift region for different values of temperature:

a) for arbitrary value of temperature the “normal” orientation (⊥c) provides larger values of maximal drain current I_D compared to “parallel” orientation (||c);

b) for arbitrary value of temperature the characteristic $I_D(V_{drift})$ has a bigger slope for small values of drain current in the case of “parallel” orientation (||c) than in the case of “normal” orientation (⊥c);

c) for higher values of drain current the situation turns out to be quite different; mostly

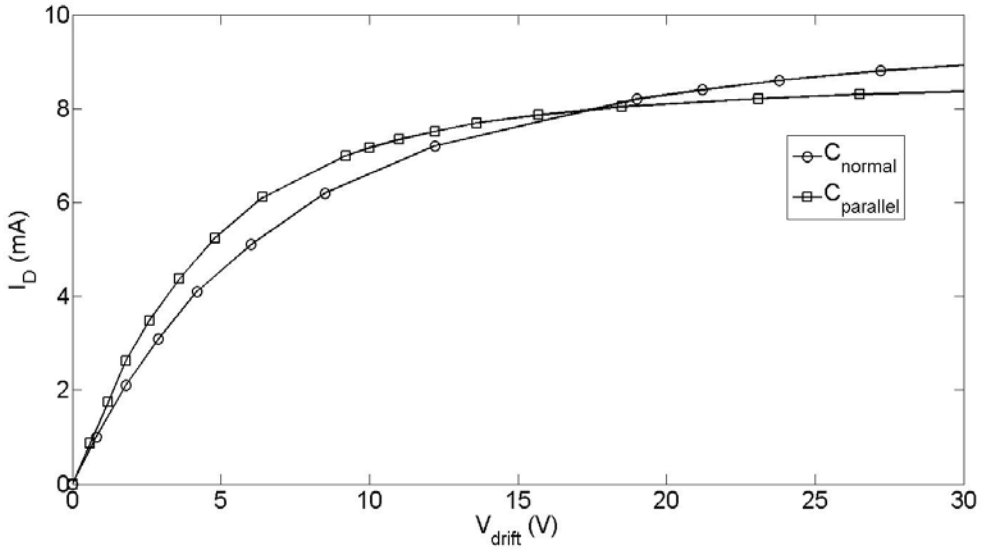


Figure 4.8a: *Drain current versus drift region voltage drop – the influence of anisotropy (temperature T=300K),* $V_{drift\ max}$*=30V,* $I_{D\ max}$*=10mA*

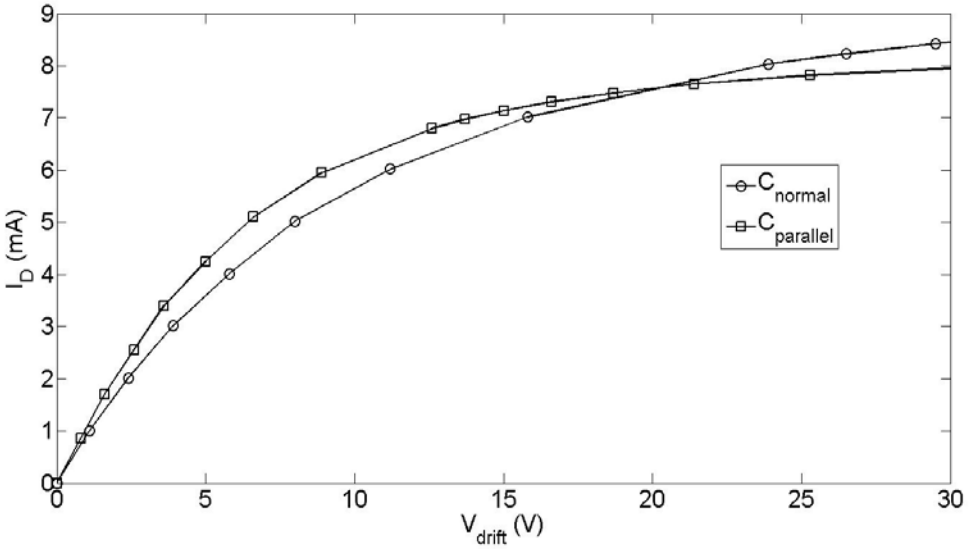


Figure 4.8b: *Drain current versus drift region voltage drop – the influence of anisotropy (temperature T=350K),* $V_{drift\ max}$*=30V,* $I_{D\ max}$*=10mA*

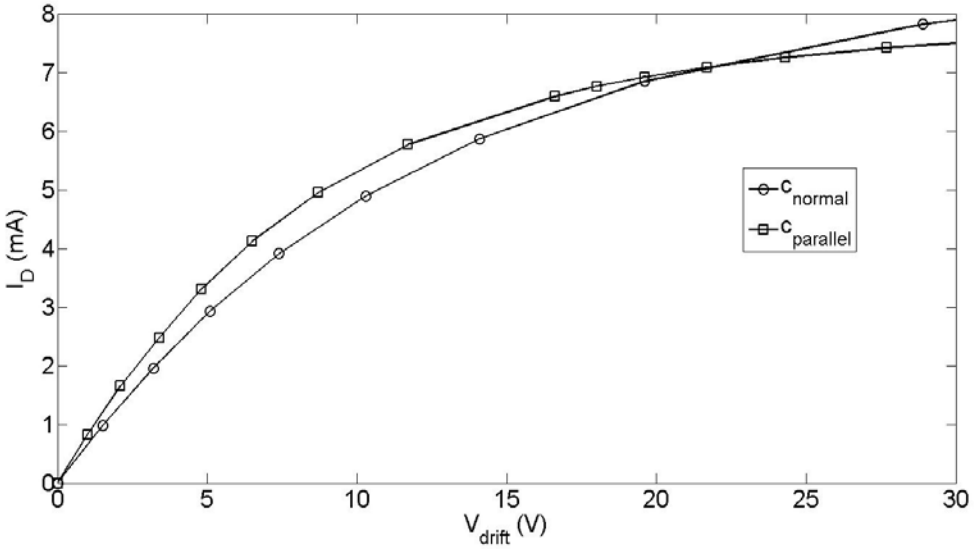


***Figure 4.8c**: Drain current versus drift region voltage drop – the influence of anisotropy (temperature T=400K), $V_{drift\ max}$=30V, $I_{D\ max}$=10mA*

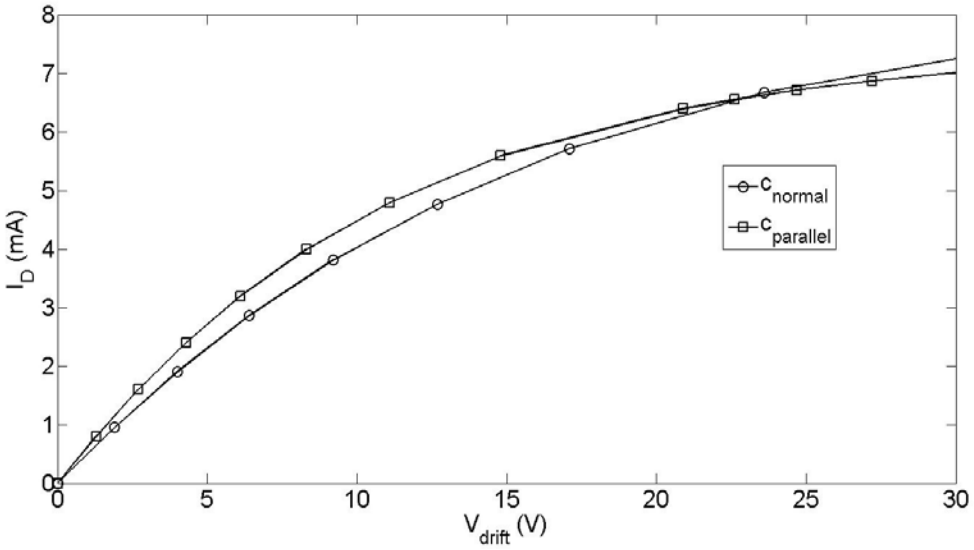


***Figure 4.8d:** Drain current versus drift region voltage drop – the influence of anisotropy (temperature T=450K), $V_{drift\ max}$=30V, $I_{D\ max}$=10mA*

due to the anisotropy of the fine tuning parameterβ, the slope of the characteristic suddenly becomes smaller in the case of "parallel" orientation (||c) compared to the case of "normal" orientation ($\perp$c), thus resulting in the smaller values of maximal drain current for "parallel" orientation (||c) than in the case of "normal" one ($\perp$c).

The figure.4.9 shows $I_D(V_{drift})$ characteristic calculated for each of the investigated orientations (figures 4.9a and 4.9b respectively) with the temperature as a varying

parameter. In both cases, for the same value of drain current, the drift region voltage drop remarkably increases with the increase of temperature, mostly due to the μ_n^{-1} dependence mentioned above.

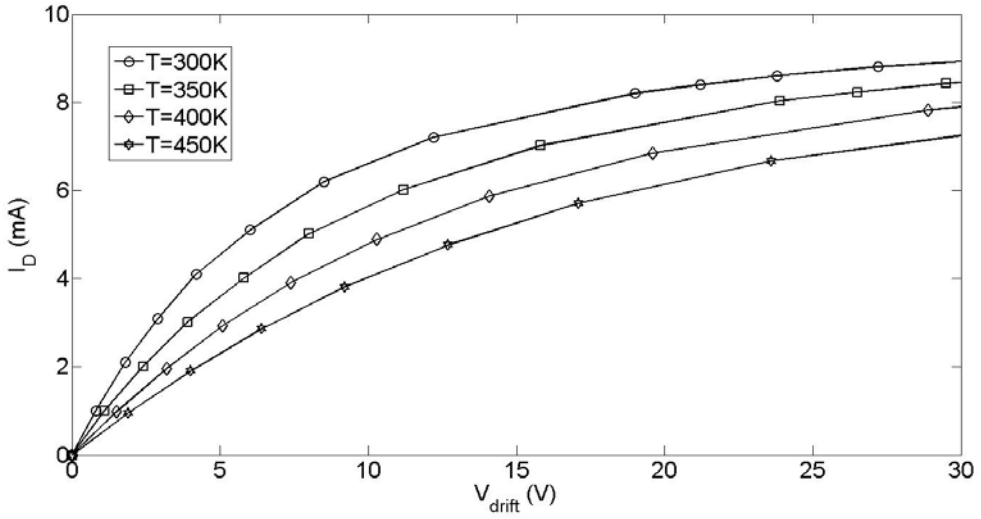


Figure4.9a. *Drain current versus drift region voltage drop for different values of temperature ("normal" orientation (⊥c)), $V_{drift\ max}$=30V, $I_{D\ max}$=10mA*

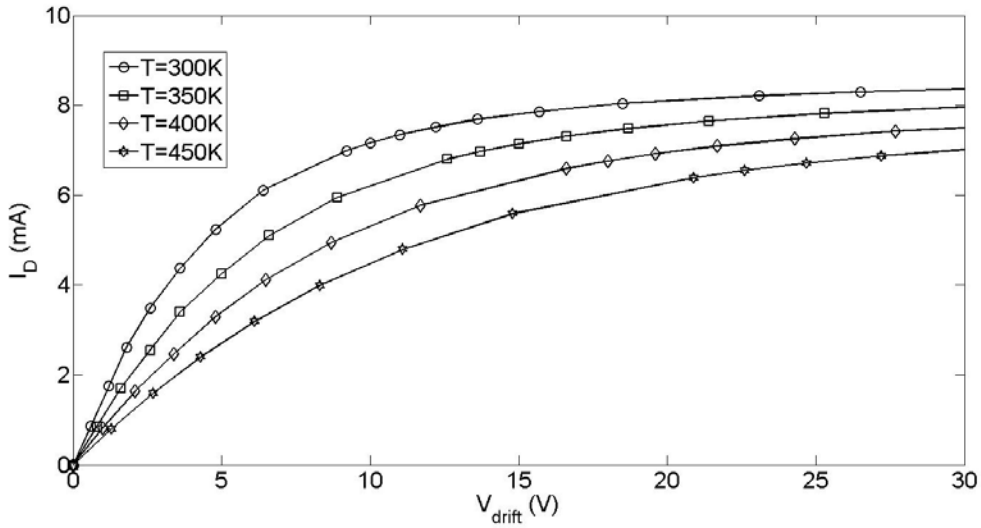


Figure 4.9 b. *Drain current versus drift region voltage drop for different values of temperature ("parallel" orientation (//c)), $V_{drift\ max}$=30V, $I_{D\ max}$=10mA.*

So far only the characteristic drain current versus drift region voltage drop has been considered. Naturally, drain current has its upper cut-off caused by the channel saturation set on. For moderate gate voltage values usually met in such structures, the part of the characteristic concerning small values of drain current (and drift region voltage drop consequently) is expected to play an important role. Drain current values

comparable to the maximal drain current:

$$I_{D\max} = e \cdot N_D \cdot W \cdot L_d \cdot v_s \qquad \textbf{(4.56)}$$

(Inevitably accompanied to greater gate voltages) appear rather as an exception. The region of ultra-small values of drain current (drift-region voltage drop V_{drift} lying in the range (0V - 5V)) can be reliably described by means of dynamical drift-region resistance [29]:

$$r_d = \left.\frac{dV_{drift}}{dI_D}\right|_{I_D=0} \qquad \textbf{(4.57)}$$

Or static drift-region resistance as well:

$$R_{DR} = \left.\frac{dV_{drift}}{dI_D}\right|_{I_D=0} \qquad \textbf{(4.58)}$$

Fortunately, both calculations in the frame of the suggested model (4.49), (4.50), (4.51), (4.52) give the same result:

$$r_d = R_{DR} = \frac{1}{e \cdot W \cdot N_D \cdot \mu_n \cdot L_d} \cdot \left[W_A + \frac{L_d}{2} \cdot tg\alpha \cdot \ln\left(1 + \frac{L_p}{L_d}\right) + \frac{W_T - W_A - \frac{1}{2} \cdot L_p \cdot tg\alpha}{1 + \frac{L_p}{L_d}} \right] \qquad \textbf{(4.59)}$$

Which strongly depends on the parameters of the structure, either geometric or technological? In order to reduce the influence of lateral geometric parameters, it is useful to calculate the “specific-on resistance”:

$$R_{DR}{}^{on} = R_{DR} \cdot W \cdot L_d = \frac{1}{e \cdot N_D \cdot \mu_n} \cdot \left[W_A + \frac{L_d}{2} \cdot tg\alpha \cdot \ln\left(1 + \frac{L_p}{L_d}\right) + \frac{W_T - W_A - \frac{1}{2} \cdot L_p \cdot tg\alpha}{1 + \frac{L_p}{L_d}} \right] \qquad \textbf{(4.60)}$$

Its value calculated according to the relation (4.60) is about 0.6mΩcm^2 and appears to be significantly lower than the data available in the literature [21, 29]. The obtained values are approximately 10mΩcm^2 [29], while Cree Research Inc. has reported 6mΩcm^2 (measured at V_{GS}=10V and decreasing if V_{GS} increases) [21]. Lower value of specific-on-resistance calculated in this study is expected and can be credibly explained by the accepted value of accumulation layer length W_A=1μm, what is considerably smaller than in the cited references. Relation (4.60) suggests that main contribution to the specific-on-resistance comes from accumulation layer length W_A; if its value would be accepted several times higher than in this study, the specific-on-resistance would

reach the values cited in the relevant references [21,29]. As expected, its anisotropic behavior is completely governed by the anisotropic character of the low field mobility μ_n, while saturation velocity v_s and fine tuning parameter β have no influence on it.

In figure 4.10 static drift region specific-on-resistance as a function of drain current has been presented. For small values of drain current this specific-on-resistance is almost constant and can be calculated by means of relation (4.58); for higher values of drain current, the static (as well as dynamic) specific-on-resistance dramatically increases showing its strongly non-linear character inherent to use in power electronics [30].

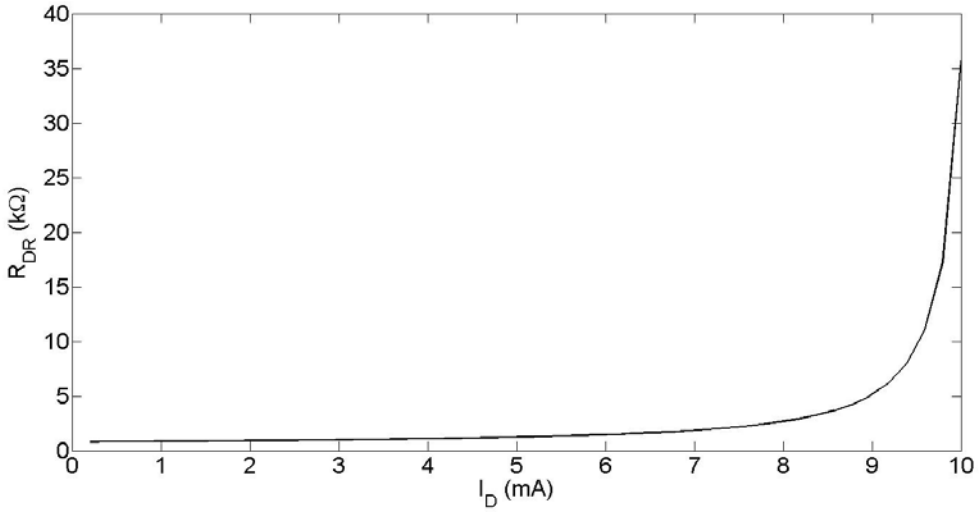


Figure.4.10: *Static drift region specific-on-resistance versus drain current*

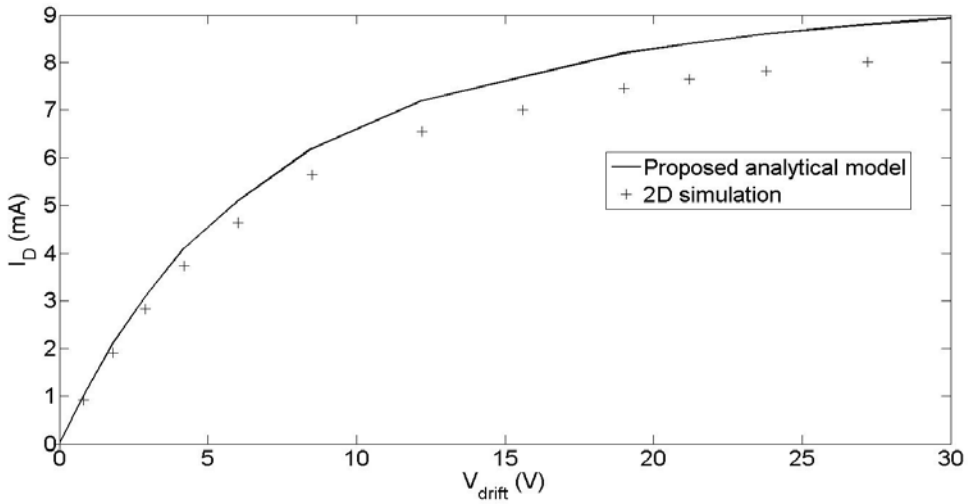


Figure:4.11 *Current - voltage characteristic of the drift region – comparison between the results obtained by the proposed analytical model and those obtained by 2D simulation ("parallel" orientation (//c), T=300K)*

The interesting part of this investigation concerns the relation of this analytical model and 2D simulation results for drift region current-voltage characteristic. For the sake of this investigation 2D simulation has been performed in a two-dimensional device simulator (ATLAS) and the results are shown in figure 4.11. The main conclusion is that the 2D simulated characteristic lies slightly under the characteristic obtained by the proposed model for the chosen set of parameters, i. e. the results of these two approaches are in a quite satisfactory agreement, as expected from the data available from literature [23, 31].

4.5. Conclusion

Our investigation was concentrated on the use of silicon carbide semiconductor in high voltage 4H- SiC DIMOSFET unipolar devices . To support the study of potential utilization of the emerging silicon carbide (SiC) unipolar devices, was investigated systematically in this investigation.

4H-SiC material showed significant promise for high-temperature, high voltage power device applications due to its large bandgap, high critical electric field, and high relatively isotropic electron mobility. The achievements are summarized as follow

An analytical model for vertical double implanted DIMOS structure has been developed to analyze the device behavior and evaluate its characteristics quite accurately A vertical device structure is proposed to verify the model in 4H-SiC , and managed us to understand the physical and electrical properties of (DIMOS). It would be much easier to be paved for beneficial in the field of high voltage power electronics. The basic principles of electrical and physics has been applied to examine the current flow profile theoretically. All the parameters describing this profile have been determined, making that way the model closed. The consequences of the suggested procedure are compared to the data available in the literature with the considerable level of agreement.

DIMOSFET power transistors can carry large currents and voltages during “on” state, vertical section (drift region) is capable of sustaining large blocking voltages in the “off” state across their drain-source terminals and its internal dynamic resistance minimized by enlarging the drift regions to three sections (accumulation channel mobility)**.** A simulation and experimental data was used to simulate the proposed device structure and thereby verify the analytical model.

The impact of drift-saturation (and hence the value of drift-saturation drain current) has been studied in details. Although drift-saturation is never achieved, it has been analytically shown and by simulations confirmed that it played very important role even for smaller values of drain current. On the other hand, rather big values of drift voltage and drain current appearing in our calculations should not worry; they were the consequence of rather big values of geometric parameters accepted in this investigation. Further size reduction will indispensably lead to lower values of drift region voltage drop and drain current, at first place of drift region saturation current, but the general shape of obtained dependances will be sustained.

The existing analytical model of current-voltage characteristic for VDIMOS drift region

introducing a more accurate transport model with fine tuning parameter included and was developed. By means of this way developed model, the drift region voltage drop has successfully been calculated. The mentioned fine tuning parameter, as well as saturation velocity and low electric field mobility posses a considerable level of anisotropy, which mainly affects the shape of current-voltage characteristics and the value of the maximal drain current. It has also been demonstrated that the change of working temperature strongly affected the investigated characteristics. , also effects like quasi-saturation, impact-ionization and self-heating, took places in high voltage unipolar power electronic devices Simulation And Experimental Data was matched Our Investigation And Parameter Extraction.

4.6.References

[1] A. Elasser, T. P. Chow: „Silicon Carbide Benefits and Advantages for Power Electronics Circuits and Systems“, Proceedings IEEE, pp. 963. – 986., Vol. 90(6), (2002.)

[2] V. Lindefelt, H. Iwata, Book Chapter in W. J. Chayke, H. Matsunami, G. Pensl: „Silicon-Carbide, Recent Major Advances“, Springer – Verlag, Berlin, (2004.)

[3] B. J. Baliga: „Silicon – Carbide Power Devices“, World Scientific Publishers, (2005.)

[4] M. Anderson, P. Kuivalainen: ″Physical Modelling of Vertical DMOS Power Transistors for Circuit Simulation″, Physica Scripta, Vol T 54, pp. 157.-158.(1994.)

[5] M. Hasanuzzaman, S. K. Islam, L. M. Tolbert, B. Ozpineci: „Analytical Modelling of Vertical Double Imolanted Power MOSFET (DIMOS) in 4H-SiC“, Proceedings of Connecticut Symposium on Microelectronics and Optoelectronics, Connecticut, (March 2002.)

[6] J. N. Shenoy, J. A. Cooper, M. R. Mellouch: „High Voltage Double Implanted Power MOSFETs in 6H-SiC“, IEEE Electron Devices Letters, Vol. 8, No 3, pp. 93.-95.(1997.)

[7] M. Hasanuzzaman, S. K. Islam: „Analytical Modelling of Vertical Double-Implanted Power MOSFET (DIMOS) in 4H-SiC“, Proceedings of Connecticut Symposium on Microelectronics and Optoelectronics, Connecticut, (March 2002.)

[8]M. D. Hasanuzzaman, Syed R. Islam, Leon M. Tolbert, Burak Ozpineci: „Design, Modeling, Testing and Spice parameter Extraction of DIMOS Transistor in 4H-SiC“, Frontiers in Electronics, pp. 733.-746.(2005)

[9] Pierre Ramond: „Field Theory – A Modern Primer“, The Benjamin Cummings Publishing Company, Inex, (1984.)

[10] M. Andersson, P. Kuivalainen: „Physical Modelling of Vertical DMOS Power Transistors for Circuit Simulation“, Physica Scripta, Vol. T54, pp. 157. – 158., (1994.)

[11] M. D.Hasanuzzaman, S. K. Islam, L. M. Tolbert, B. Ozpineci: „Design, Modeling, Testing and Spice Parameter Extraction of DIMOS Transistor in 4H-SiC“, Frontiers in Electronics, pp. 733. – 746., (2005.)

[12] S. R. de Groot, L. G. Suttorp: „Foundations of Electrodynamics“, North-Holland

Publishing Company, Amsterdam, (1972.)

[13] Yogesh Singh Chauhan et. al.: „Scalable General High Voltage MOSFET Model Including Quasisaturation and Self-Heating Effects“, Solid State Electronics, Vol. 50, pp. 1801. – 1813., (2006.)

[14] Cree. Research, Silicon . Carbide Product Specification,Version 981218.05

[15] Rifat M. Ramović, Rajko M. Šašić, Petar M. Lukić, J. Optoelectron. Adv. Mater. **8**(4), 1418.(2006.)

[16] Petar M. Lukić, Rajko M. Šašić, Boris B. Lončar, Aleksandar G. Žunjić, Optoelectronics and Adv. Mater. Rapid Communications, **5**(5), 551.(2011.)

[17] R. Šašić, P. M. Lukić, S. M. Ostojić, R. M. Ramović, J. Optoelectron. Adv. Mater. **10**(12), 3430 (2008.)

[18] Rajko M. Šašić, Petar M. Lukić, Stanko M. Ostojić, J. Optoelectron. Adv. Mater., 12(5), 1161.(2010.)

[19] Yogesh Singh Chauhan et. al.: „Scalable general high voltage MOSFET model including quasisaturation and self-heating effects“, Solid State Electronics, **50**, 1801 (2006.)

[20] M. Hjelm, H- E. Nilsson, A. Martinez, K. F. Brennan, E. Belloti: Materials Science Forum, 338 – 342 (2000.), pp. 1335. – 1338.

[21] Cree research: “Silicon Carbide Product Specification”, version 981218.05

[22] R. M. Ramović, R. M. Šašić and P. M. Lukić: Journal of Optoelectronics

[23] M. D. Hasanuzzaman, S. K. Islam, L. M. Tolbert and B. Ozpineci: Frontiers in Electronics, (2005.), pp. 733. – 746.

[24] P. M. Lukic, R. M. Sasic, B. B. Lončar and A. G. Žunjić: Optoelectronics and Advanced Materials Rapid Communications 5 (5) (2011.),.pp. 551. - 554.

[25] W. J. Schaffer, H. G. H. Negley, K. G. Irvine and J. P. Palmour: MRS Proceedings, 339 (1994.), pp. 595. – 600.

[26] M Roschke and F. Schwiertz: IEEE Trans. Elec. Devices, 48 (7) (2001.), pp. 1442. – 1447.

[27] H. E. Nilsson, K. Bertilsson, M. Hjelm and E. Dubaric: Journal of Wide Bandgap Materials 9 (4) (2002.), pp. 293. – 305.

[28] L. C. Yu: “Simulation, Modeling and Characterization of SiC Devices”, The State University of New Jersey, Graduate School – New Brunswick Rutgers, PhD Dissertation, (2010).

[29] J. Scoffed, R. Sei-Hyung, S. Krishnaswami, H. Fatima and A. K. Agarwal: “1.8kV

10mΩcm2 4H-SiC JFETs", (2006.), preprint - AFRL-PR-WP-TP-2007-207, Report No AD-A464844

[30] B. J. Baliga: "Silicon Carbide Power Devices", World Scientific Publishers (2005.)

[31] W. J. Choyke, H. Matsunami and G. Pensl: "Silicon Carbide, Recent Major Advances" (U. Lindefelt, H. Iwata - Book Chapter), Springer – Verlag, Berlin (2004.)

5. Conclusion

The subject of interest of this dissertation is silicon carbide because of it's enhancing role in electronics, especially power electronics. Its first chapter is recognized as introduction and justifies the limits of silicon based components. It also announces the possible advantages of silicon carbide counterparts. Naturally, beside a lot of superior features silicon carbide also has several shortcomings, but they are expected to be overcome by the development of its manufacturing technology.

The second chapter is entirely devoted to the physical and electrical properties of silicon carbide. The crystal lattice of 4H-SiC, 6H-SiC and 3C-SiC poly type has been described in details special attention has been paid to parameters relevant for the construction of components in power electronics, such as saturation velocity, low field mobility and thermal conductivity, always comparing their values and doping level of temperature dependences with the situation usually met in the case of other semi conducting material.

The third chapter deals with the electronic components in which silicon carbide plays the main role. The entire spec turn of them has been mentioned, some of them where described in more details but the full attention has been only paid to VDIMOS. with all necessary mathematically derivations. Physical aspects of such structure performances were considered carefully, pointing out all shortcomings and problems appearing in the available literature.

The fourth chapter explains the contribution of this dissertation to the investigation of VDIMOS as a representative of important silicon carbide based electronic devices. For the first time quasi- analytical contemplation of two dimensional Poisson' equation concerning drift region has been carried out. This way obtained position dependent electric fields were the starting point for the construction of the lagrangion density of the current flow. Further use of the minimal action principle has lead to the approximate calculation of geometric parameters current flow in the drift region. Special attention has been paid for relation describing drift diffusion transport of carriers in drift region that is improved by fine tuning parameter. Its influence on flow profile and the value of drain current has been successfully calculated. last but not least silicon carbide is to known to be anisotropic material for a certain level (6H- SiC is strongly anisotropic, while 4H-SiC possesses not so salient anisotropy). This anisotropy was expected to have influence on device design and modeling, what was confirmed in our instigations.

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Студијски програм : Technical physics

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